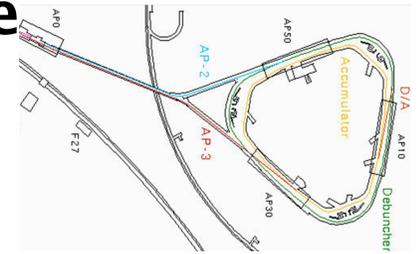




# FPGA-Based Instrumentation for the Fermilab Antiproton Source

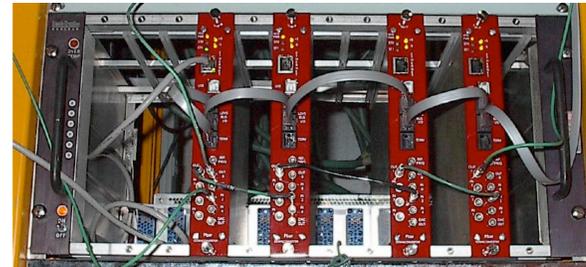
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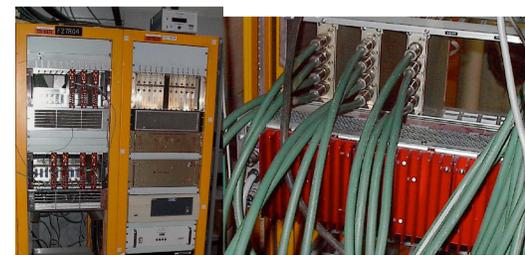


## Abstract

We have designed and built low-cost, low-power, Ethernet-based circuit boards to apply DSP techniques to several instrumentation updates in the Fermilab Antiproton Source. Commodity integrated circuits such as direct digital synthesizers, D/A and A/D converters, and quadrature demodulators enable digital manipulation of RF waveforms. A low cost FPGA implements a variety of signal processing algorithms in a manner that is easily adapted to new applications. An embedded microcontroller provides FPGA configuration, control of data acquisition, and command-line interface. A small commercial daughter board provides an Ethernet-based TCP/IP interface between the microcontroller and the Fermilab accelerator control network. The boards are packaged as standard NIM modules. Applications include Low Level RF control for the Debuncher, readout of transfer-line Beam Position Monitors, and narrow-band spectral analysis of diagnostic signals from Schottky pickups.



NIM modules connect to ACNET via Ethernet. Nearby modules communicate over an ad-hoc LVDS bus.

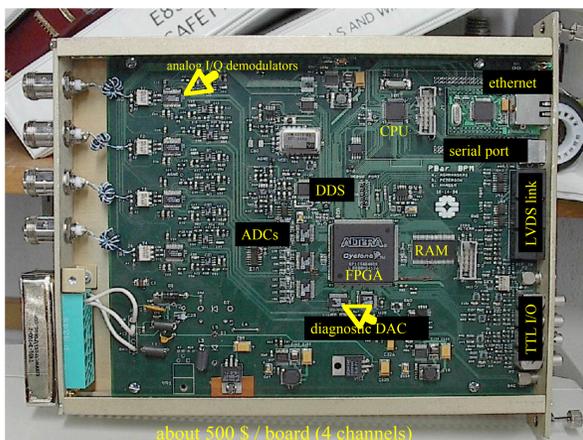
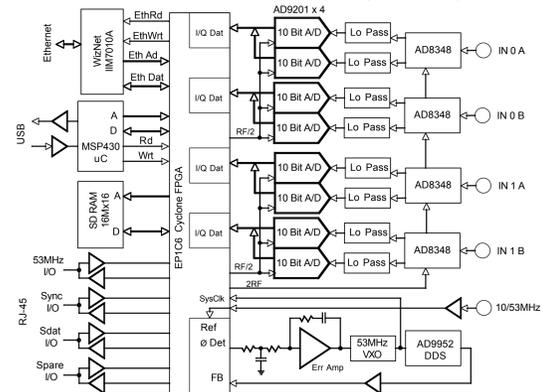


Modules were designed to minimize changes to existing infrastructure. Left: new and legacy systems side-by-side. Right: new modules receiving cables from AP2 line tunnel.

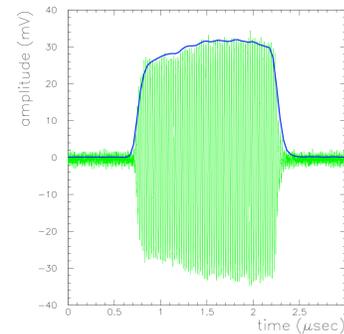
## 53 MHz BPM downconverter for the AP2 transfer line

The 34 BPMs in the AP2 line are unusual in that they see only 53 MHz bunch structure, they see relatively small ( $10^{10}$ ) numbers of particles per spill, and many signal cables see significant crosstalk from the Debuncher injection kicker. Reliable BPM measurements for reverse protons are needed to characterize the AP2 lattice, as part of an acceptance upgrade project. Readout during normal operation is also useful for monitoring orbit stability and recording secondary particle flux along the line.

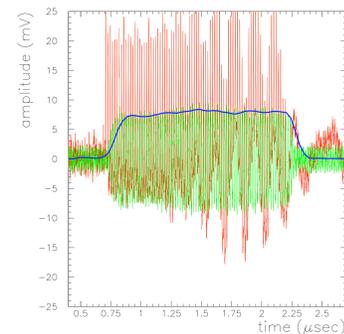
Debuncher Transfer Line BPM Card (2 BPMs/card)



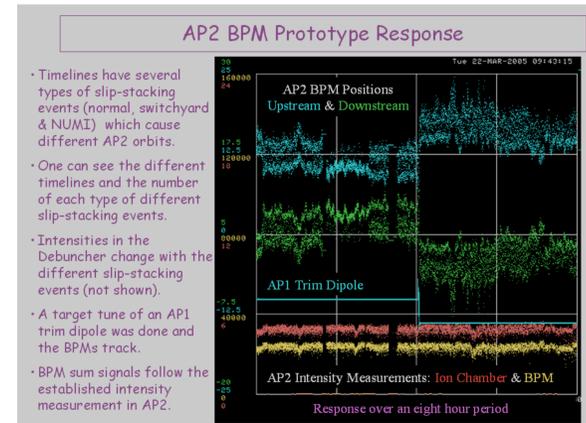
about 500 \$ / board (4 channels)



Green: BPM signal read from oscilloscope (includes bandpass filter). Blue: 53 MHz envelope read from BPM board's RAM.



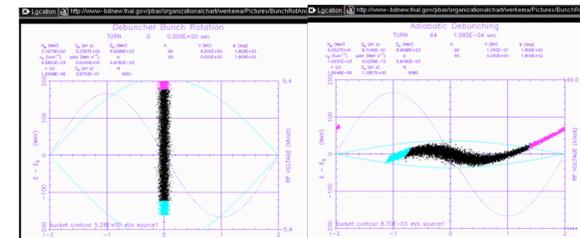
A particularly noisy BPM signal. Red: oscilloscope trace without bandpass filter, showing kicker crosstalk. Green, blue: as above.



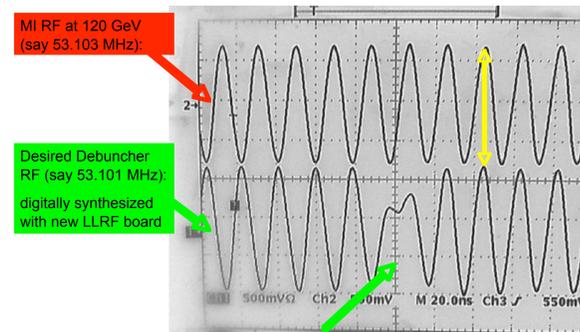
(Courtesy of Keith Gollwitzer).

## Debuncher RF phase jump

- Decouples Debuncher RF frequency from Main Injector 120 GeV frequency
- Few kHz tuning range about 53.1 MHz
- Center MI & Debuncher orbits simultaneously
- Added degree of freedom facilitates upcoming recalibration of "8 GeV" across machines

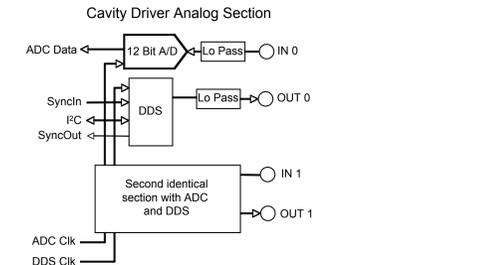


ESME simulator (courtesy S.Werkema) illustrating Debuncher bunch rotation when center of momentum aperture and center of RF bucket do not coincide—the case before implementing phase jump.



Before MI extraction, jump phase of synthesized Debuncher RF to match measured phase of MI RF, plus programmable offset phase jump → bucket-to-bucket transfer still works

The next production run of phase jump modules will be of sufficient quantity to drive each Debuncher cavity with its own digital synthesizer and to monitor its feedback signal, eventually replacing the legacy LLRF system. We hope to provide more precise phase alignment with reduced human intervention.



Block diagram of analog input/output section of phase jump / LLRF board. The digital section uses the same design as the BPM board.

## Digital framework

```

begin
  -- hypot_idf
  -- calculate sqrt((I^2+Q^2)) given I and Q
  -- begin 2009-02-10 by wja
  title "calculate sqrt(I^2+Q^2)";
  include "ipm_ff.inc";
  include "ipm_adc.inc";
  include "ipm_adc_sub.inc";
  include "altert.inc";
  parameters
  Q;
  sum = sum + ipm_adc_sub(I, Q);
  report "sum (I^2) must be a positive integer" when
  severity ERROR;
  addsign hypot
  cl;
  ipm_adc(I);
  ipm_adc(Q);
  sqrt(I^2+Q^2);
end;
  
```

Simple FPGA code example: computing sqrt(I<sup>2</sup>+Q<sup>2</sup>)

```

BusRdData[ ] = BusAddr[ ] == h"0001" & h"deadbeef";
BusWrData[ ] = BusAddr[ ] == h"0002" & h"uptime,q";
  
```

Defining bus-addressable registers and reading/writing them via remote network connection.



Seeing bus-addressable registers from ACNET.

## Acknowledgments

We are indebted to B. Chase, G. Dugan, G.W. Foster, K. Gollwitzer, D. McGinnis, S. Pordes, M. Tigner, and S. Werkema for advice and inspiration.

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## References

- Tevatron I design report, Fermilab, 1984.
- P. Adamson, et al., "Operational performance of a bunch by bunch digital damper in the Fermilab Main Injector," these proceedings.