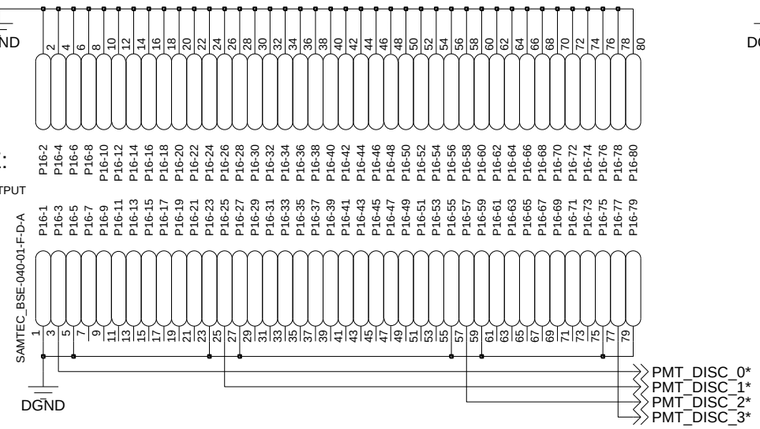
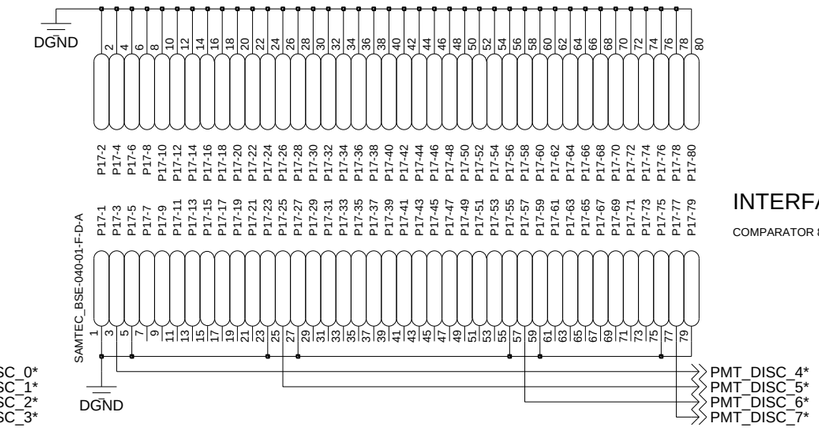


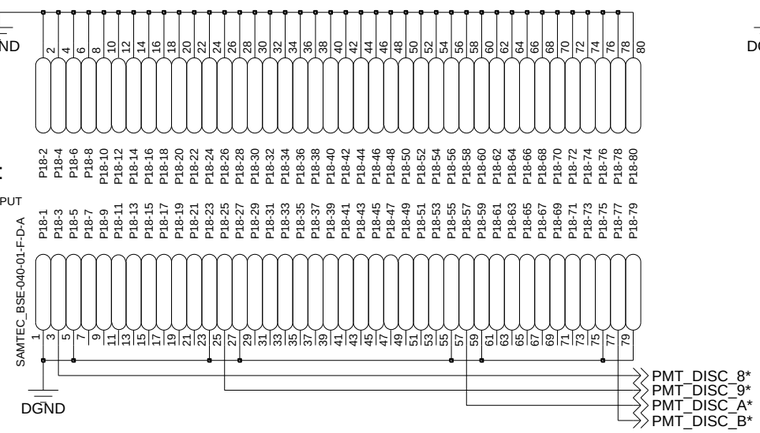
INTERFACE:

COMPARATOR 0..3 OUTPUT



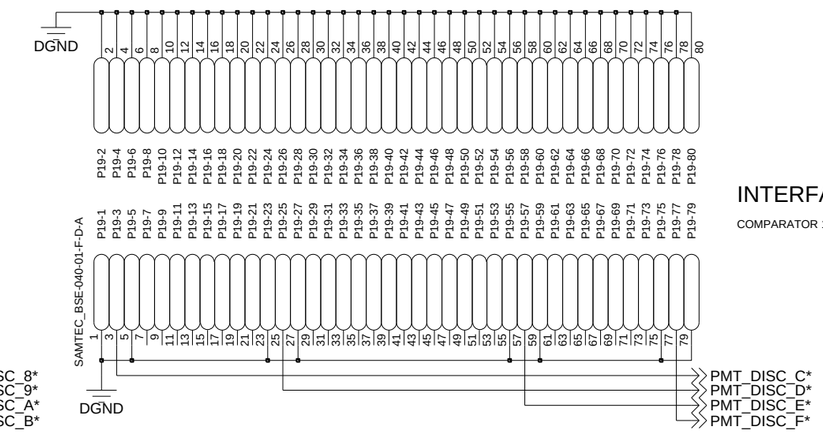
INTERFACE:

COMPARATOR 8..11 OUTPUT



INTERFACE:

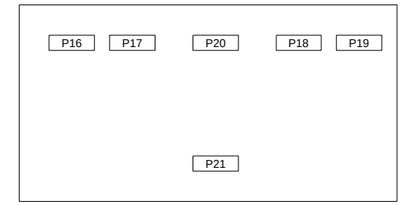
COMPARATOR 4..7 OUTPUT



INTERFACE:

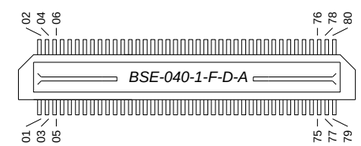
COMPARATOR 12..15 OUTPUT

CONNECTOR PLACEMENT



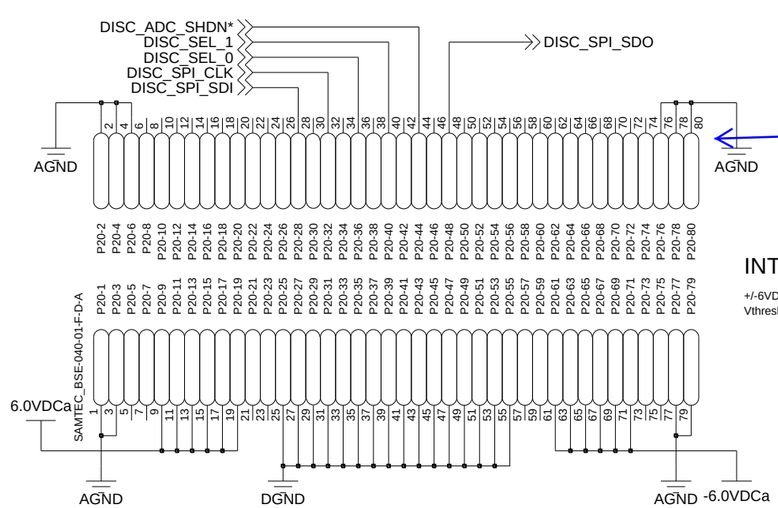
CONNECTOR PINOUT

.8mm DOUBLE ROW SOCKET ASSEMBLY



Board-to-Board Spacer:

McMaster-Carr:	93505A460
Type:	Male/Female Threaded Hex
Material Type:	Aluminum
BodyLength:	3.16" (0.1875", 4.75mm)
Hex Width:	3.16" (0.1875", 4.75mm)
Male Screw Size:	4-40
Female Tread Size	4-40



Each pin is numbered RIGHT of the symbol. This makes DISC_ADC_SHDN* connected to P20-44 and not P20-42 as called for in the AFE design.

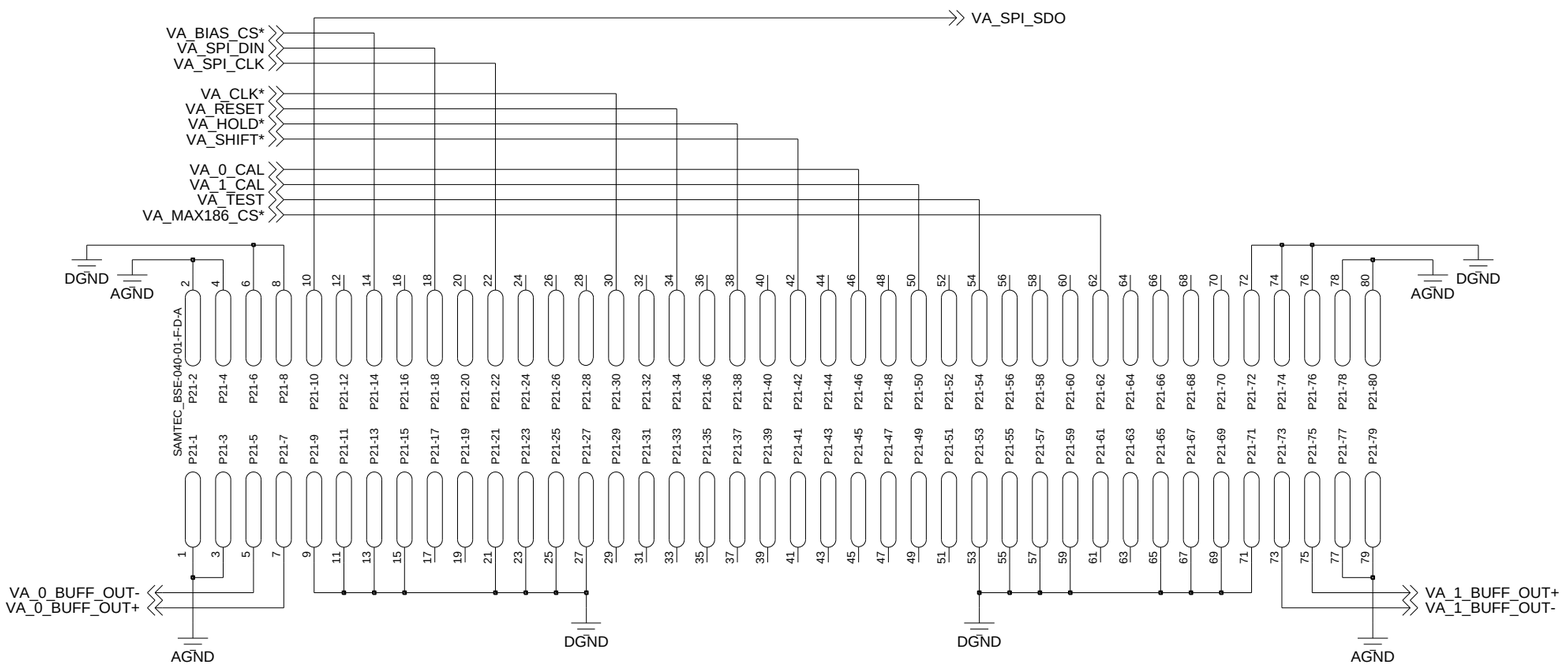
INTERFACE:

+/-6VDC power, Ground, Analog Ground
Vthresh SPI

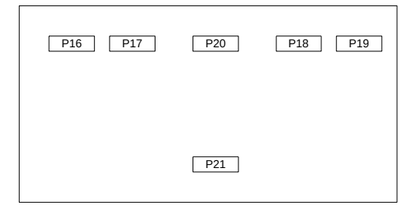
NOTE: DISCRIMINATOR SIGNALS

1.1) Current monitoring removed from AFE, removed signals *-IMON
1.2) Signal names consistant between AFE and STAC designs

STAC		
Analog Front End interface - Discriminator		
Rev	**Designed By**	**Saved Date**
C4	J. Ameel	Saturday, August 22, 2009
		8:08:43 am
		Sheet 01 of 13

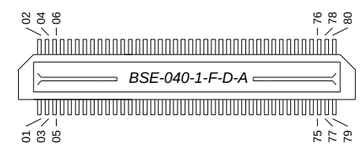


CONNECTOR PLACEMENT

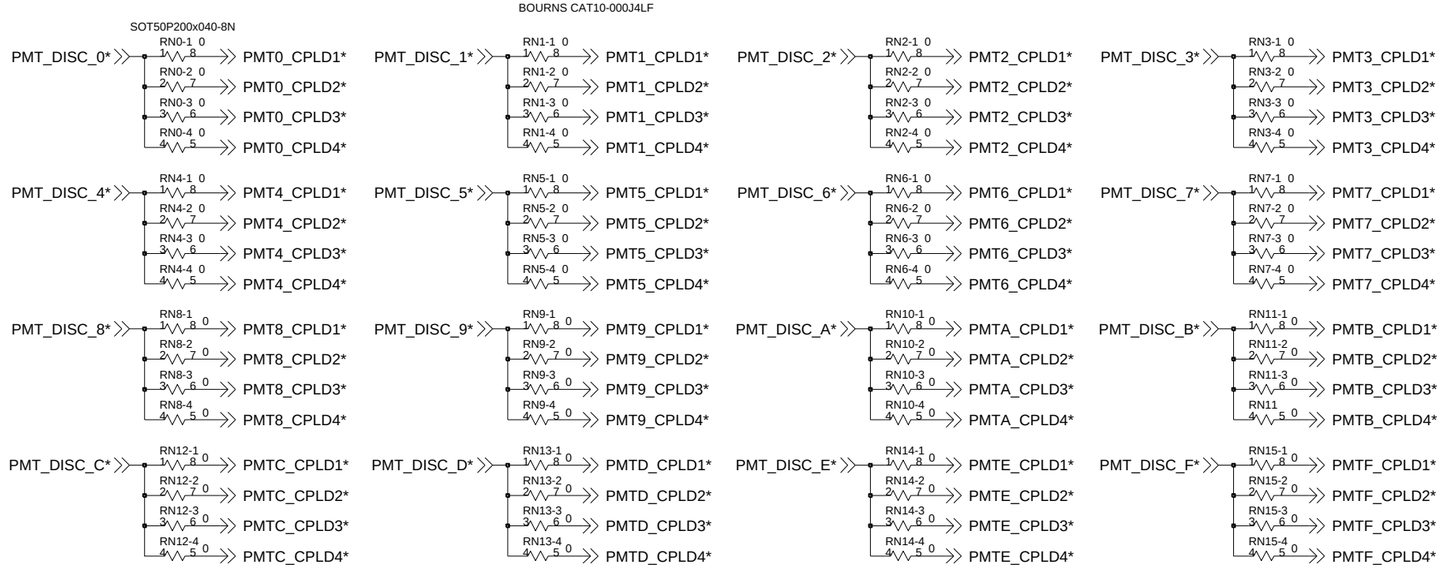


CONNECTOR PINOUT

.8mm DOUBLE ROW SOCKET ASSEMBLY



Zero ohm resistor network similar to:
BOURNS CAT10-000J4LF



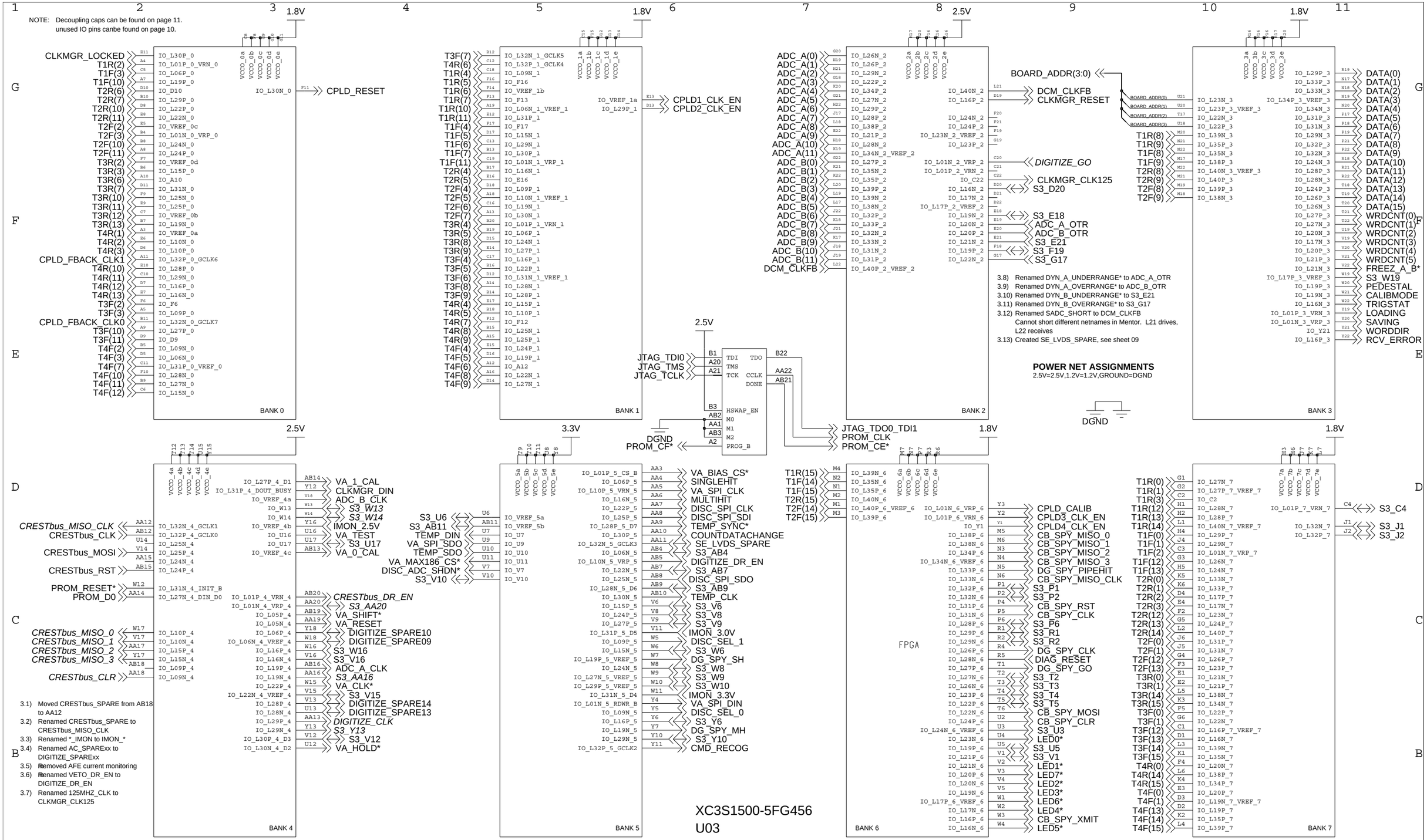
Board-to-Board Spacer:

McMaster-Carr:	93505A460
Type:	Male/Female Threaded Hex
Material Type:	Aluminum
BodyLength:	3.16" (0.1875", 4.75mm)
Hex Width:	3.16" (0.1875", 4.75mm)
Male Screw Size:	4-40
Female Tread Size	4-40

2.1) Testpoints omitted in favor of large vias (VIA_160-095-175)
2.2) Current monitoring signals removed from AFE, removed from this page
2.3) Signal names match between AFE and STAC design

STAC		
VA circuitry header interface, comparator output discribution circuitry		
Rev	**Designed By**	**Saved Date**
C4	J. Ameel	Tuesday, September 8, 2009
		5:10:25 pm
		Sheet 02 of 13

NOTE: Decoupling caps can be found on page 11.
unused IO pins canbe found on page 10.

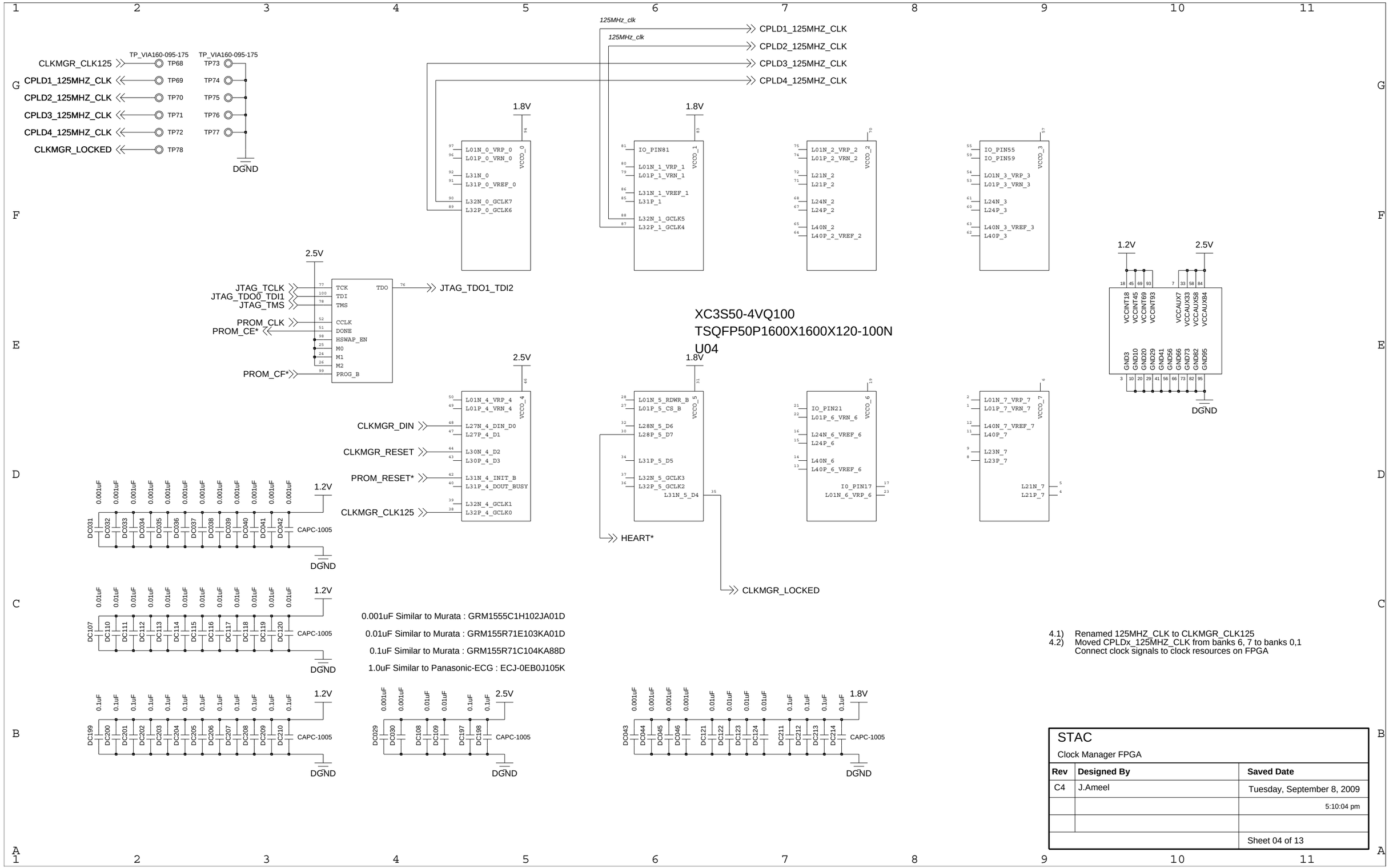


3.8) Renamed DYN_A_UNDERRANGE* to ADC_A_OTR
3.9) Renamed DYN_A_OVERRANGE* to ADC_B_OTR
3.10) Renamed DYN_B_UNDERRANGE* to S3_E21
3.11) Renamed DYN_B_OVERRANGE* to S3_G17
3.12) Renamed SADC_SHORT to DCM_CLKFB
Cannot short different netnames in Mentor. L21 drives, L22 receives
3.13) Created SE_LVDS_SPARE, see sheet 09

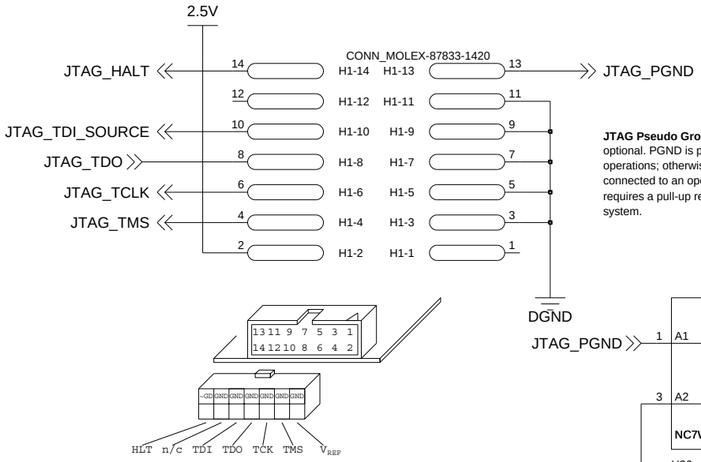
POWER NET ASSIGNMENTS
2.5V=2.5V,1.2V=1.2V,GROUND=DGND

3.1) Moved CRESTbus_SPARE from AB18 to AA12
3.2) Renamed CRESTbus_SPARE to CRESTbus_MISO_CLK
3.3) Renamed *_IMON to IMON_*
3.4) Renamed AC_SPAREx to DIGITIZE_SPAREx
3.5) Removed AFE current monitoring
3.6) Renamed VETO_DR_EN to DIGITIZE_DR_EN
3.7) Renamed 125MHZ_CLK to CLKMGR_CLK125

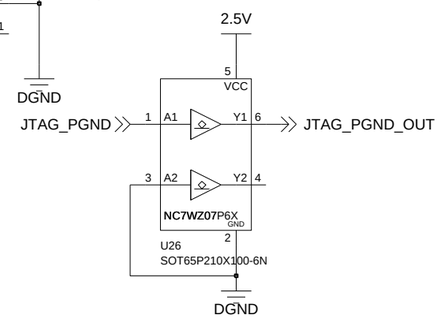
STAC	Main Spartan 3 FPGA	Rev: C4	Designed By: J.Ameel	Last Save: Tuesday, September 8, 2009	University of Michigan	Physics	Sheet: 03 of 13


CLKMGR_CLK125
CPLD1_125MHZ_CLK
CPLD2_125MHZ_CLK
CPLD3_125MHZ_CLK
CPLD4_125MHZ_CLK
CLKMGR_LOCKED
TP_VIA160-095-175
TP68
TP69
TP70
TP71
TP72
TP78
TP73
TP74
TP75
TP76
TP77
DGND
125MHz_clk
1.8V
2.5V
1.2V
JTAG_TCLK
JTAG_TDO0_TDI1
JTAG_TMS
PROM_CLK
PROM_CE*
PROM_CF*
TCK
TDI
TMS
CCLK
DONE
HSWAP_EN
M0
M1
M2
PROG_B
TDO
JTAG_TDO1_TDI2
XC3S50-4VQ100
TSQFP50P1600X1600X120-100N
U04
CLKMGR_DIN
CLKMGR_RESET
PROM_RESET*
HEART*
VCCO_0
VCCO_1
VCCO_2
VCCO_3
VCCO_4
VCCO_5
VCCO_6
VCCO_7
VCCINT18
VCCINT45
VCCINT69
VCCINT93
VCCAUX7
VCCAUX33
VCCAUX58
VCCAUX84
GND3
GND10
GND20
GND29
GND41
GND56
GND66
GND73
GND82
GND95
CAPC-1005
0.001uF Similar to Murata : GRM1555C1H102JA01D
0.01uF Similar to Murata : GRM155R71E103KA01D
0.1uF Similar to Murata : GRM155R71C104KA88D
1.0uF Similar to Panasonic-ECG : ECJ-0EB0J105K
4.1) Renamed 125MHZ_CLK to CLKMGR_CLK125
4.2) Moved CPLDx_125MHZ_CLK from banks 6, 7 to banks 0,1
Connect clock signals to clock resources on FPGA
STAC
Clock Manager FPGA
Rev
Designed By
Saved Date
C4
J.Ameel
Tuesday, September 8, 2009
5:10:04 pm
Sheet 04 of 13

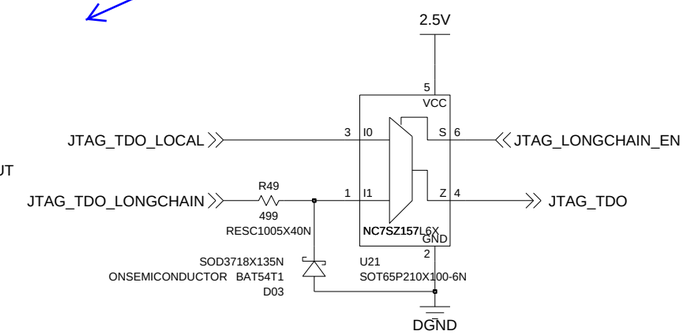
JTAG INTERFACE -INPUT



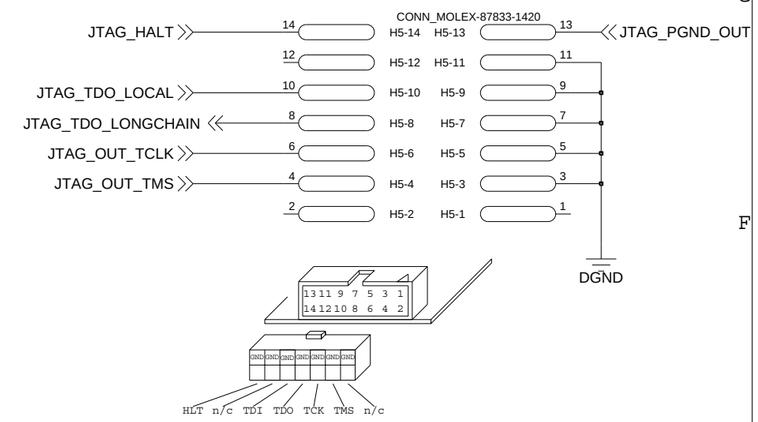
JTAG Pseudo Ground. Use of this pin is optional. PGND is pulled Low during JTAG operations; otherwise, it is high-Z. This pin is connected to an open-drain driver and requires a pull-up resistor on the target system.



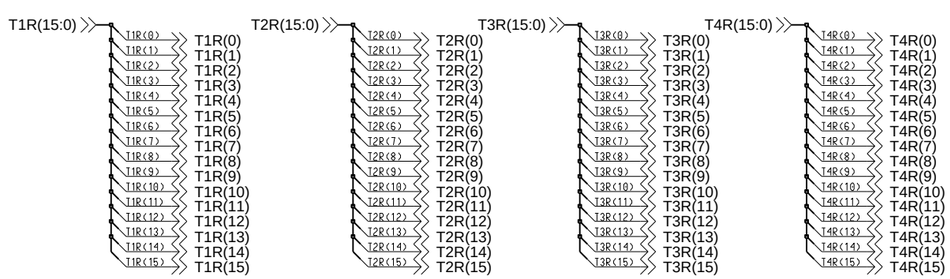
MORE TESTPOINTS!

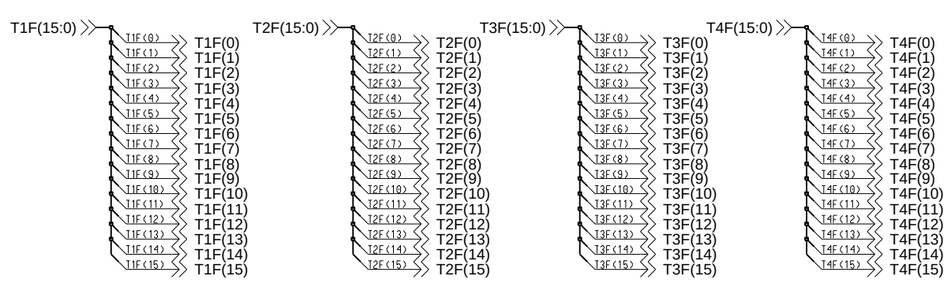


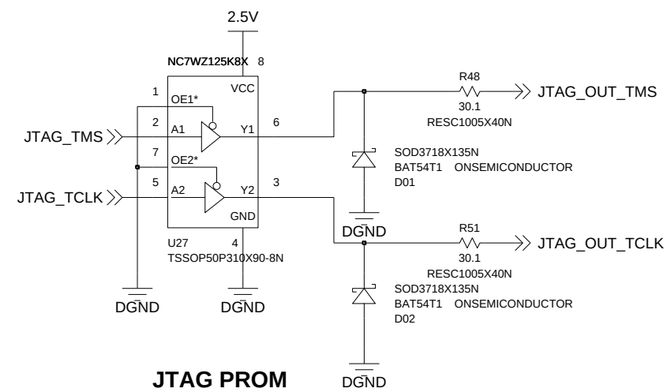
JTAG INTERFACE - OUTPUT



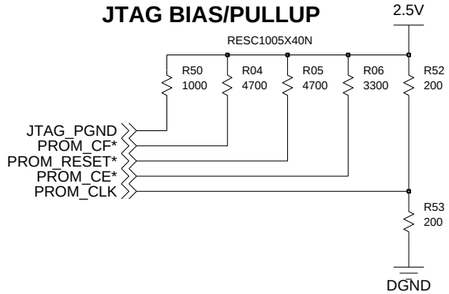
TIMING BUS NOTATION FOR RISING AND FALLING EDGES



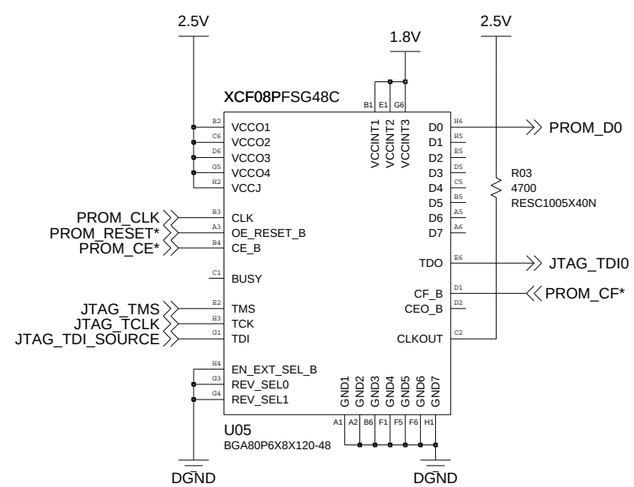




JTAG BIAS/PULLUP

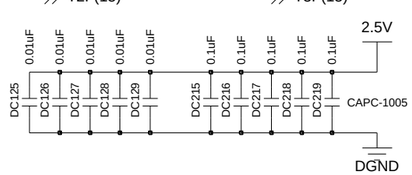


JTAG PROM

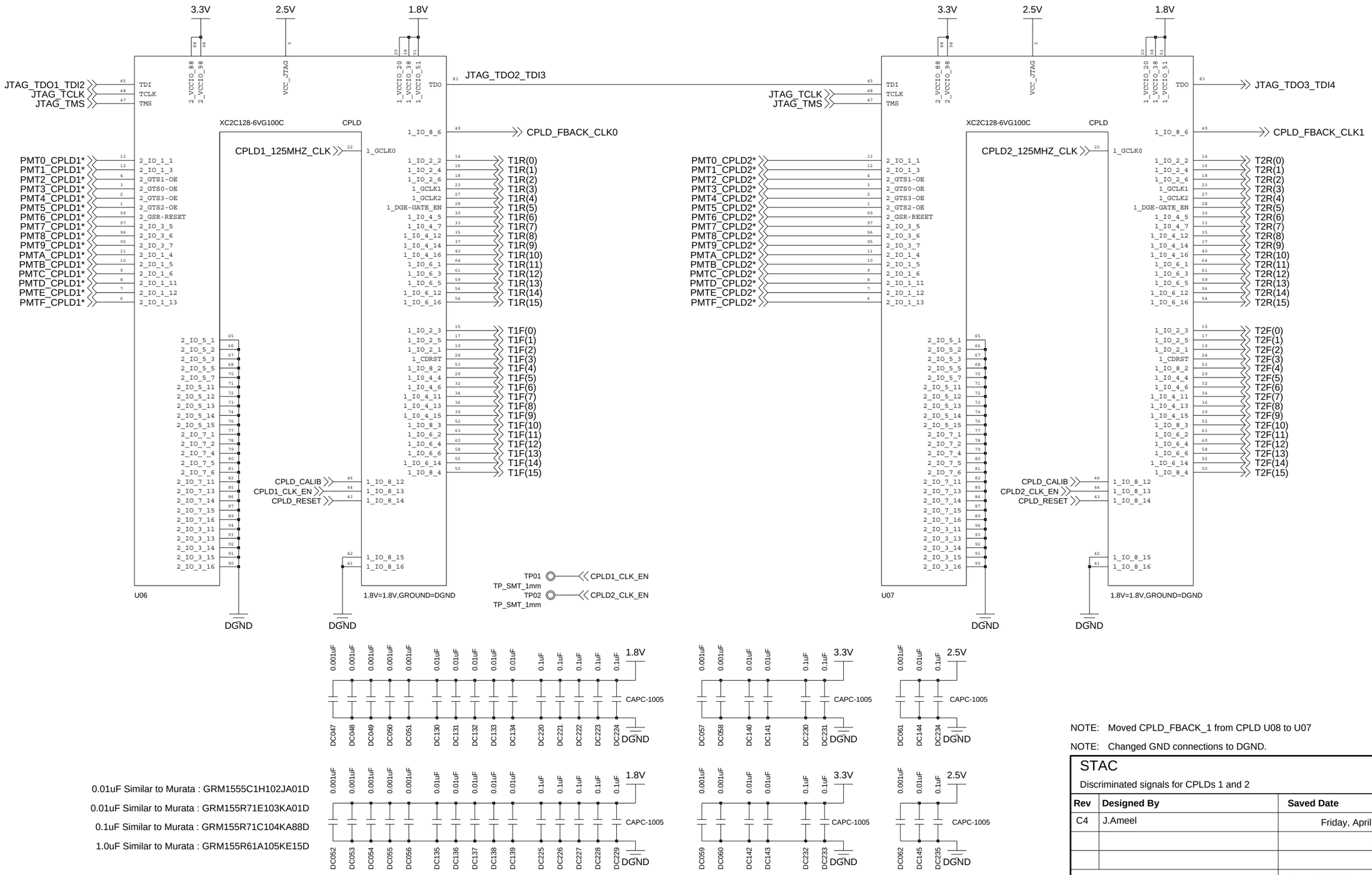


5.1) Added 200 ohm bias to PROM_CLK
5.2) Added LongChain TDO multiplexer.
Added OUT_TCLK and OUT_TMS buffer
Added PGND driver chip
Changed XCF08P symbol to show VCCINT and GND pins
5.3) Removed 2.5V from JTAG output header
5.4) Tied floating input U26-3 to GND

0.01uF Similar to Murata : GRM1555C1H102JA01D
0.01uF Similar to Murata : GRM155R71E103KA01D
0.1uF Similar to Murata : GRM155R71C104KA88D
1.0uF Similar to Murata : GRM155R61A105KE15D



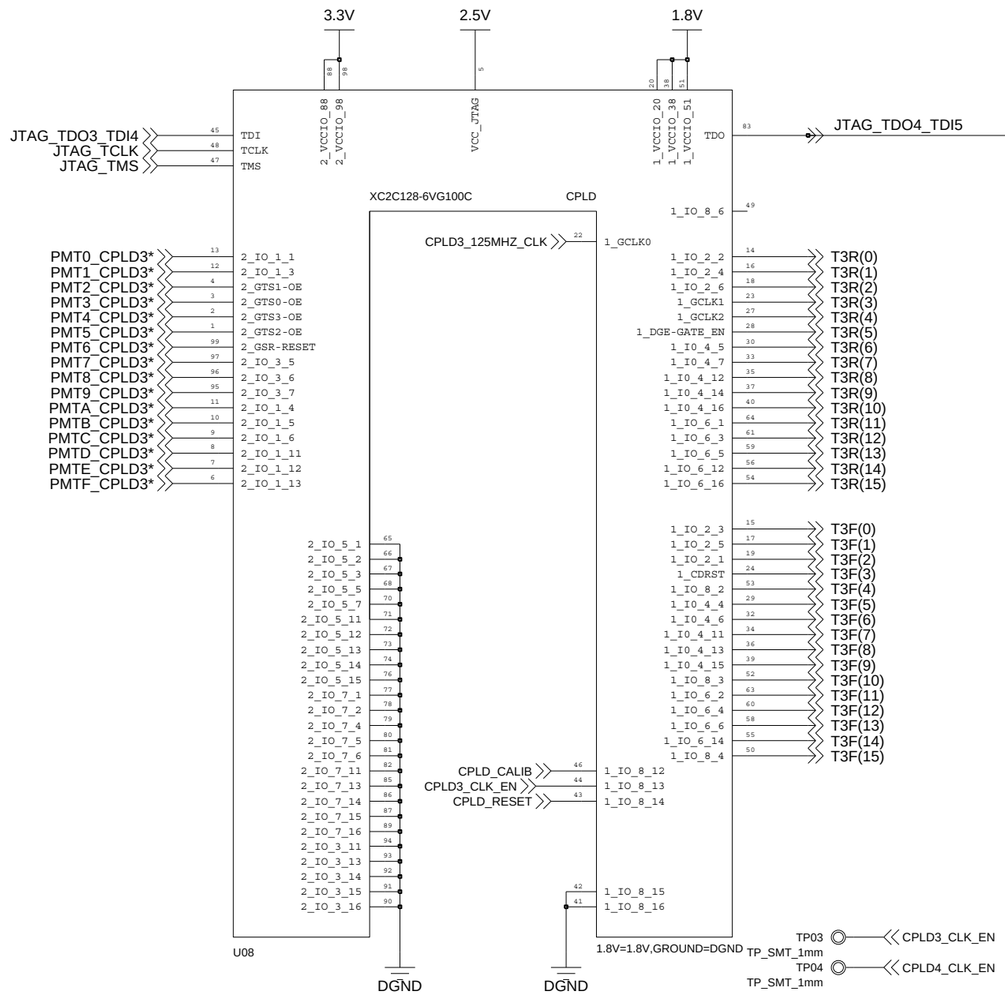
STAC		
PROM, JTAG interface, JTAG chain circuitry		
Rev	**Designed By**	**Saved Date**
C4	J.Ameel	Tuesday, September 8, 2009
		5:09:59 pm
		Sheet 05 of 13

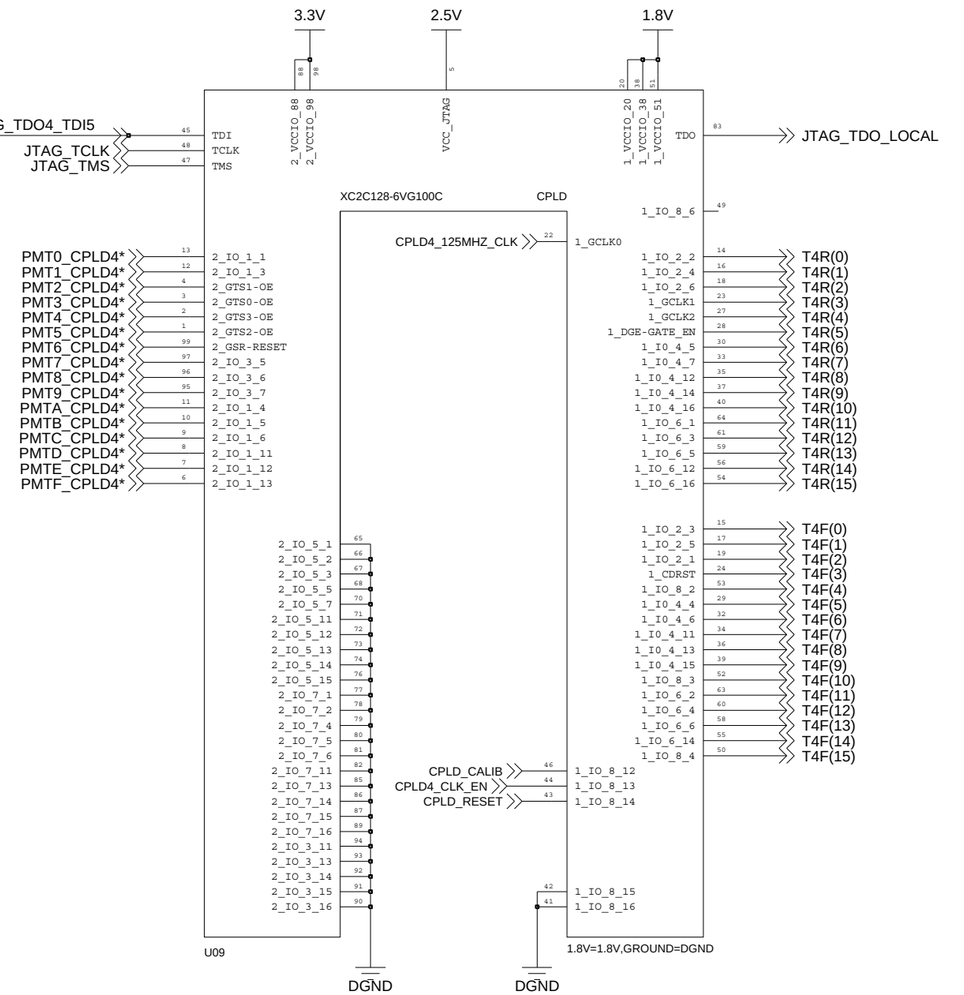


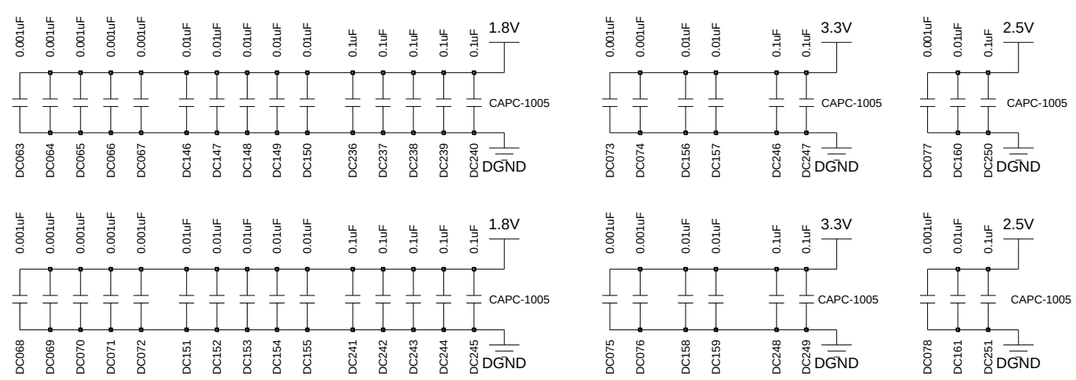
NOTE: Moved CPLD_FBACK_1 from CPLD U08 to U07

NOTE: Changed GND connections to DGND.

STAC		
Discriminated signals for CPLDs 1 and 2		
Rev	**Designed By**	**Saved Date**
C4	J.Ameel	Friday, April 17, 2009
		3:48:59 am
		Sheet 06 of 13







0.01uF Similar to Murata : GRM1555C1H102JA01D

0.01uF Similar to Murata : GRM155R71E103KA01D

0.1uF Similar to Murata : GRM155R71C104KA88D

1.0uF Similar to Murata : GRM155R61A105KE15D

NOTE: Changed JTAG_TDO5_TDI6 to JTAG_TDO_LOCAL

NOTE: Moved CPLD_FBACK_1 from CPLD U08 to U07

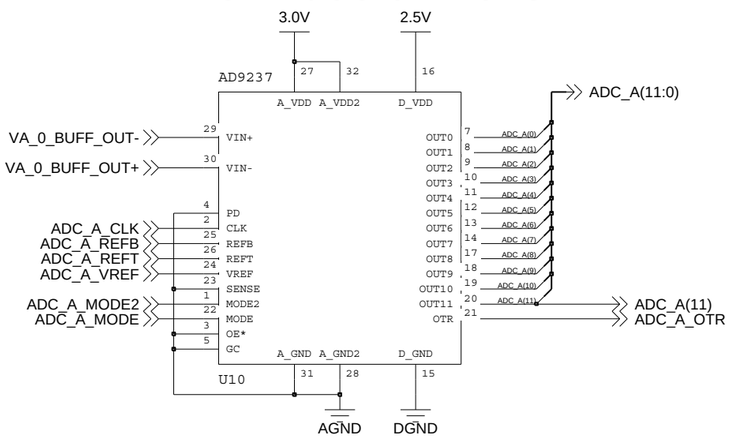
NOTE: Changed GND connections to DGND.

STAC

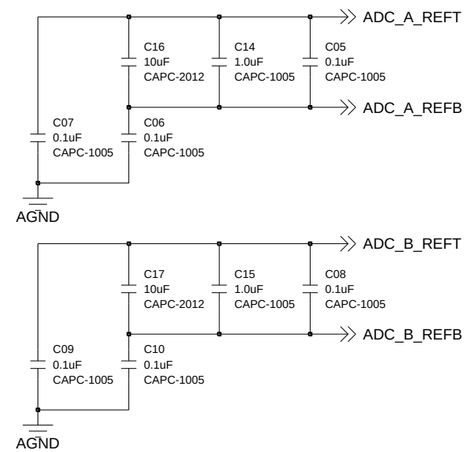
Discriminated signals for CPLDs 3 and 4

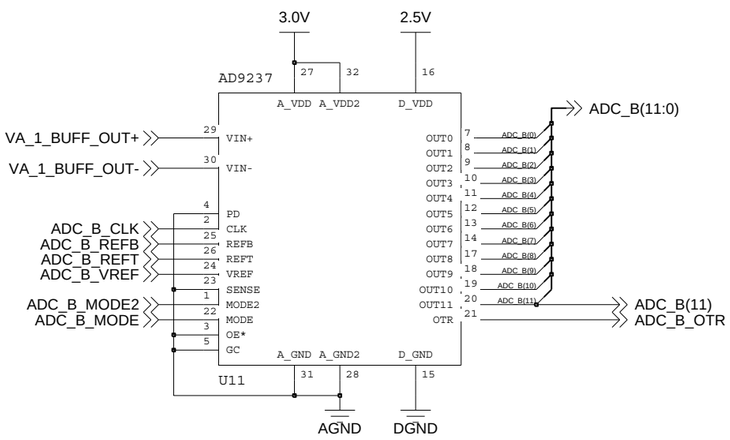
Rev	Designed By	Saved Date
C4	J.Ameel	Friday, April 17, 2009
		3:50:09 am
		Sheet 07 of 13

DUAL AD9237s FOR DYNODES

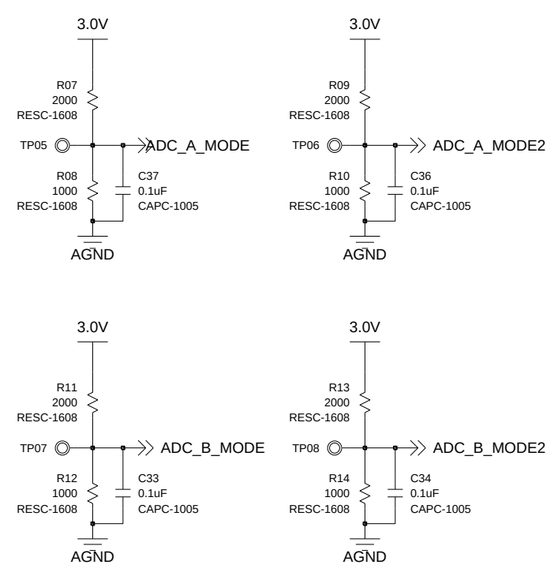


REFERENCE CAPACITORS





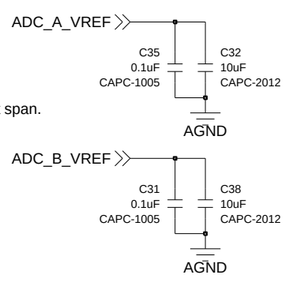
AD9237 MODE SETTINGS



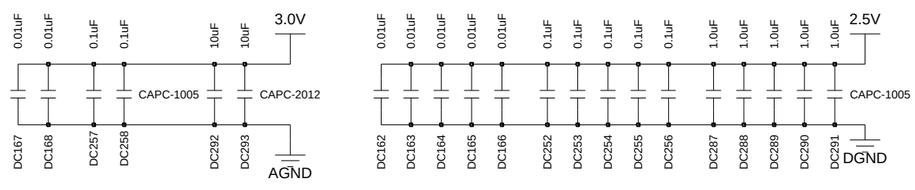
NOTE:

There is an error in the AD9237 datasheet.
It is only possible to choose an input span
of 1.0V or 2.0V. CREST requires a 2.0V input span.

SENSE = 0V VREF = floating but decoupled.



8.1) Fixed AnalogDevices error re: span and Vref
See note in section C2
8.2) Changed mode setting resistors from 10000 to 1000 ohms
8.3) Changed mode setting resistors from 20000 to 2000 ohms
8.4) Added capacitor to support ADC MODE signals
8.5) Removed OUT-OF-RANGE logic and circuitry
THIS CHANGE REQUIRES FIRMWARE CHANGE TO MATCH
8.6) Changed MODE2 setting resistors from 2/3 to 1/3 Vref

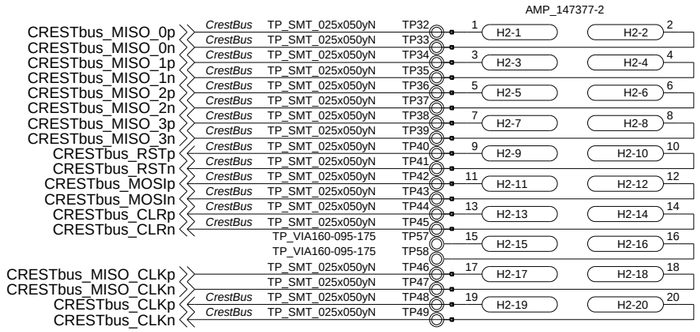


0.01uF Similar to Murata : GRM1555C1H102JA01D
0.01uF Similar to Murata : GRM155R71E103KA01D
0.1uF Similar to Murata : GRM155R71C104KA88D
1.0uF Similar to Murata : GRM155R61A105KE15D
10uF Similar to Murata : GRM21BR71A106KE51L

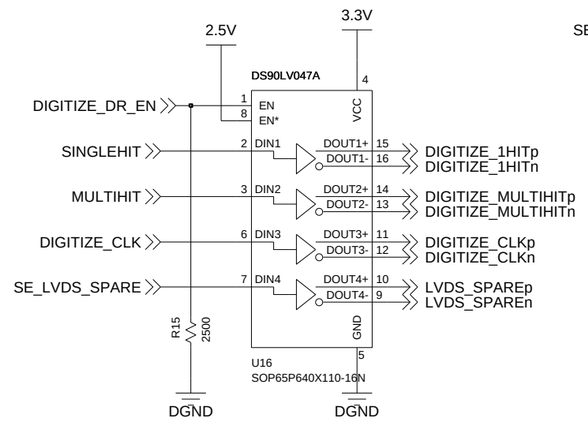
STAC		
A/D Conversion, ADC out-of-range decoding, mode setting		
Rev	**Designed By**	**Saved Date**
C4	J.Ameel	Thursday, September 3, 2009
		4:44:20 pm
		Sheet 08 of 13

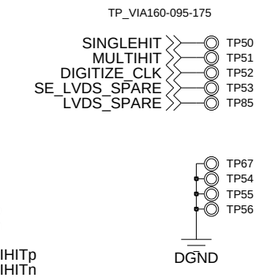
CRESTBUS INTERFACE

Testpoints are 0.25mm x 0.50mm Unused pins are routed to 2.54mm header



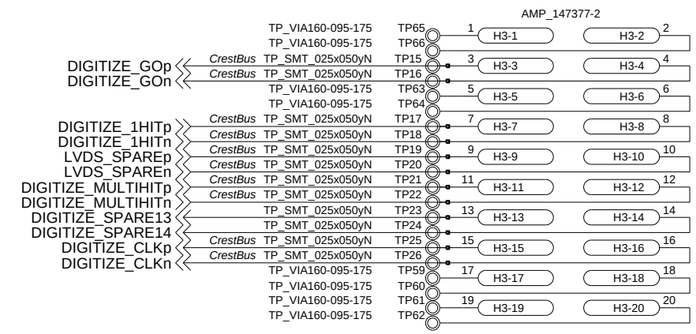
LVDS TRANSMITTER





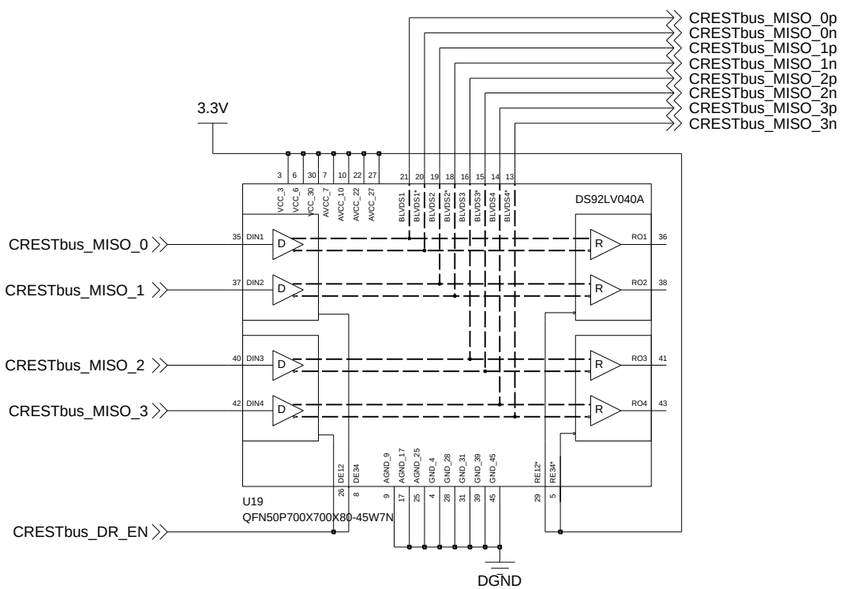
DIGITIZE REPORTING

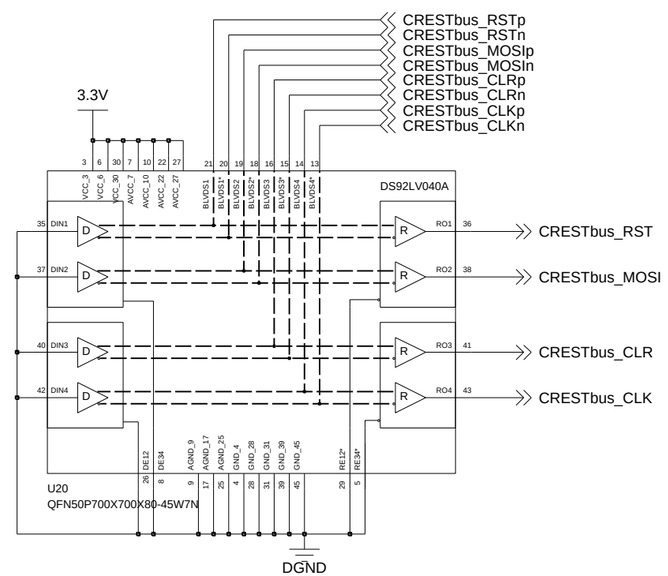
Testpoints are 0.25mm x 0.50mm Unused pins are routed to 2.54mm header

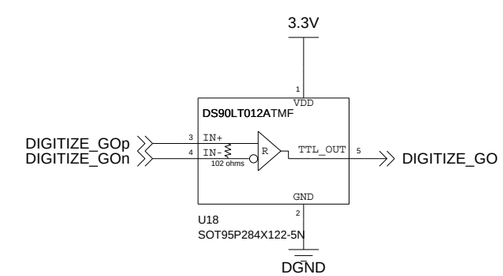


DIGITIZE SIGNAL BIAS

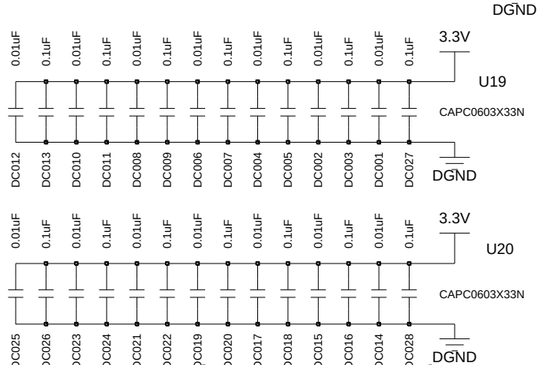
Digitize decision biasing handled within firmware
Bias resistors and custom rail removed from design







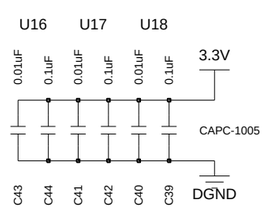
9.1) Removed +/- 6V from anticoincidence cable
9.2) Removed all termination resistors from CRESTbus
BLVDS termination installed only at both ends of the line.
9.3) BLVDS testpoints replaced with 0.25mm x 0.50mm pads
9.4) Renamed VETO_DR_EN to DIGITIZE_DR_EN
9.5) Renamed AC_SPARExx to DIGITIZE SPARExx
9.6) Removed DGND connection from CRESTbus and DIGITIZE Decision header
9.7) Removed DIGITIZE decision biasing resistors and rails
9.10) Tied DR_EN signal on U18 to disabled state (GND)
9.11) Assigned CRESTbus_SPARE to CRESTbus_MISO_CLK
9.12) Configured U17 as a BLVDS driver and removed FPGA control
9.13) Assigned unused SE to LVDS driver to a spare 0.1" testpoints
9.14) Created SE_LVDS_SPARE signal
9.15) Changed BLVDS drivers from always enabled to FPGA controlled

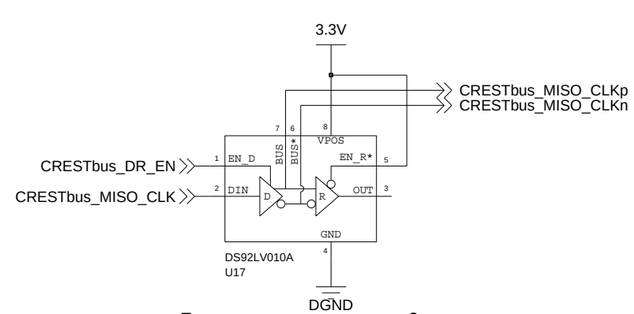


0.01uF Similar to Murata : GRM155R71E103KA01D

0.1uF Similar to Murata : GRM155R71C104KA88D

1.0uF Similar to Murata : GRM155R61A105KE15D





STAC		
Board I/O, AntiCoincidence signals, Bias and Termination		
Rev	**Designed By**	**Saved Date**
C4	J.Ameel	Tuesday, September 8, 2009
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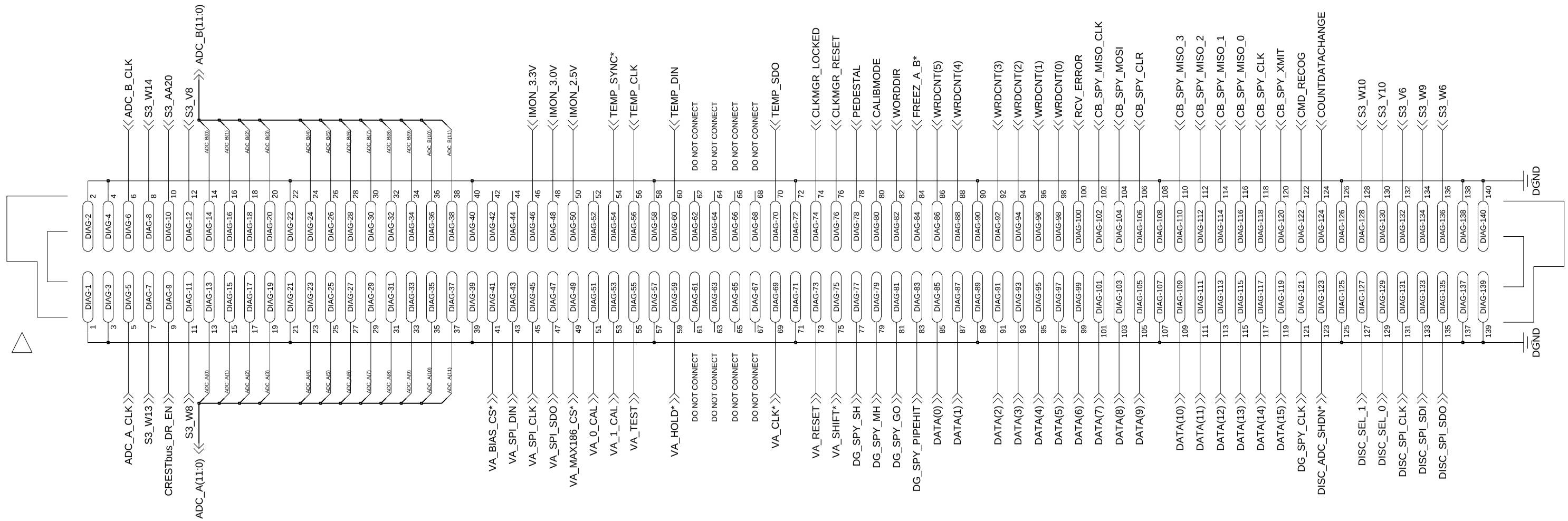
DIAGNOSTIC HEADER

AMP 5-5179009-6



10.1) Removed AFE current monitoring signals
10.2) Renamed x_IMON to IMON_x

NOTE: Replaced AMP 5-179031-6 (Plug) with AMP 5-5179009-6 (Recpt)

STAC		
Diagnostic Header		
Rev	**Designed By**	**Saved Date**
C4	J.Ameel	Tuesday, September 8, 2009
		5:08:55 pm
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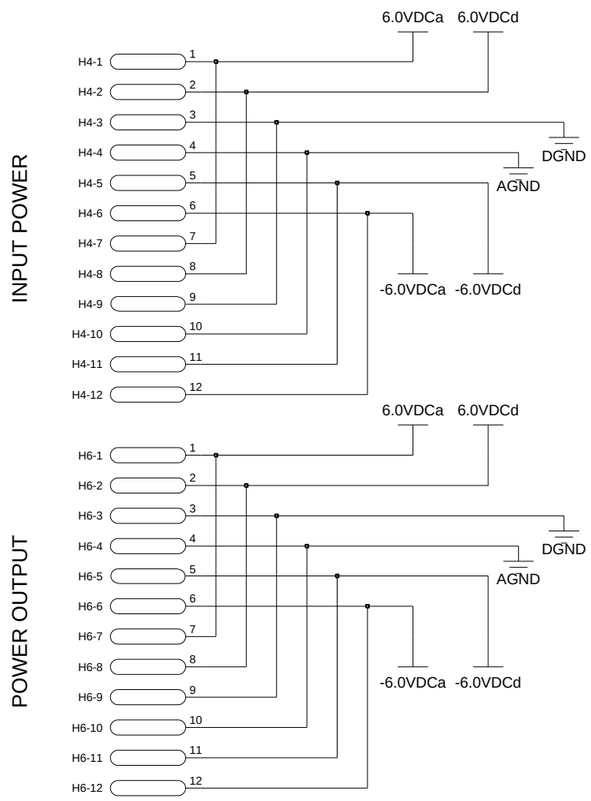
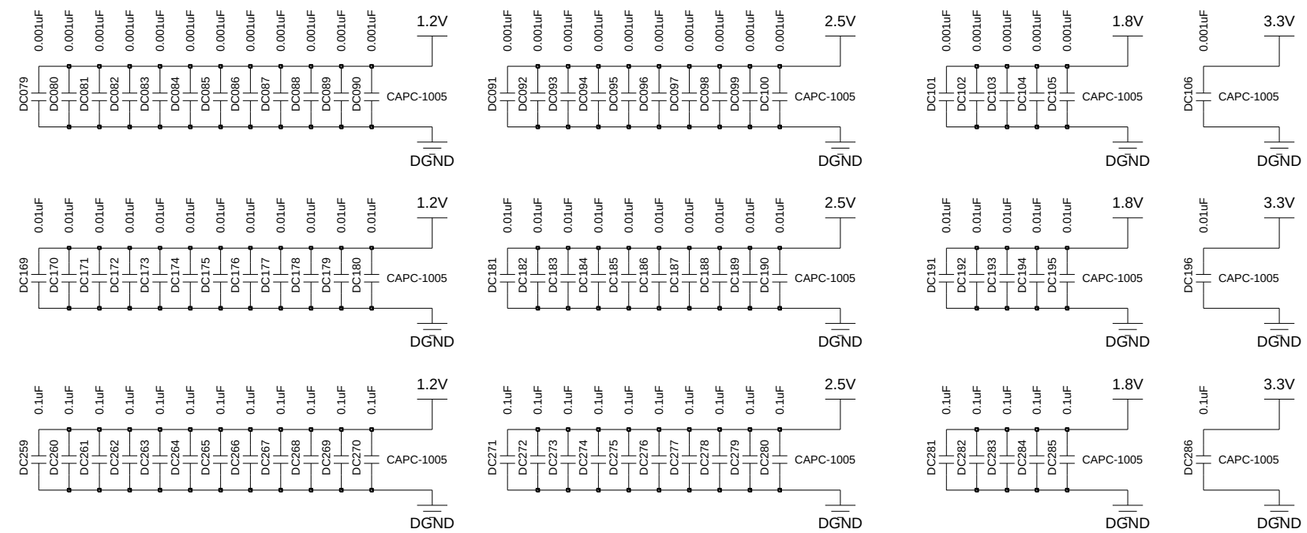
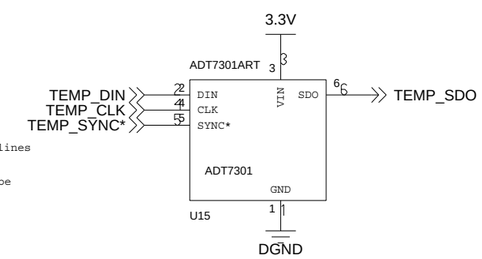
FIX Power In/Power Out vias and routing.





NOTE: There are 3 decades of capacitors for each Power pin, VCCIO, VCCINT, VCCJTAG.

THERMAL MONITORING



0.01uF Similar to Murata : GRM1555C1H102JA01D

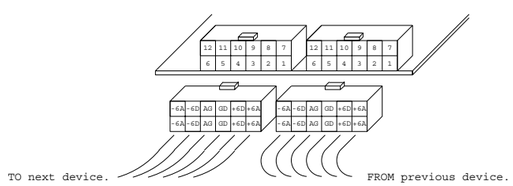
0.01uF Similar to Murata : GRM155R71E103KA01D

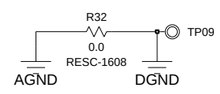
0.1uF Similar to Murata : GRM155R71C104KA88D

1.0uF Similar to Murata : GRM155R61A105KE15D

NOTE: The Dual 12 pin connector allows for redundant supply lines and greatly simplified cable construction.

In the orientation below, the header on the right can be considered INPUT. The header on the left can be considered OUTPUT.





NOTE: The _IMON signal is a 160Hz PWM signal with duty cycle proportional to supply current

NOTE: Inductors in the power supplies are either 82uH or 73uH depending on availability of components, the 'a' options are much better at noise immunity

STAC		
Power Connections, Temp Monitor, Spartan Decoupling		
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C4	J.Ameel	Tuesday, September 8, 2009
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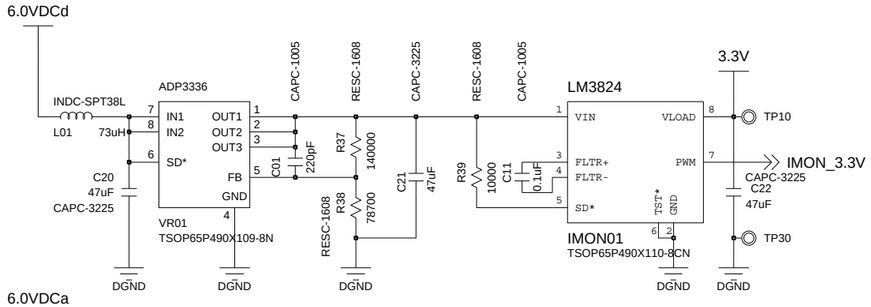
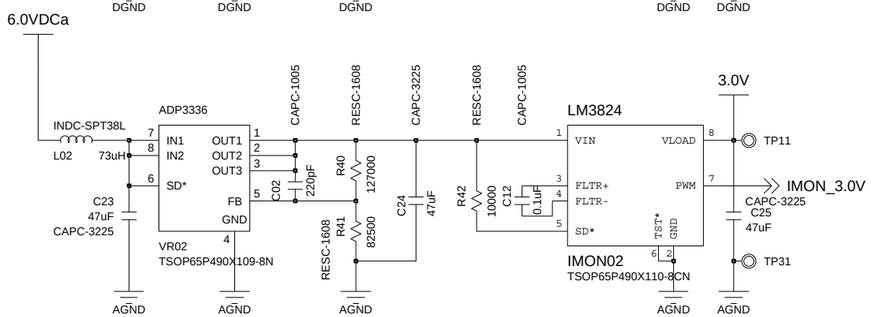
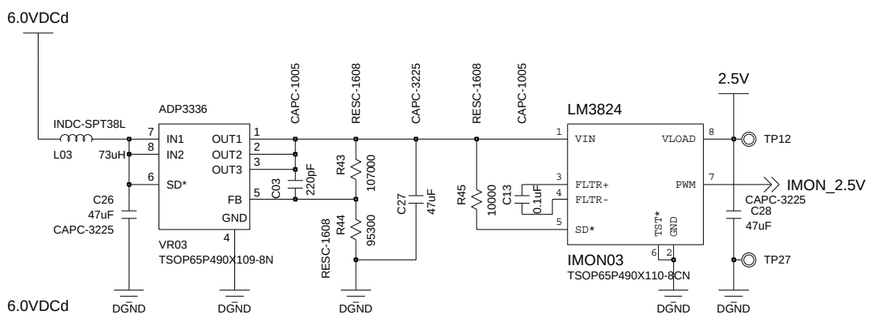
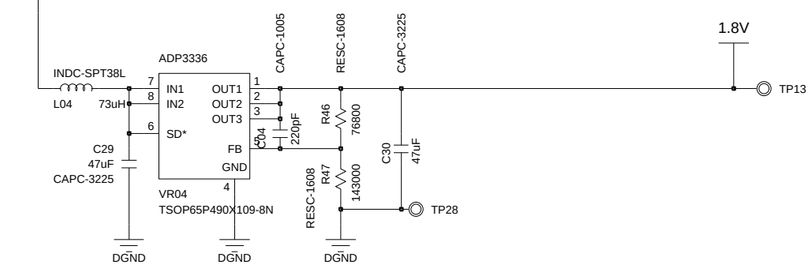


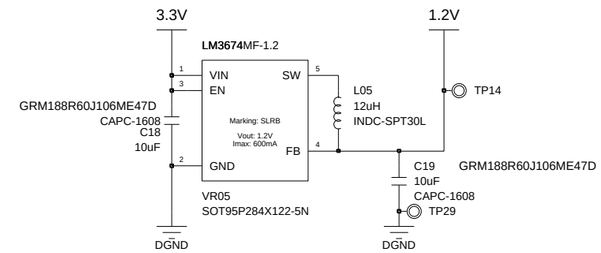






NOTE: The 1.8V power rail does not have current monitoring because the LM3824 will not function below 2.0V.

NOTE: Eliminated ability for Spartan3 to shutdown its own power rails. Prevents STAC suicide.

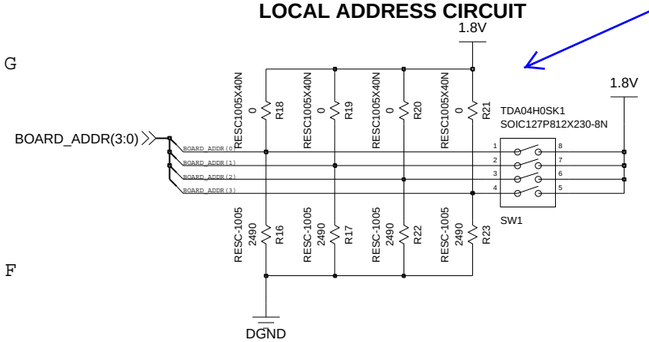


NOTE: The LM3674 requires an input voltage below 6.0V so this regulator uses the existing 3.3V rail

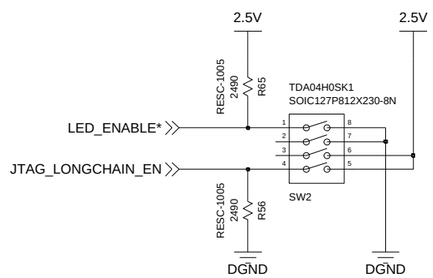
STAC		
Power Supplies and Regulators - Local Rails		
Rev	**Designed By**	**Saved Date**
C4	J.Ameel	Tuesday, September 8, 2009
		5:08:33 pm
		Sheet 12 of 13

MARK 0 ohm resistors as DO NOT INSTALL in BOM

LOCAL ADDRESS CIRCUIT

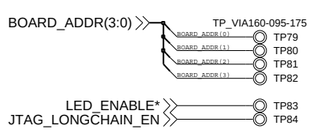


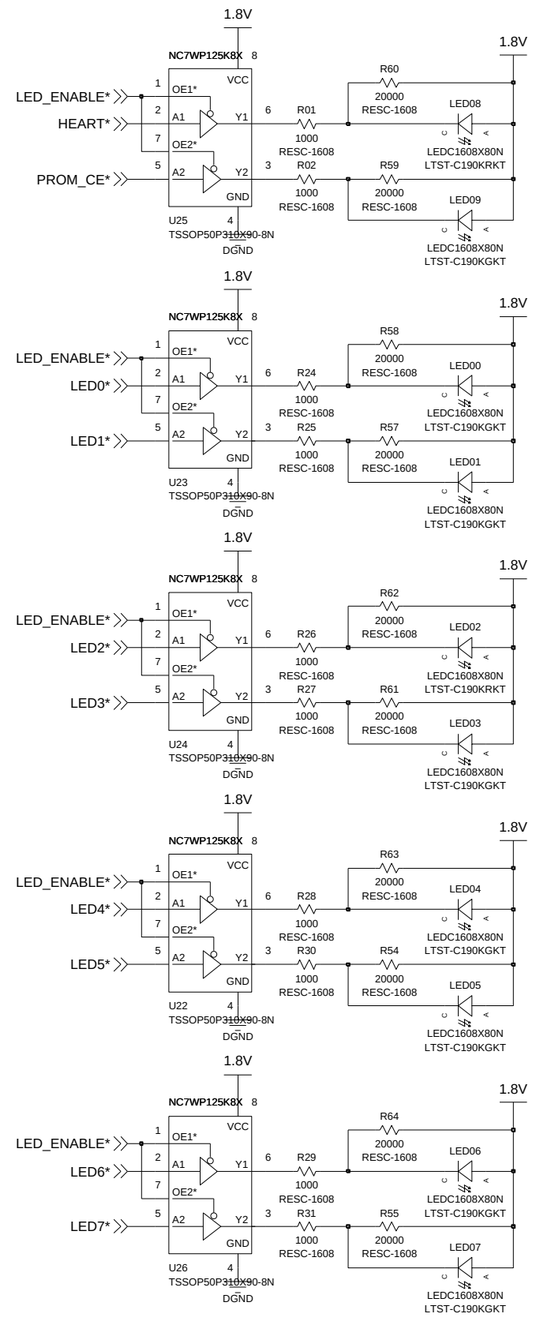
LOCAL ENABLE CIRCUIT



LED_ENABLE*
ENABLE LED indicators visible
DISABLE LED Indicators cannot light

JTAG_LONGCHAIN_EN
ENABLE JTAG TDO sourced from previous STAC
DISABLE JTAG TDO is sourced from this STAC only



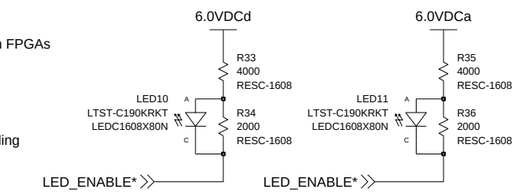


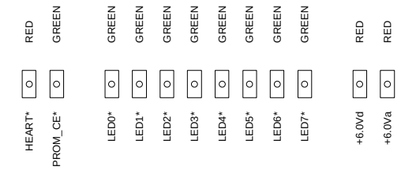
HEART*
Flashes when Spartan FPGAs are programmed.

PROM_CE*
Low during JTAG loading

Digital +6.0V Supply received

Analog +6.0V Supply received





STAC INDICATOR LEDS

13.1) Added pads for 0 ohm resistors if they are deemed necessary
13.2) Added 2 LEDs to allow for 8 custom indicators
13.3) Removed specific wording for LED meanings. allows future modification

Added JTAG long chain slideswitch
Added LED Enable slideswitch

STAC		
Indicator LEDs, local switch settings		
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C4	J.Ameel	Tuesday, September 8, 2009
		5:08:20 pm
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