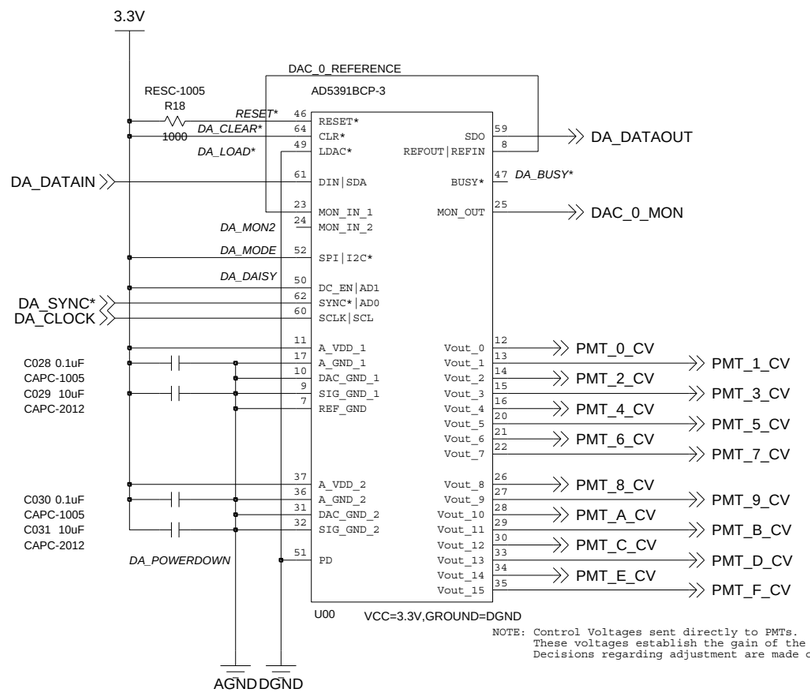
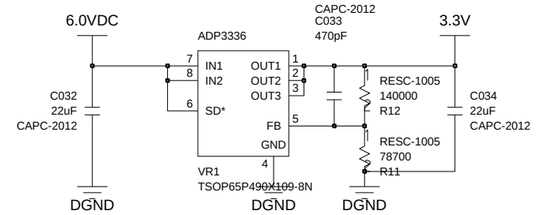
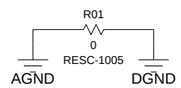


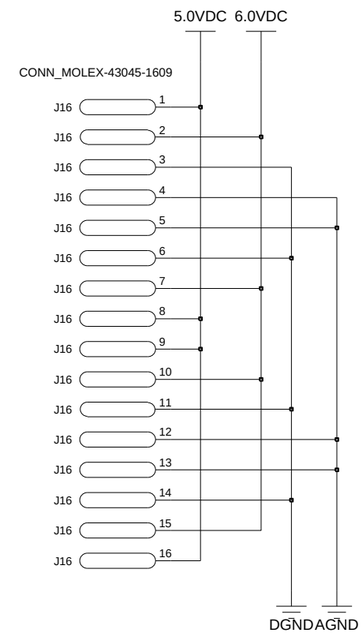
NOTE: Control Voltages sent directly to PMTs.
These voltages establish the gain of the individual tubes.
Decisions regarding adjustment are made offboard.





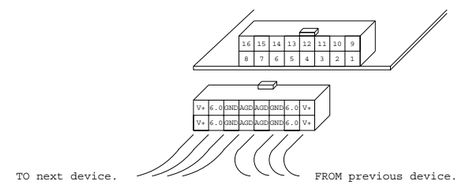
NOTE: Single point connection for analog and digital ground. This point will be realized as a single resistor connecting between internal GND and AGND layers

Also assign connection between new DGND and Rev.A's generic "Ground'

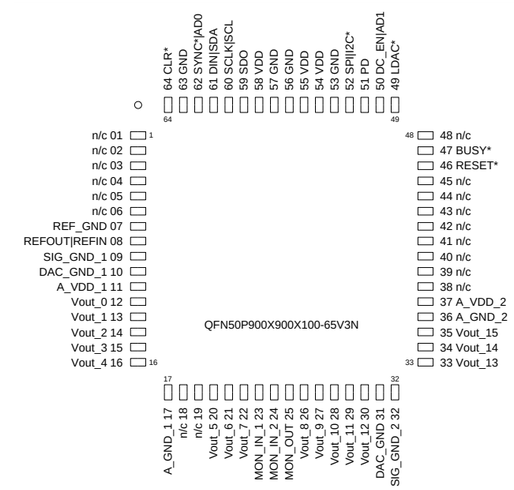


NOTE: 16pin connector allows for redundant supply lines and greatly simplified cable construction.

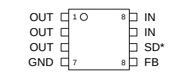
In the orientation below, pins 1..4, 9..12 can be considered INPUT. Pins 5..8 and 13..16 can be considered OUTPUT.

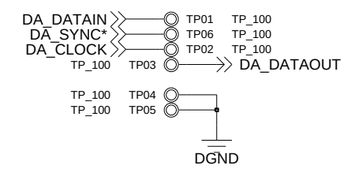


COMPONENT SPEC: AD5391BCP-3



COMPONENT SPEC: ADP3336





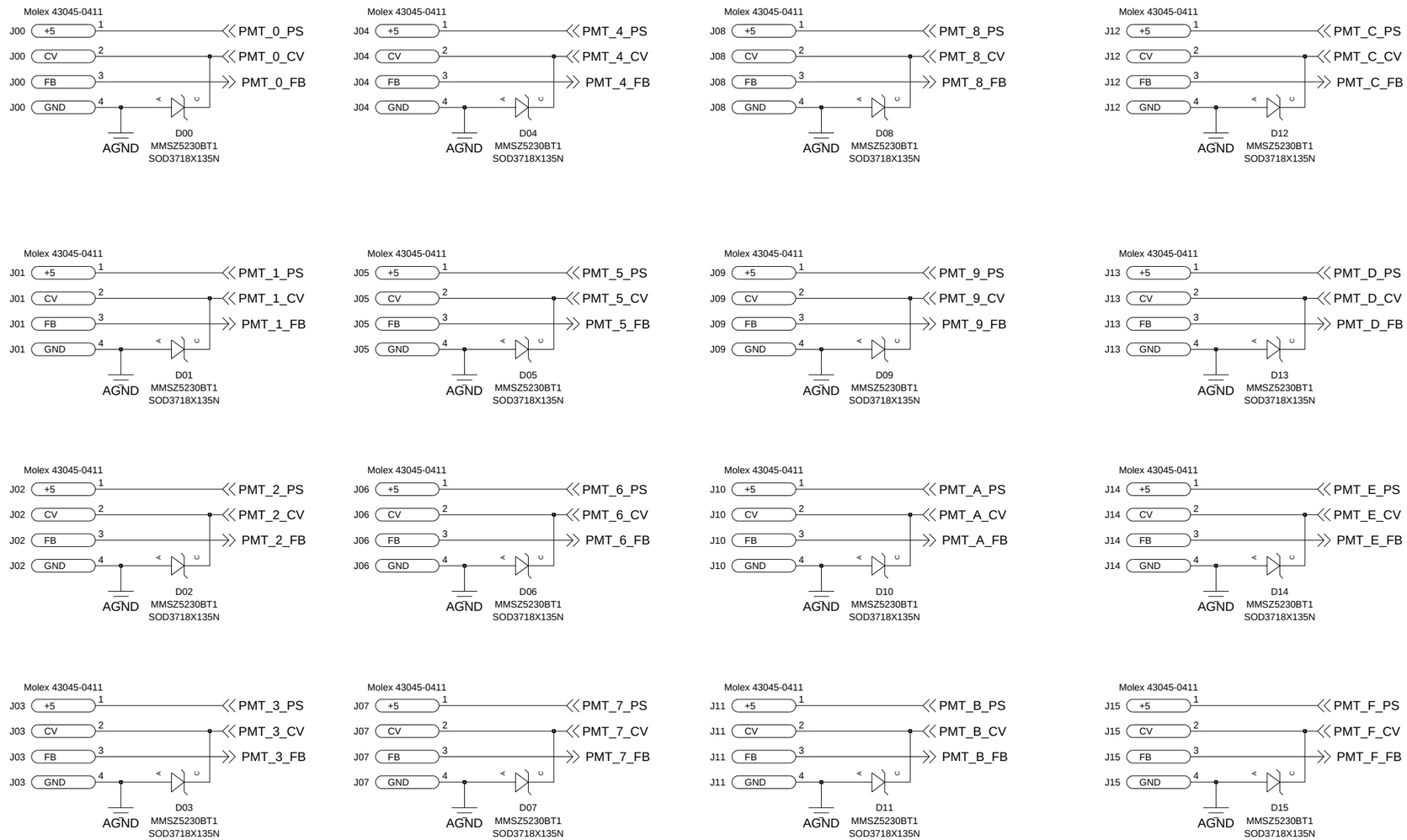
MODIFICATIONS

MOD 1.1.) 12 pin power connector replaced with 16pin 43045-1609
MOD 1.2.) ~~DAC U02 hardware disabled as there are no CT values to set Device populated to maintain MVC control software/firmware compatibility across revisions.~~
MOD 1.3.) Changed VPOS PMT Supply rail to 5.0VDC to avoid confusion
MOD 1.4.) Renumbered references to match new designs.
MOD 1.5.) Capacitor geometries set to 2012 (EIA 0805) across design
MOD 1.6.) Removed hardware RESET* signal. Reset now handled by software only
MOD 1.7.) Removed DAC U02.
Moved DA_DATAOUT from U02 to U01-59

Sedecim Voltage Interpreter

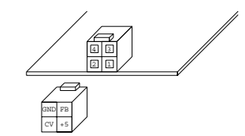
Digital to Analog Conversion and Power Supply

Rev	Designed By	Saved Date
B.2	Jon Ameel	Tuesday, June 30, 2009
		4:23:33 pm
		Sheet 01 of 07



COMPONENT SPEC: 43045-0411

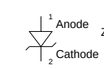
NOTE: GND and PMT feedback are accessible on upper pair. Control and Supply voltages are the lower pair



COMPONENT SPEC: MMSZ5230BT1

SOD3718X135N

Zener Diode D0 through D15



ZenerVoltage:4.7V

NOTE: Components D0..D15 are Zener diodes with a reverse bias voltage of 4.7V and a 500mW rating.
D0..D15 similar to OnSemiconductor : MMSZ5230BT1

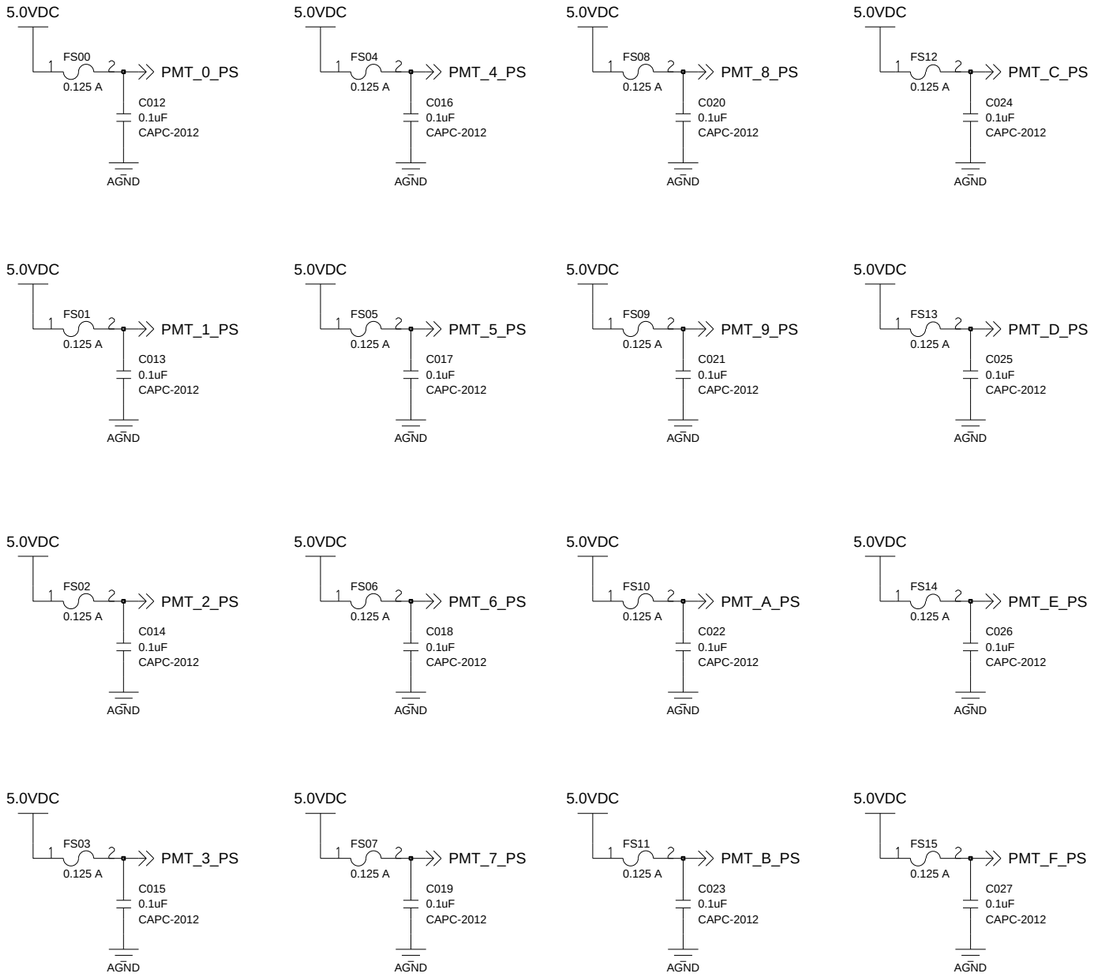
MODIFICATIONS

MOD 2.1.) 4 pin PMT connector replaced with entirely SMT version
MOD 2.2.) Zener diode D00..D15 obsolete, replaced with current version
MOD 2.3.) ~~Added parallel 0.1uF capacitance between PMT_x_FB and Ground~~ Removed in favor of Mod 2.5.)
MOD 2.4.) Renumbered references to match new designs.
MOD 2.5.) Added Op amp follower for PMT_x_FB

Sedecim Voltage Interpreter

PMT Interface and zener protection

Rev	Designed By	Saved Date
B.2	Jon Ameel	Tuesday, June 30, 2009
		4:23:52 pm
		Sheet 02 of 07



MODIFICATIONS

MOD 3.)	Changed VPOS PMT Supply rail to 5.0VDC to avoid confusion
MOD 4.)	Renumbered references to match new designs.
MOD 5.)	Capacitor geometries set to 2012 (EIA 0805) across design
MOD 9.)	Replaced LM3822 current monitors with 0466.125NR circuit protector Removed associated circuitry for LM3822 Added parallel capacitance on both sides of circuit protector.
MOD 10.)	Added parallel 0.1uF capacitance between PMT_x_SV and Ground
MOD 11.)	Removed PWM to V conversion circuit as there is no PWM signal generated

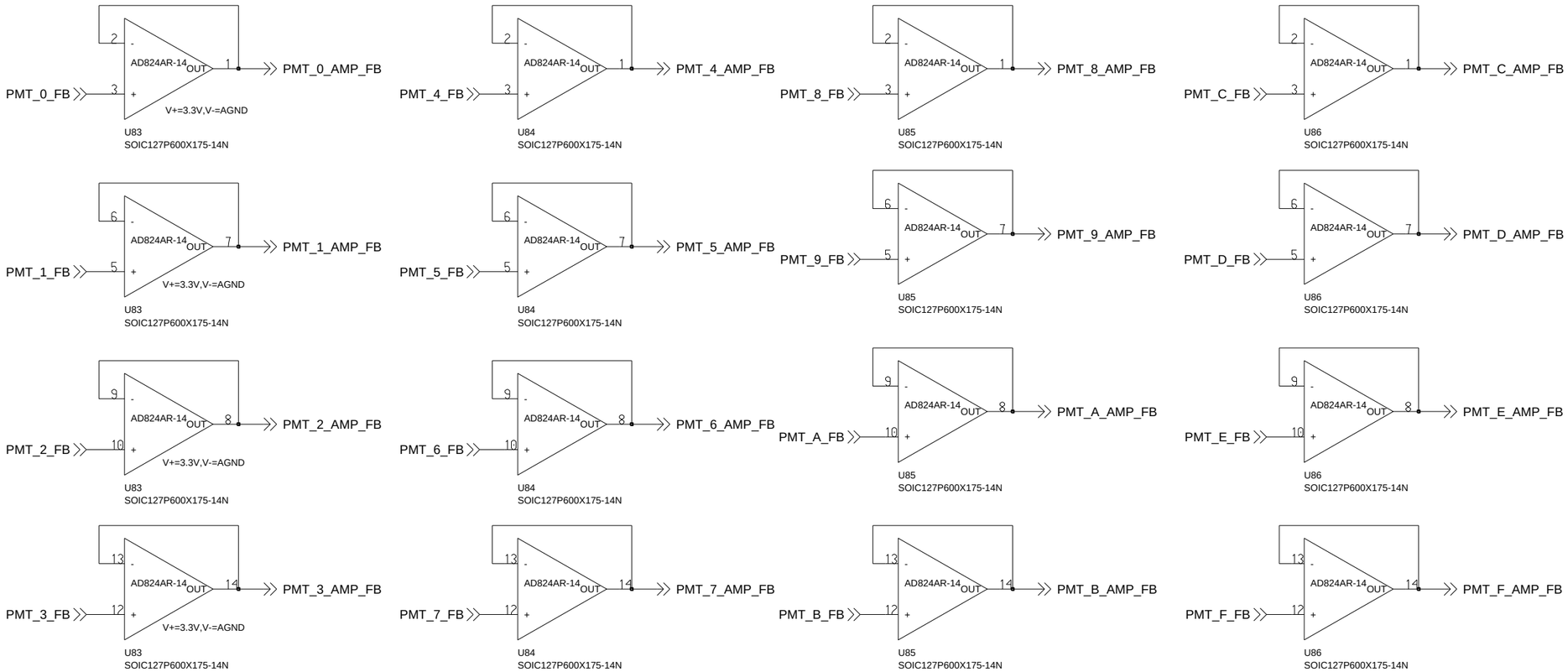
NOTE:
Circuit protection device is as follows:

Part #	0466.125NR
Manufacturer	Littelfuse
geometry	RESC-3216

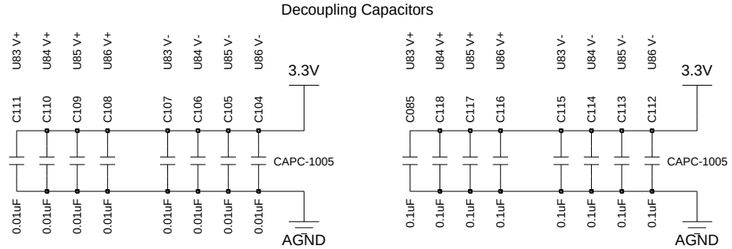
Sedecim Voltage Interpreter

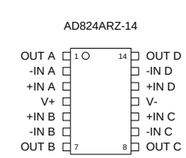
PMT OverCurrent Protection and Supply Voltage dividers.

Rev	Designed By	Saved Date
B	Jon Ameel	Tuesday, June 30, 2009
		4:24:18 pm
		Sheet 03 of 07

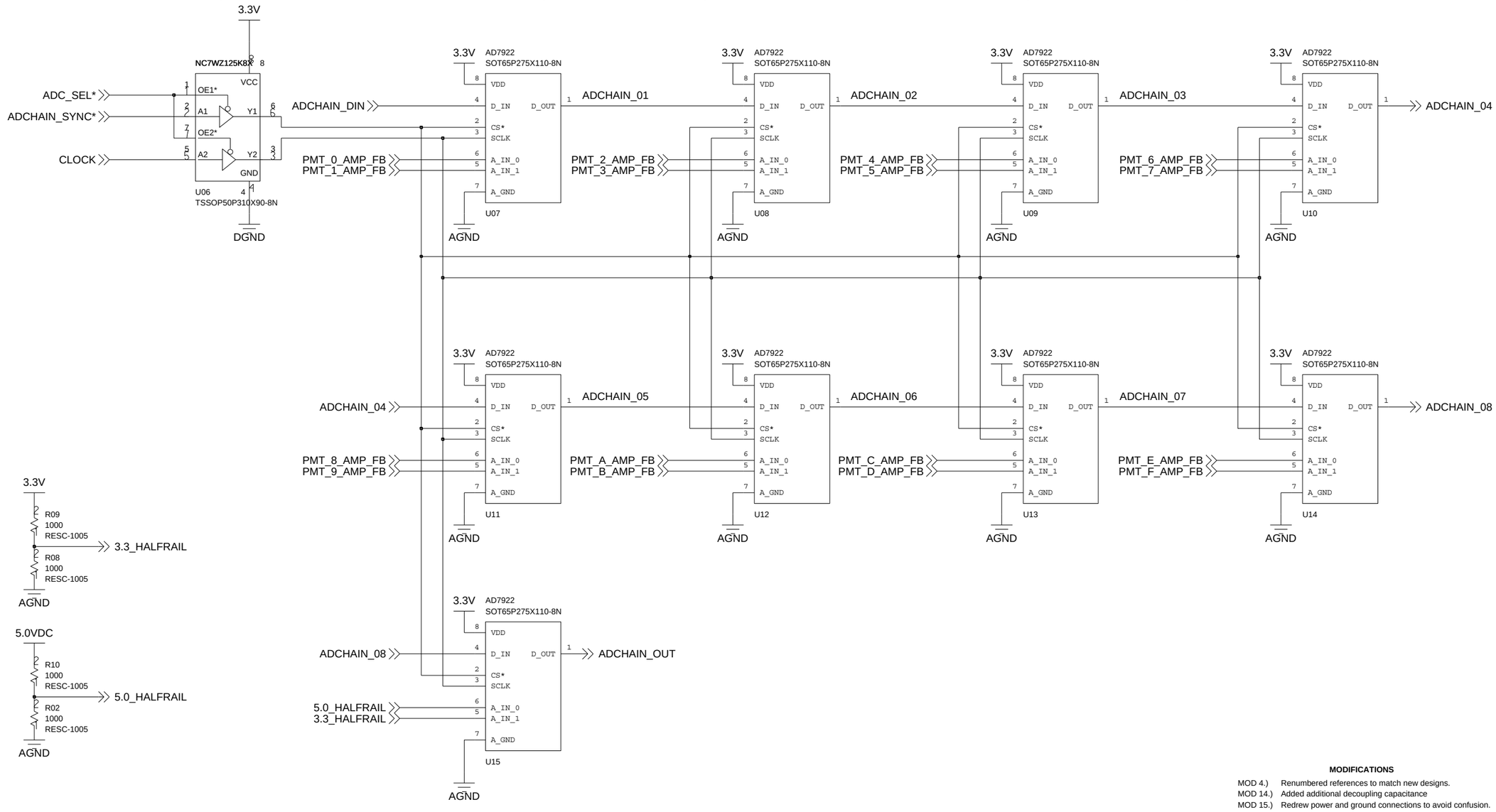


Decoupling Capacitors



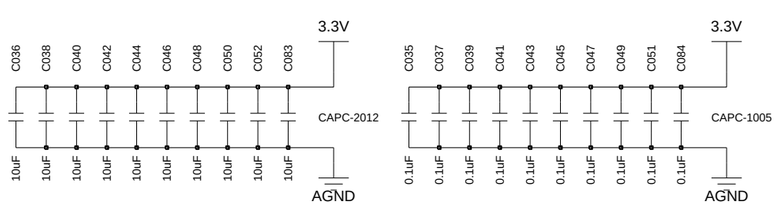


Sedecim voltage Interpreter		
PMT Feedback (High Z) Voltage Follower		
Rev	**Designed By**	**Saved Date**
B	Jon Ameel	Tuesday, June 30, 2009
		4:24:39 pm
		Sheet 04 of 07

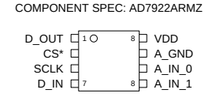


MODIFICATIONS

MOD 4.) Renumbered references to match new designs.
MOD 14.) Added additional decoupling capacitance
MOD 15.) Redrew power and ground connections to avoid confusion.



COMPONENT SPEC: AD7922ARMZ

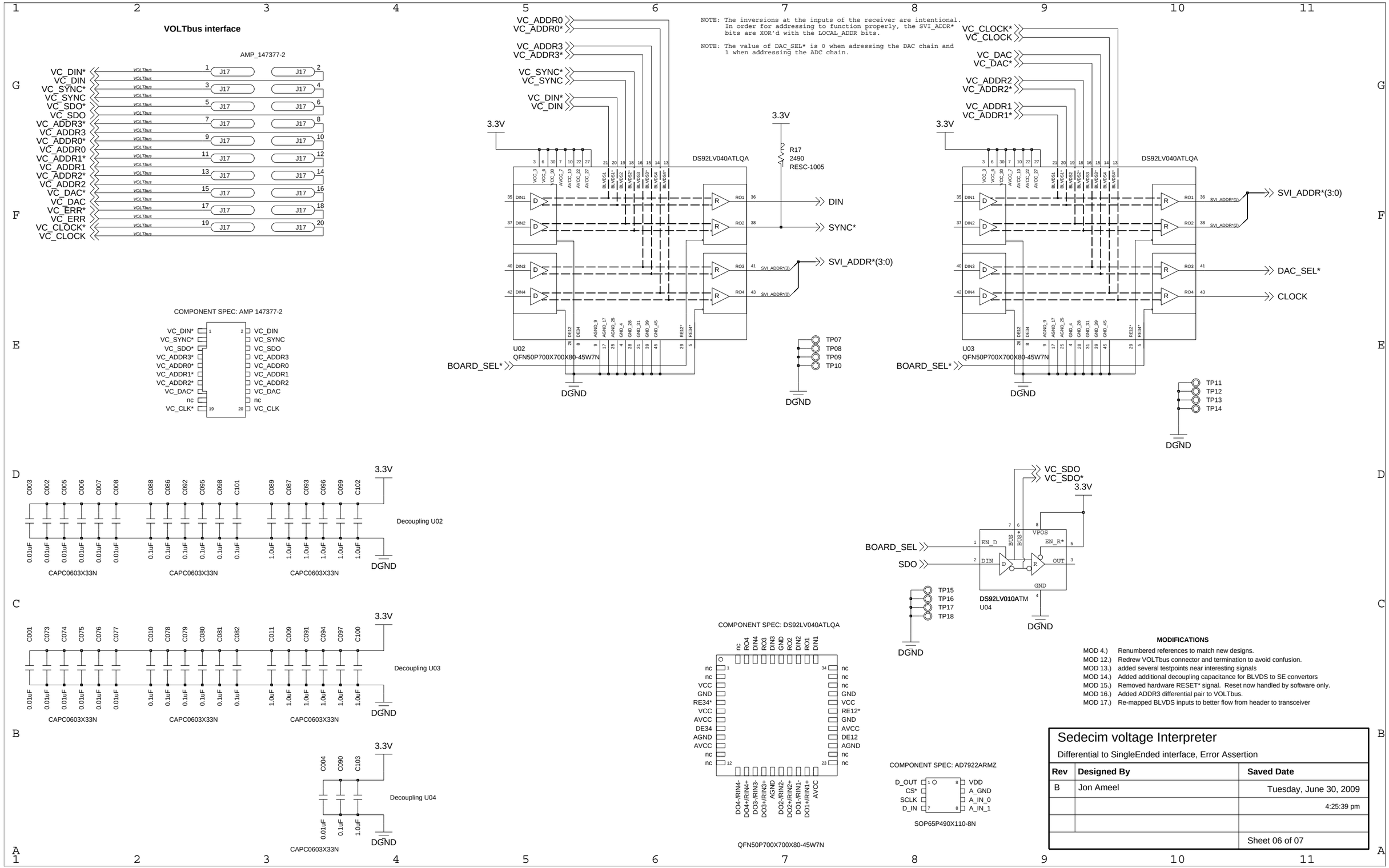


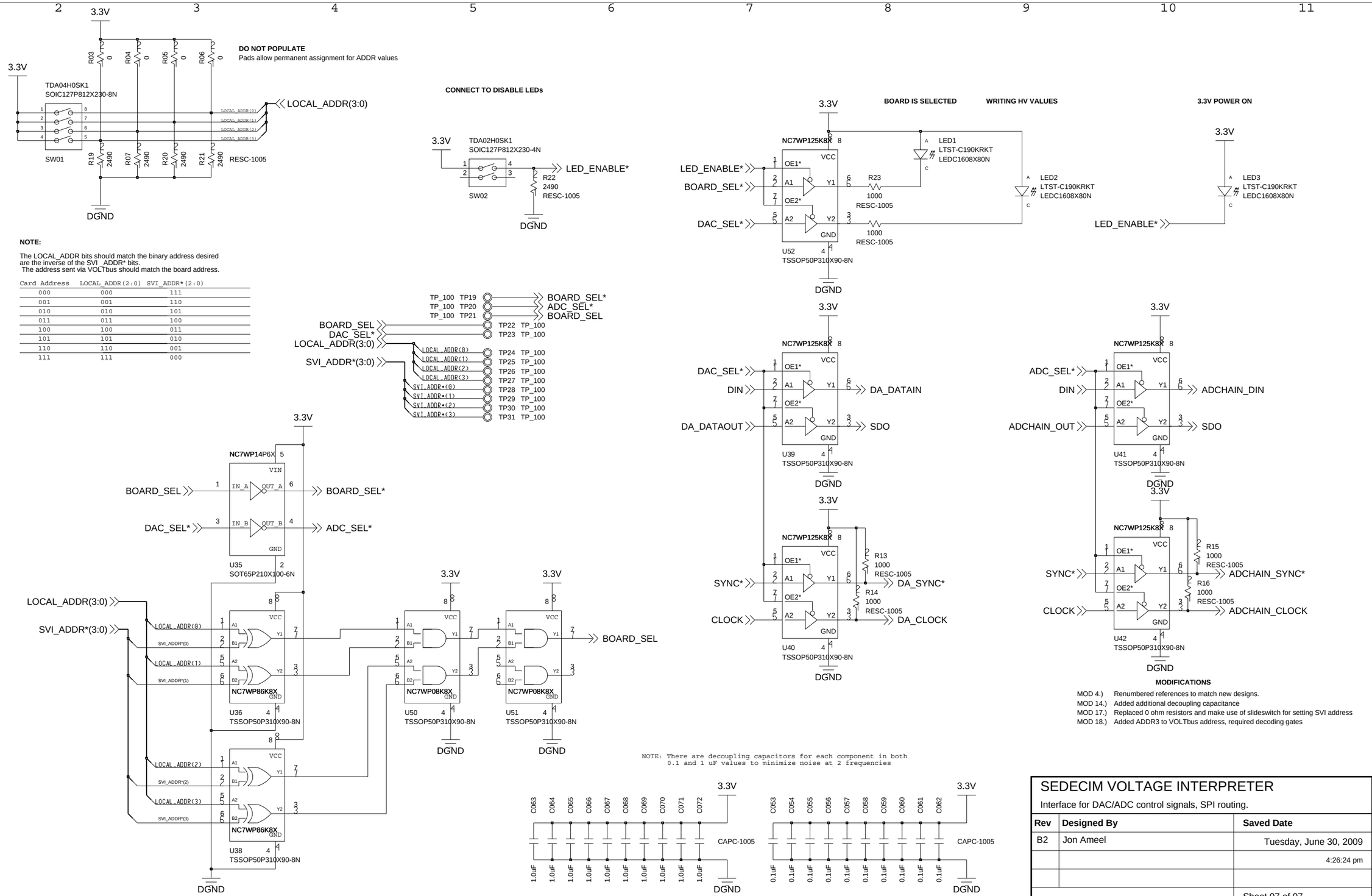
SOP65P490X110-8N

Sedecim Voltage Interpreter

PMT ADC Chain : Cockroff/Walton Feedback

Rev	Designed By	Saved Date
B	Jon Ameel	Tuesday, June 30, 2009
		4:25:16 pm
		Sheet 05 of 07


VOLTbus interface
AMP_147377-2
VC_DIN*
VC_DIN
VC_SYNC*
VC_SYNC
VC_SDO*
VC_SDO
VC_ADDR3*
VC_ADDR3
VC_ADDR0*
VC_ADDR0
VC_ADDR1*
VC_ADDR1
VC_ADDR2*
VC_ADDR2
VC_DAC*
VC_DAC
VC_ERR*
VC_ERR
VC_CLOCK*
VC_CLOCK
VOLTbus
J17
COMPONENT SPEC: AMP 147377-2
nc
NOTE: The inversions at the inputs of the receiver are intentional. In order for addressing to function properly, the SVI_ADDR* bits are XOR'd with the LOCAL_ADDR bits.
NOTE: The value of DAC_SEL* is 0 when adressing the DAC chain and 1 when addressing the ADC chain.
3.3V
DS92LV040ATLQA
R17
2490
RESC-1005
DIN
SYNC*
SVI_ADDR*(3:0)
SVI_ADDR*(1)
SVI_ADDR*(2)
DAC_SEL*
CLOCK
U02
U03
QFN50P700X700X80-45W7N
BOARD_SEL*
DGND
TP07
TP08
TP09
TP10
TP11
TP12
TP13
TP14
Decoupling U02
Decoupling U03
Decoupling U04
CAPC0603X33N
VC_SDO
VC_SDO*
BOARD_SEL
SDO
TP15
TP16
TP17
TP18
DS92LV010ATM
U04
COMPONENT SPEC: DS92LV040ATLQA
COMPONENT SPEC: AD7922ARMZ
SOP65P490X110-8N
MODIFICATIONS
MOD 4.) Renumbered references to match new designs.
MOD 12.) Redrew VOLTbus connector and termination to avoid confusion.
MOD 13.) added several testpoints near interesting signals
MOD 14.) Added additional decoupling capacitance for BLVDS to SE convertors
MOD 15.) Removed hardware RESET* signal. Reset now handled by software only.
MOD 16.) Added ADDR3 differential pair to VOLTbus.
MOD 17.) Re-mapped BLVDS inputs to better flow from header to transceiver
Sedecim voltage Interpreter
Differential to SingleEnded interface, Error Assertion
Rev
Designed By
Saved Date
B
Jon Ameel
Tuesday, June 30, 2009
4:25:39 pm
Sheet 06 of 07



NOTE:

The LOCAL_ADDR bits should match the binary address desired are the inverse of the SVI_ADDR* bits.
The address sent via VOLTbus should match the board address.

Card Address	LOCAL_ADDR(2:0)	SVI_ADDR*(2:0)
000	000	111
001	001	110
010	010	101
011	011	100
100	100	011
101	101	010
110	110	001
111	111	000

MODIFICATIONS

MOD 4.) Renumbered references to match new designs.
MOD 14.) Added additional decoupling capacitance
MOD 17.) Replaced 0 ohm resistors and make use of slideswitch for setting SVI address
MOD 18.) Added ADDR3 to VOLTbus address, required decoding gates

SEDECIM VOLTAGE INTERPRETER

Interface for DAC/ADC control signals, SPI routing.

Rev	Designed By	Saved Date
B2	Jon Ameel	Tuesday, June 30, 2009
		4:26:24 pm
		Sheet 07 of 07