Bill, Eric, Frank, Ray, Ron
May 21 2004

"Current" Status of the TDC Readout

Many changes were proposed as far back as May 21 2003

Finally implemented by March 20 2004

→ *Balanced data load in VRB crates*

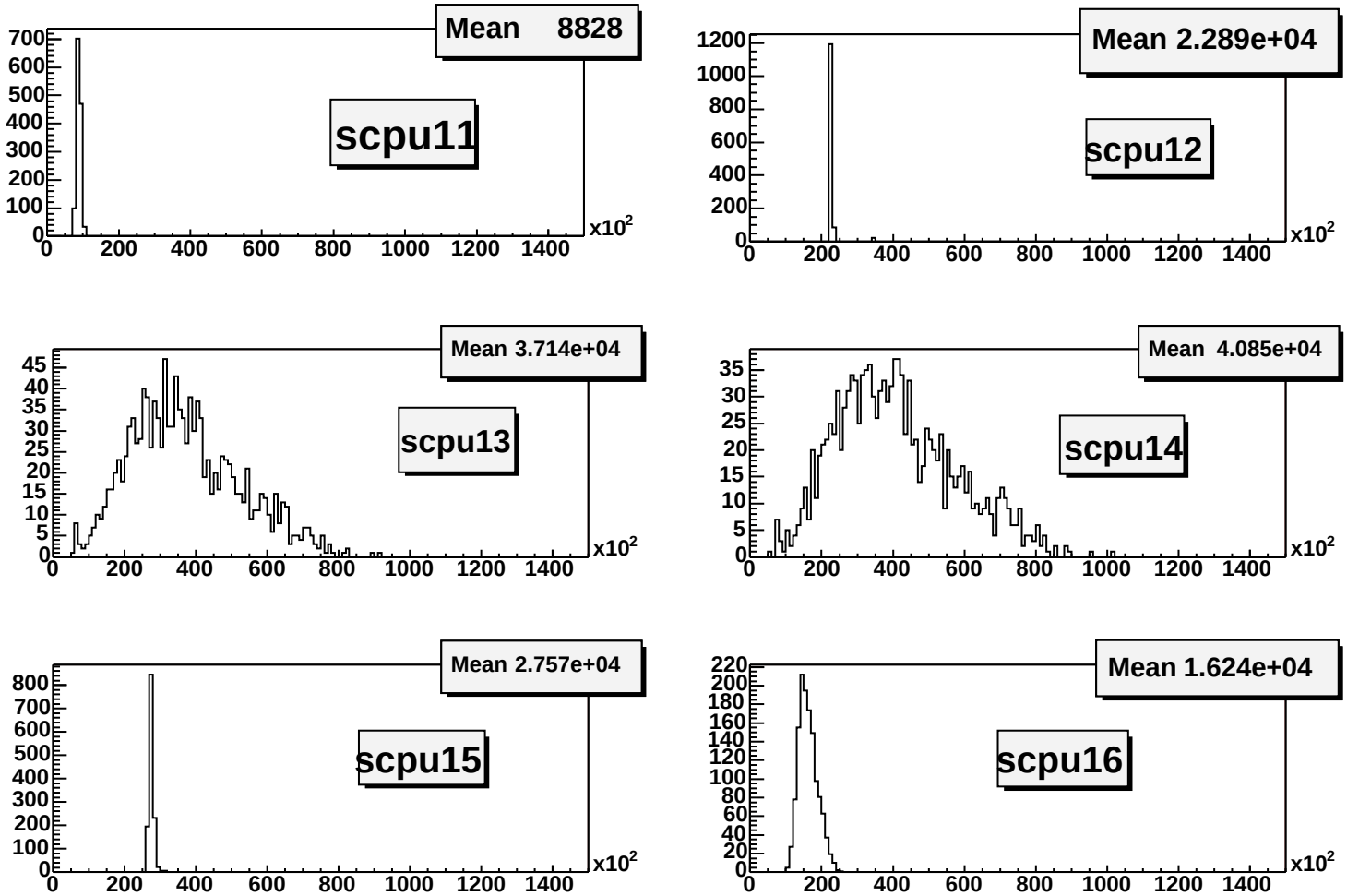
→ *Faster processors*

→ *Improved DSP code*

→ *Changes to data format*

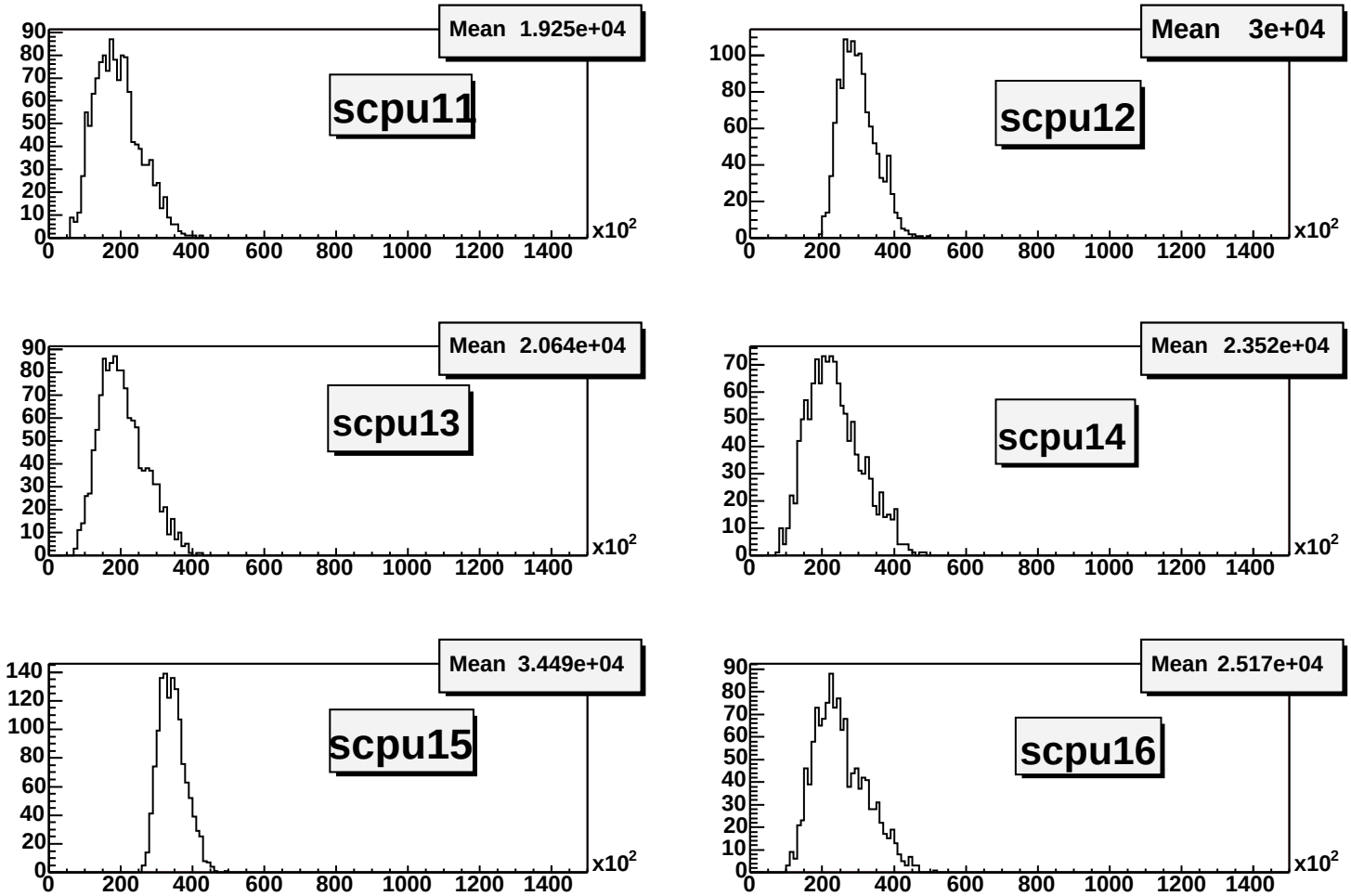
→ *Optimized readout code*

Data from the COT crates were being concentrated in two VRB crates (SCPU13, SCPU14)

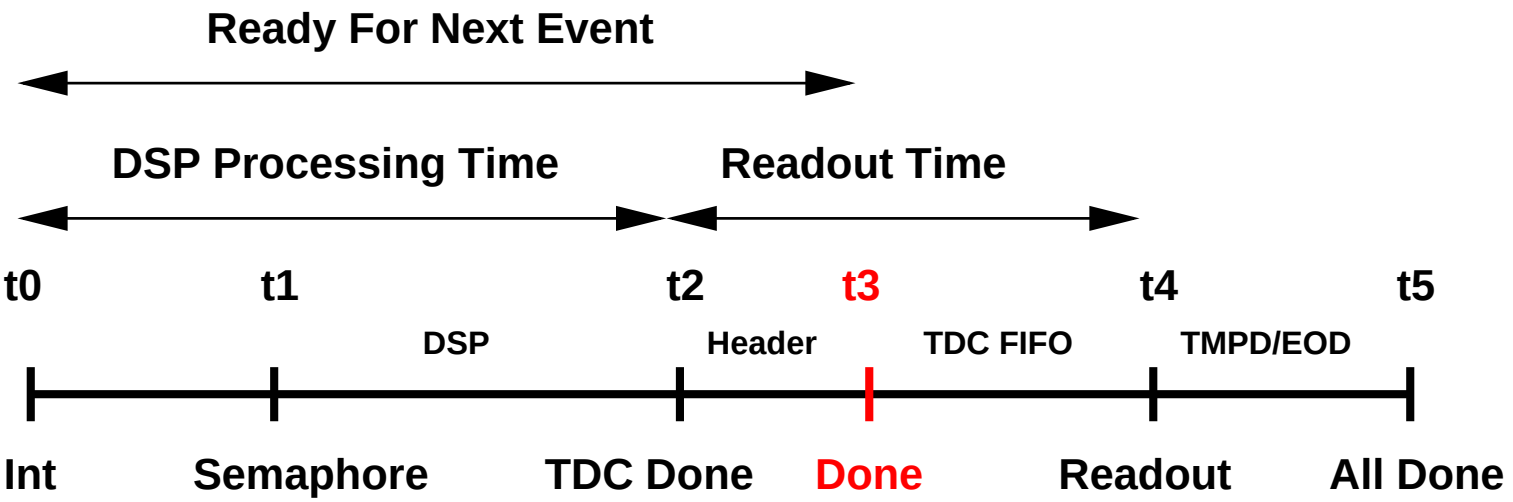


As the occupancy went up we saw that we were limited by the EVB readout

Rebalanced the data load across the VRB crates



Timing information is stored for each event in the TMPD bank

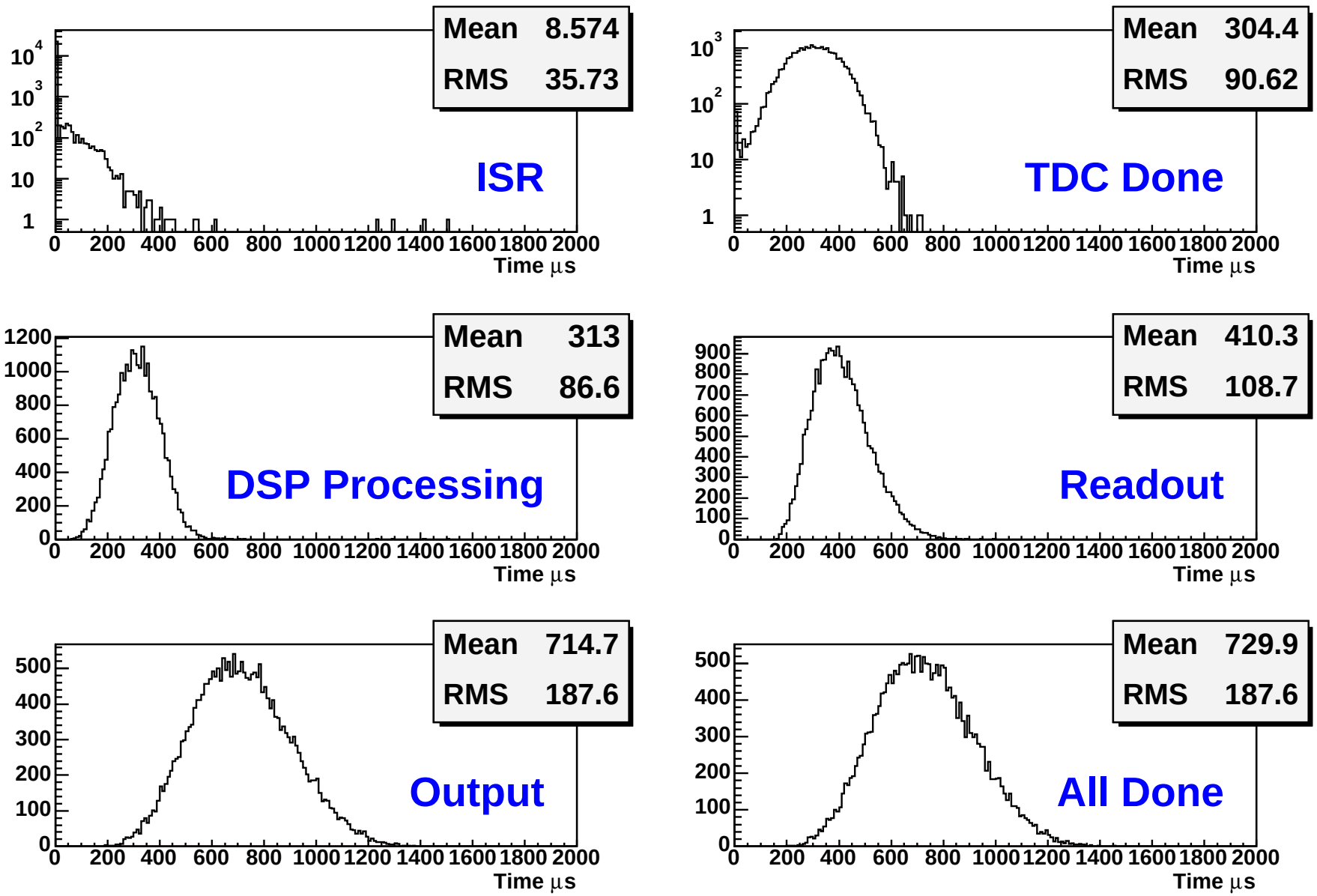


In order to get a unbiased look at the data, selected events from the L3 Monitor path

Ran over the "d stream" and used the prereq module:

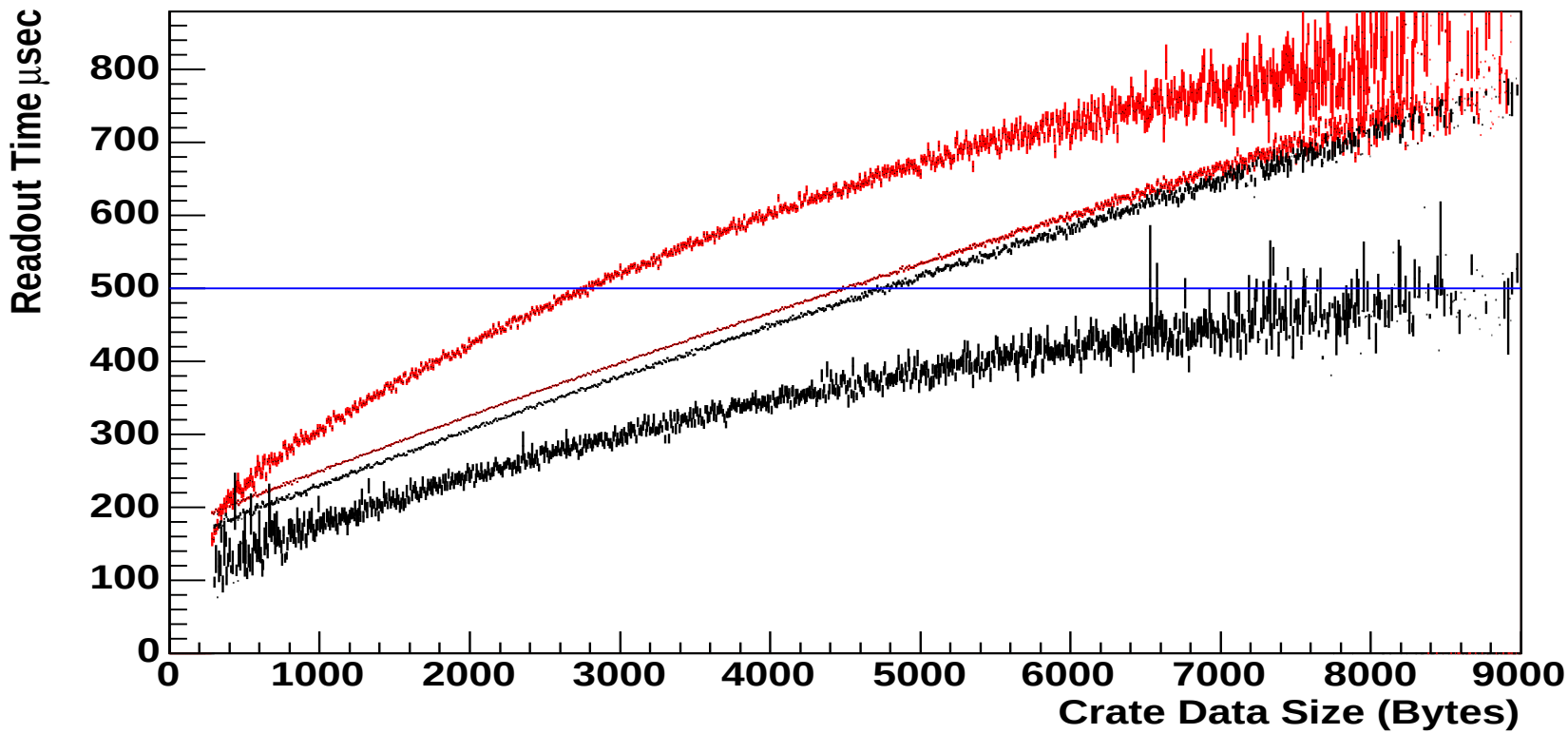
```
L3TriggerNames    set MONITOR_L3TAG
```

→ Recently added a new measurement point (Tracer Done Set)


Mean 8.574
RMS 35.73
ISR
Time μs
Mean 304.4
RMS 90.62
TDC Done
Time μs
Mean 313
RMS 86.6
DSP Processing
Time μs
Mean 410.3
RMS 108.7
Readout
Time μs
Mean 714.7
RMS 187.6
Output
Time μs
Mean 729.9
RMS 187.6
All Done
Time μs

The Tracer Done is set before the TDCs are readout

→ The maximum of Readout Time or DSP processing time limits our readout



Red: Old DSP version

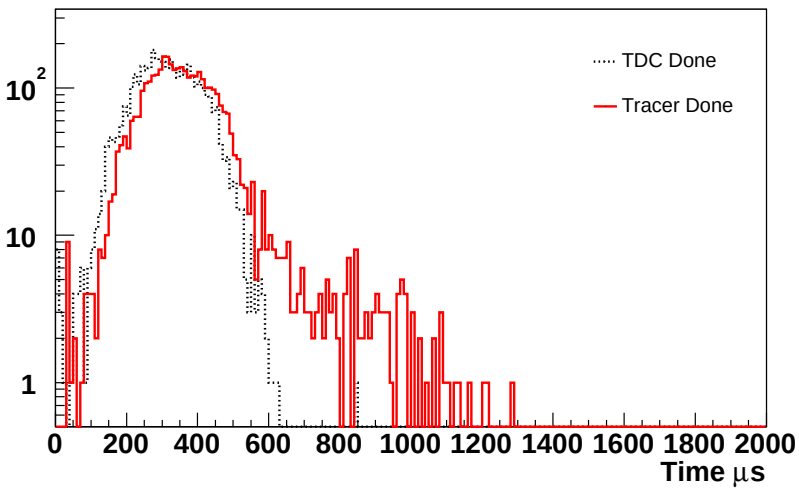
Black: V45 of the DSP code

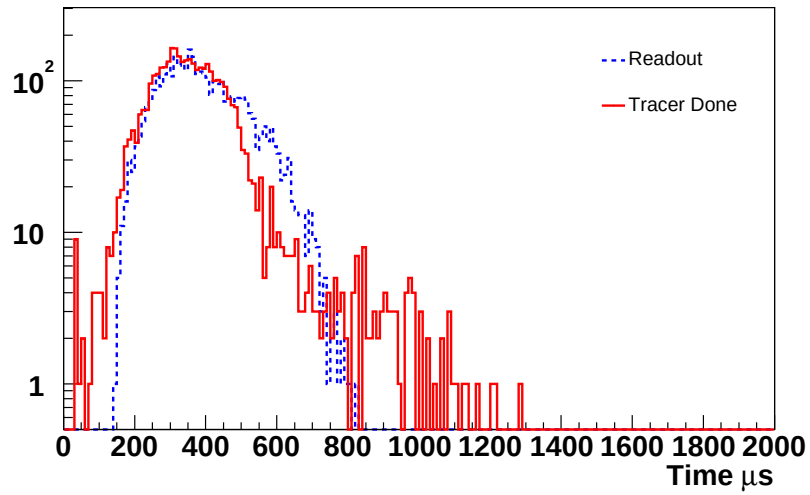
Ron has some ideas to reduce the data volume by 1/3

Recently added Time to Set TRACER Done

After the TDCs are done we need to readout the TDC header before setting the TRACER Done

Once the TRACER Done is set the Trigger supervisor is ready to issue the next decision

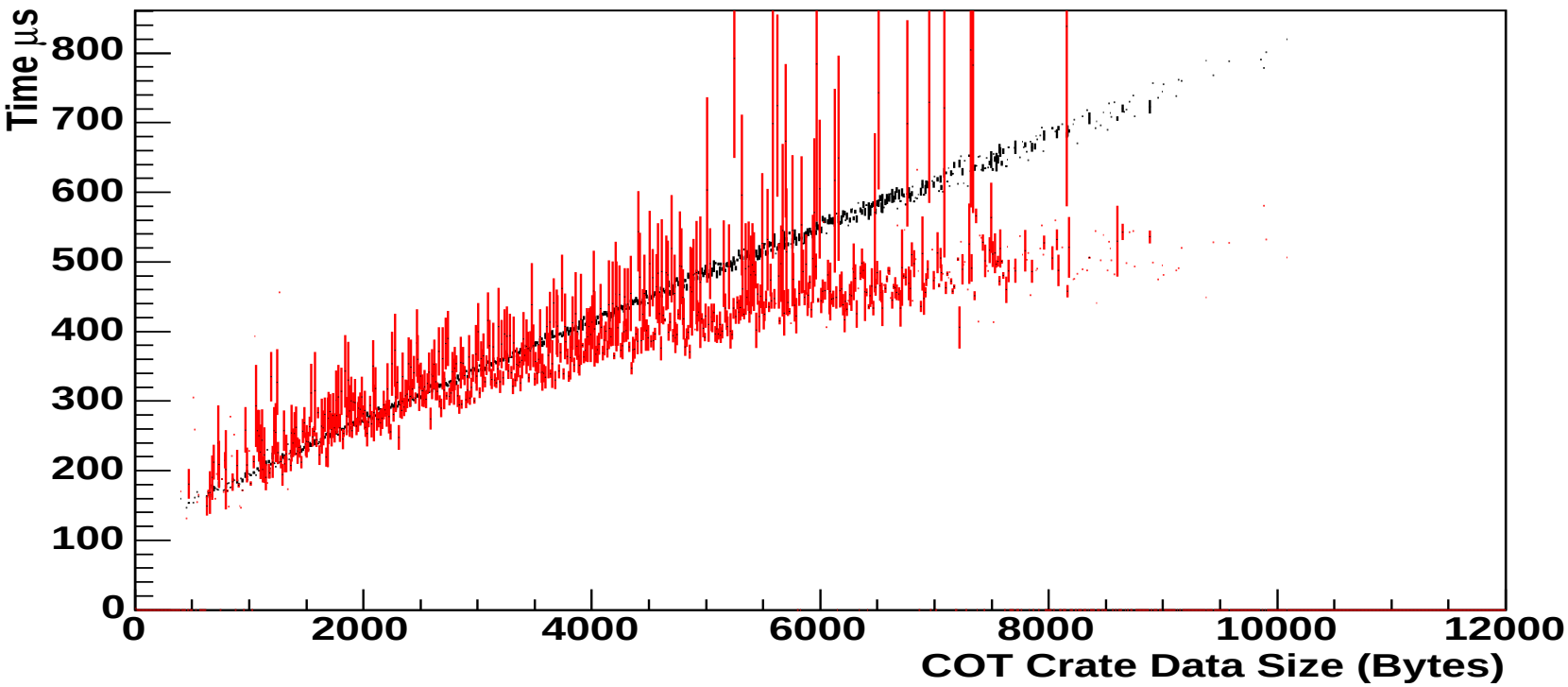




The time to set the TRACER Done is less than the readout time

Need to understand tail (context switch, FADC...)

Time to set TRACER done is comparable to the readout time



Readout time grows faster that the *Time to Set TRACER Done*

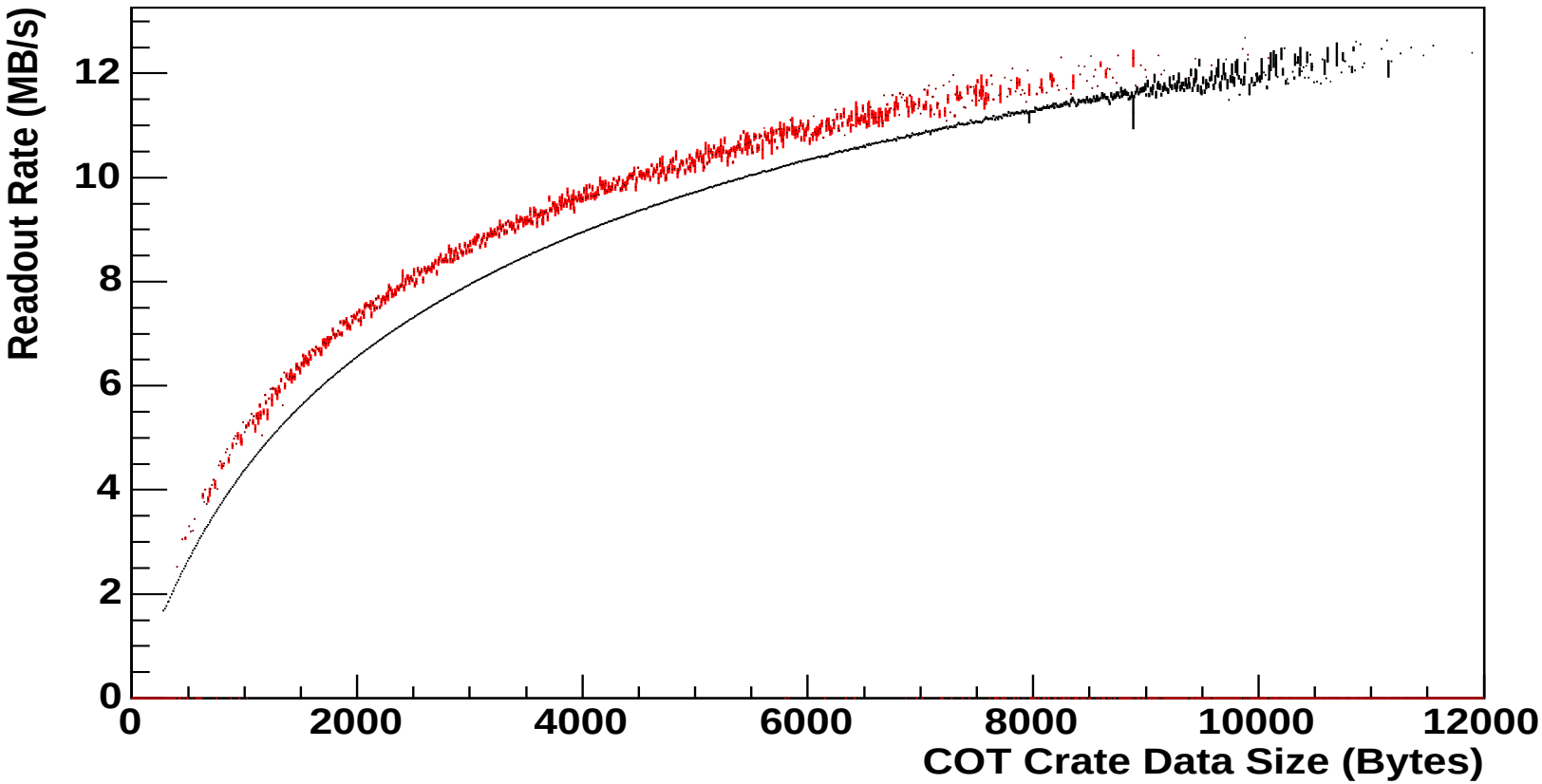
→ See some tails that need to be understood...

→ Only have limited statistics...

Reduced time to readout the TDC headers from

53-67 $\rightarrow$ 26-28 μs

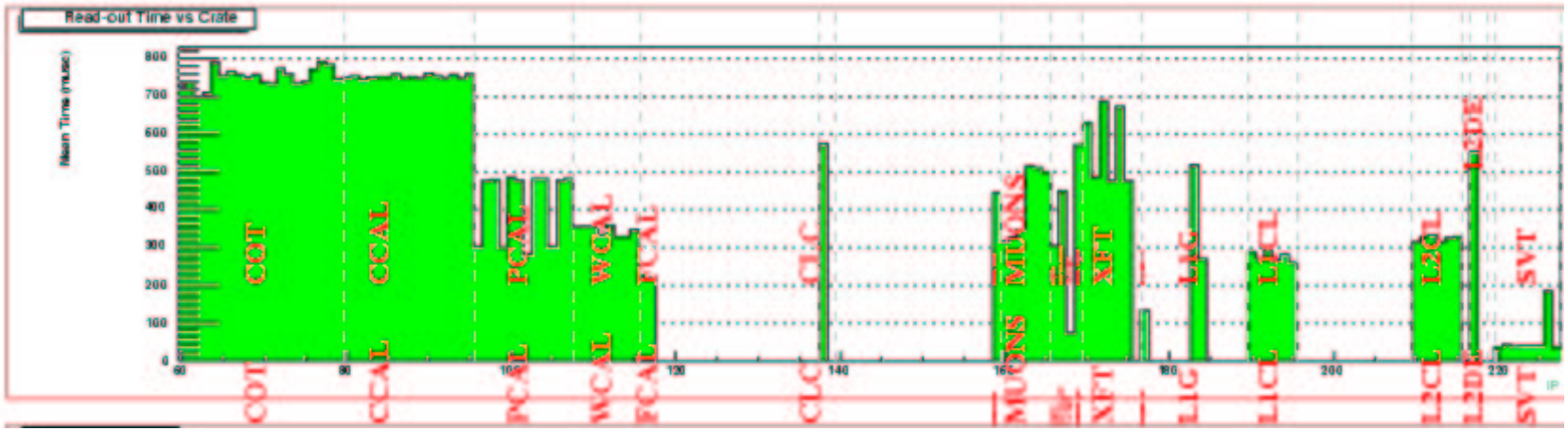
Need to readout headers before setting the TRACER Done



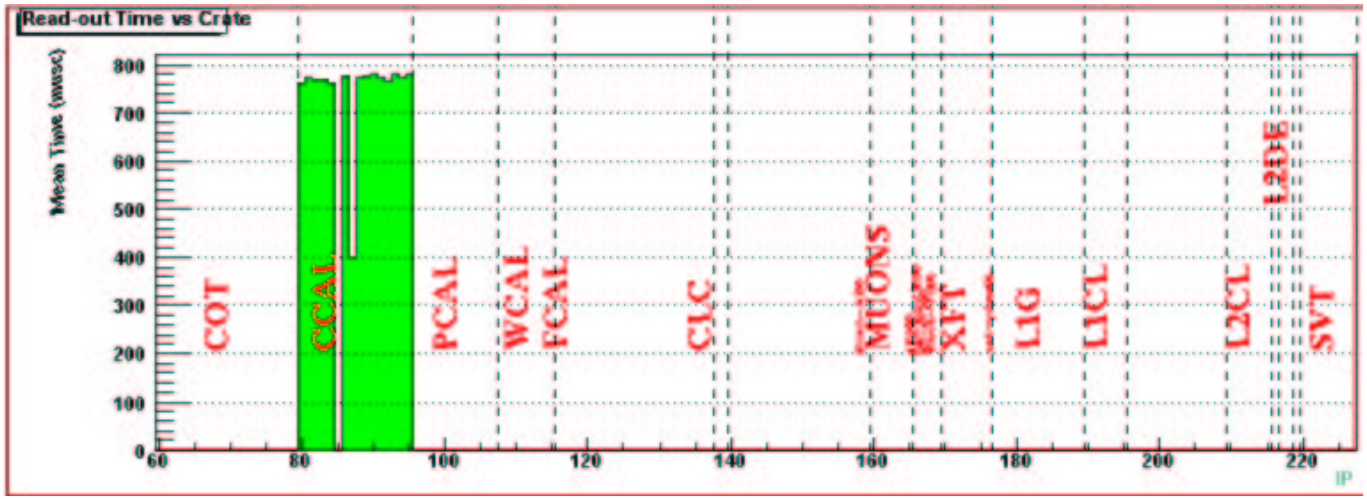
Every little bit helps...

COT readout latencies are now comparable to the CCAL

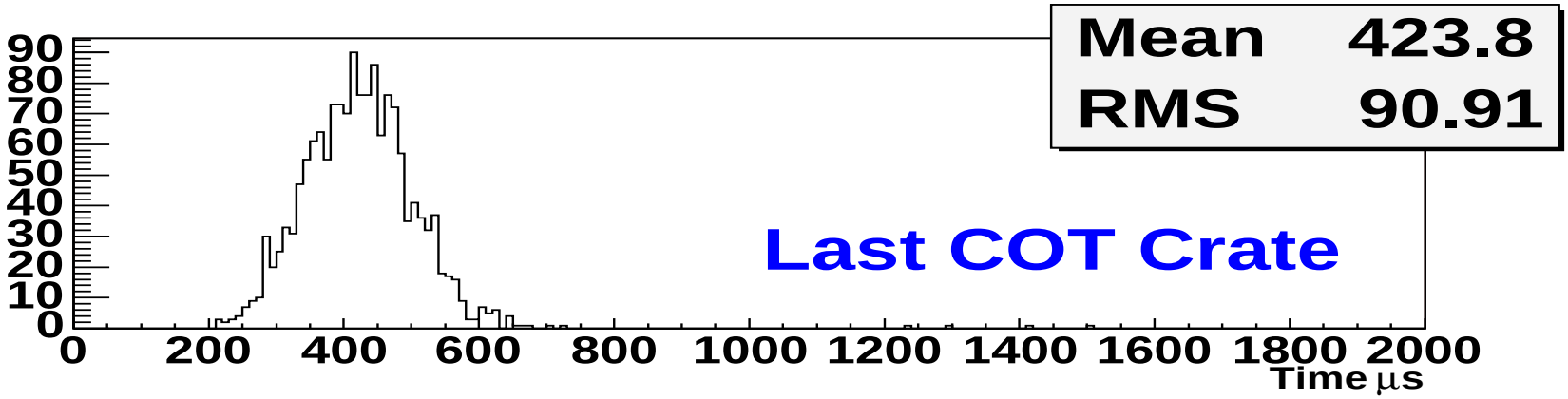
Run 182873 LStart = 60 E30 LStop = 52 E30

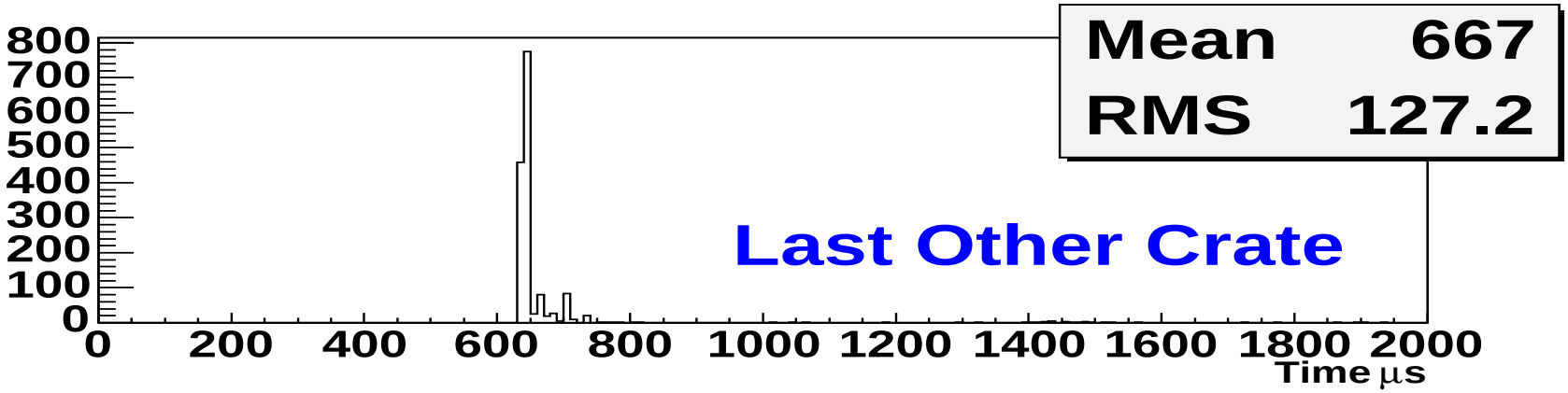


Will move the MVME2400 from the COT crates to the CCAL crates



Next slowest crate





XFT02 shows up most often and the next slowest crate, but not so bad.

Readout for other systems is under control...

DAQ Performance

Actual performance may vary....

Need to better characterize the performance of the overall system running under realistic conditions

→ Random triggers with random occupancy...

→ Trigger mix will change for Run IIb

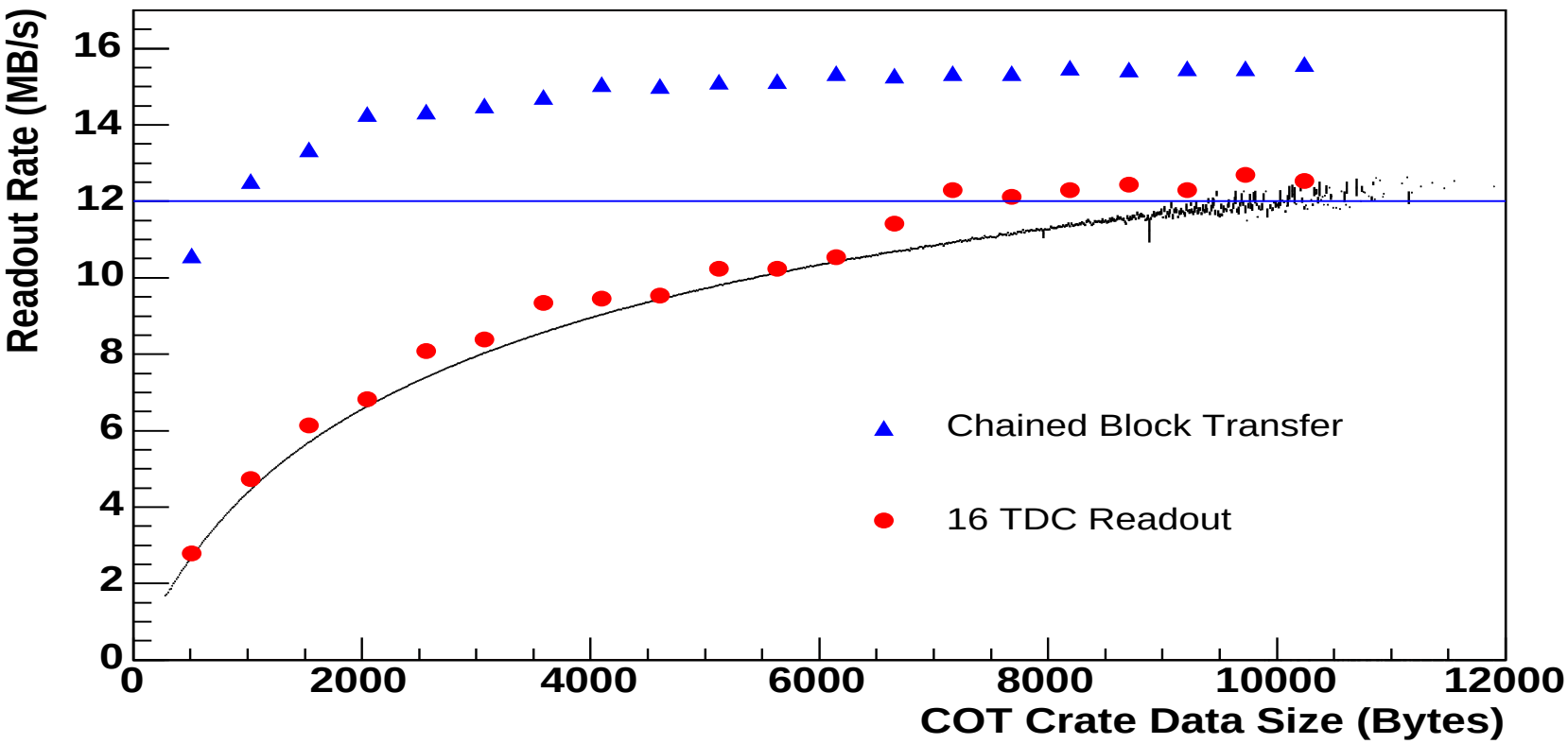
→ EVB upgrade, EVB currently limited to about 400 Hz

→ At high rates we see L2 dead time

→ SVT

→ Silicon

TDC Readout limit $\sim$ 15.8 MB/s
Tracer Readout limit $\sim$ 12 MB/s



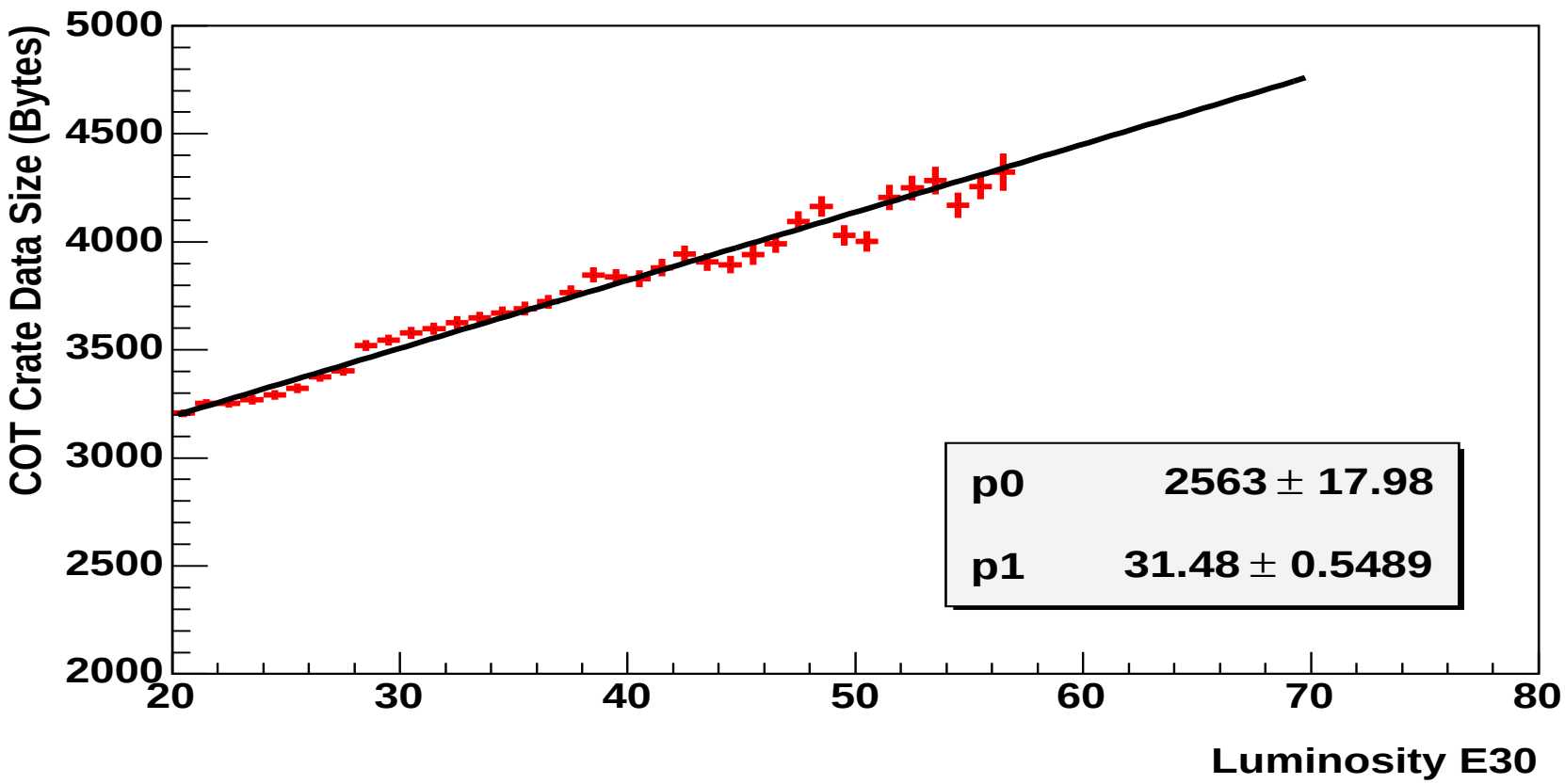
$\rightarrow$ Chained Blk: Read header, read TDC fifo

$\rightarrow$ 16 TDC Readout: 16$\times$ read header, 16$\times$ read TDC fifo

Chained block mode: 12 $\rightarrow$ 15.5 MB/s

Average event size from the COT crates versus luminosity

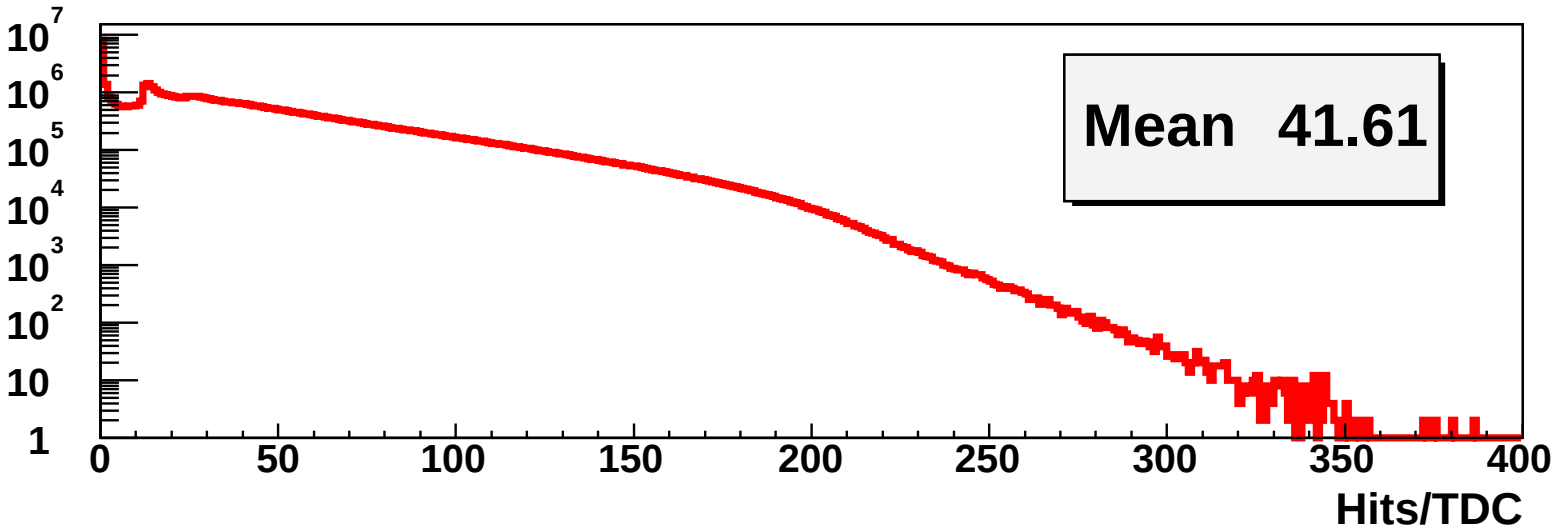
Run 178785

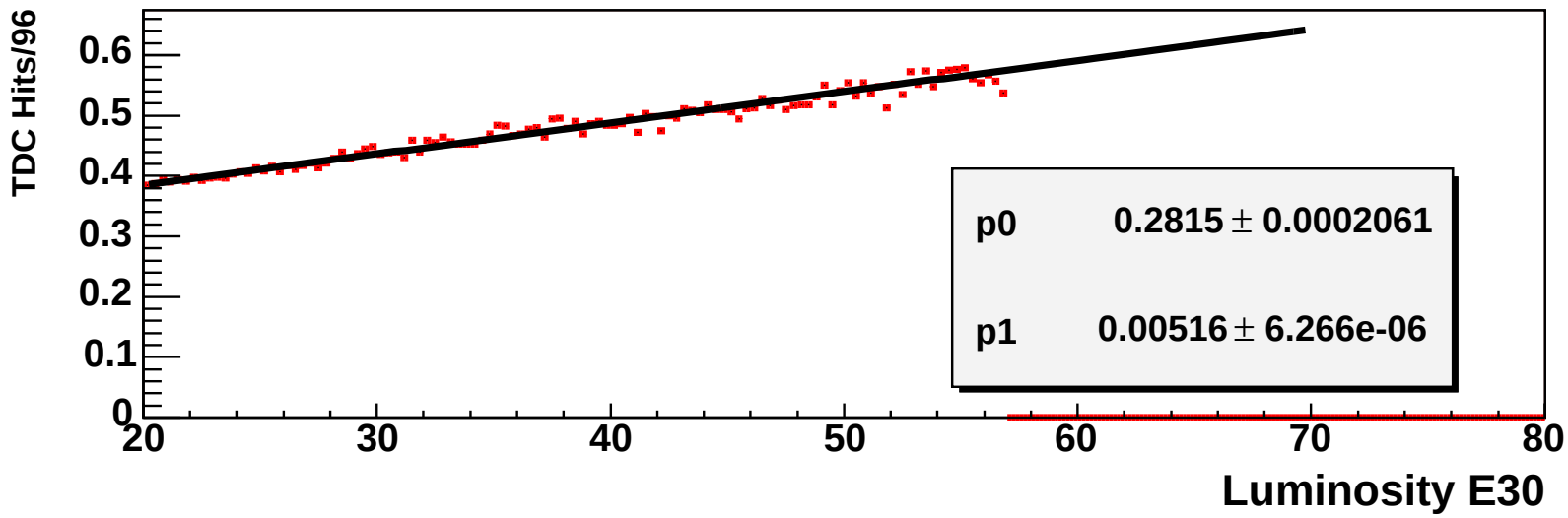


Extrapolation to Run IIb luminosity (330×10^{30})

$$2563 + 31.5 \times 330 = 12958 \quad \text{bytes}$$

$12958 \times 2/3 = 8638 \quad$ bytes

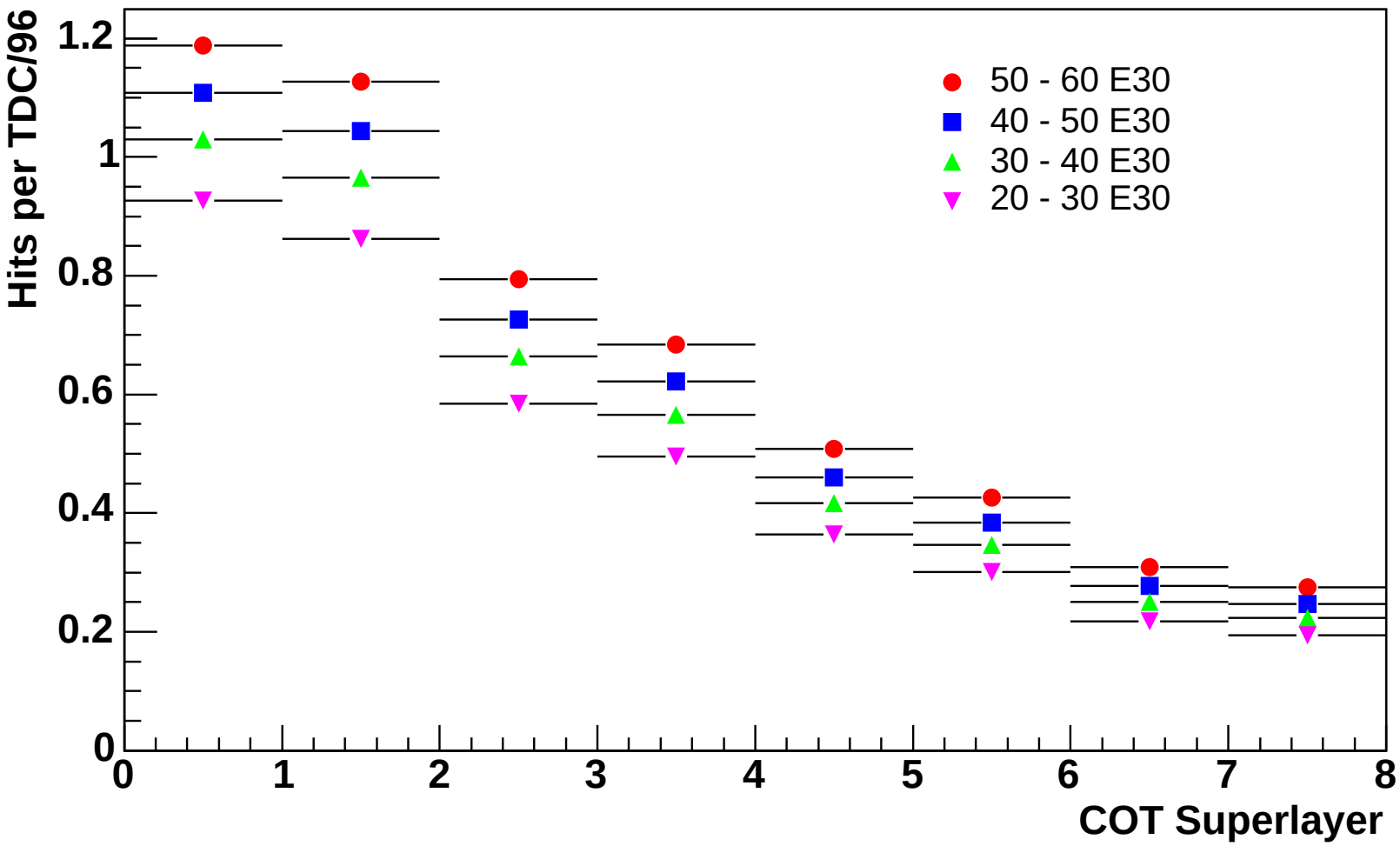




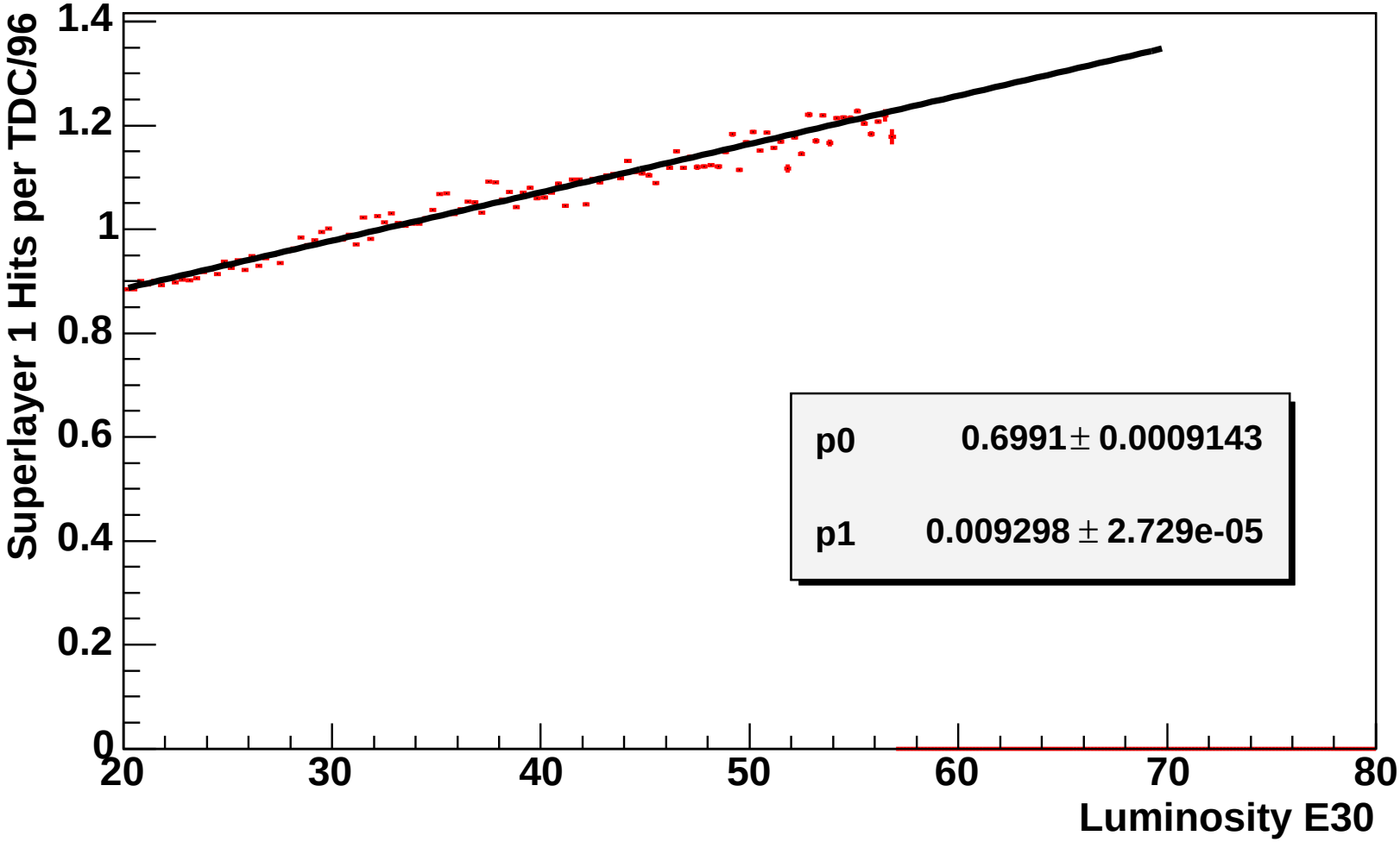
Extrapolation to Run IIb luminosity (330×10^{30})

$$0.28 + 0.005 \times 330 = 1.93 \quad \text{hits/channel}$$

TDC Occupancy for each Superlayer



SL1 Occupancy versus Luminosity

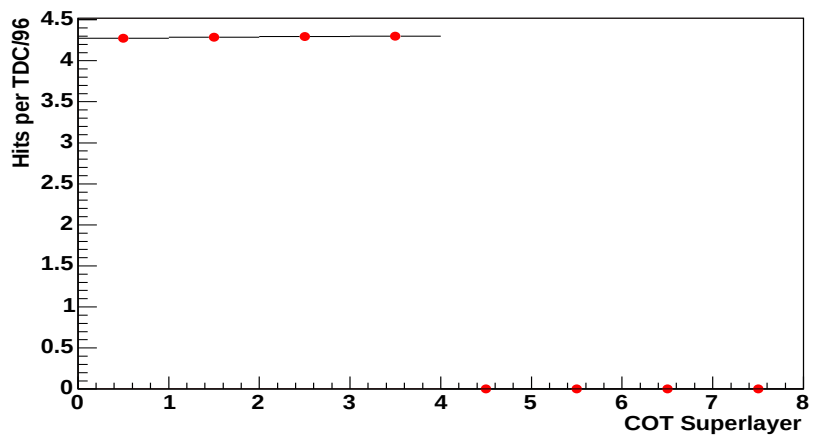


Extrapolation to Run IIb luminosity (330×10^{30})

$$0.6991 + 0.009298 \times 330 = 3.8 \quad \text{hits/channel}$$

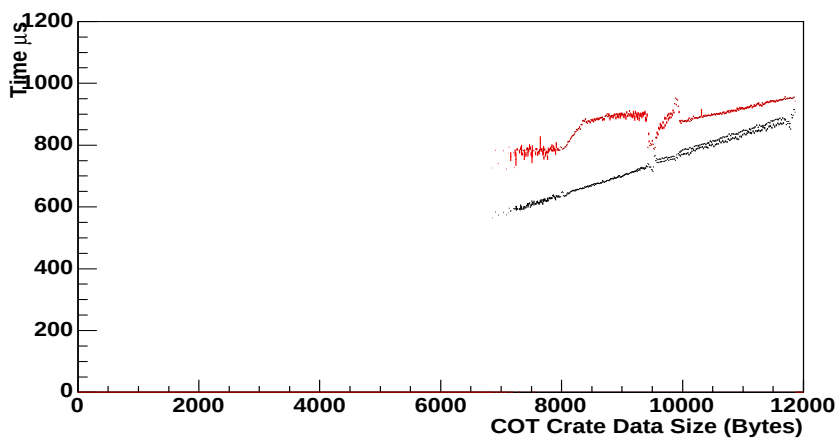
Pulsed Chamber

Not fair to project the DSP processing time from low occupancies to high occupancies → *at higher occupancies the DSP code will have to processes more hits/channel...*



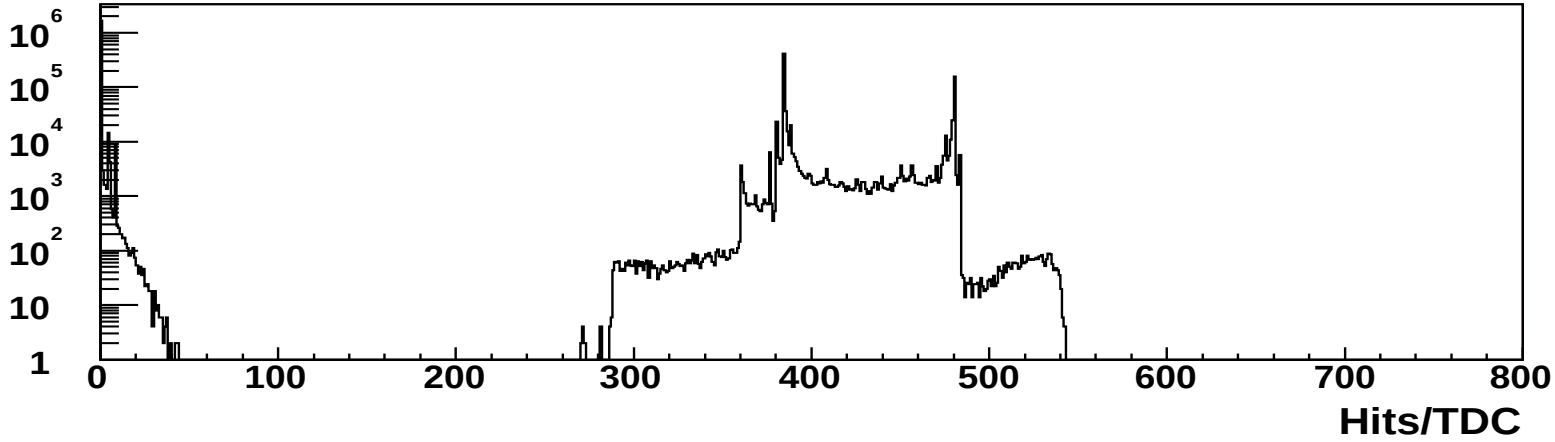
Used the calibration system to pulse the chamber and readout using the calib continuous trigger.

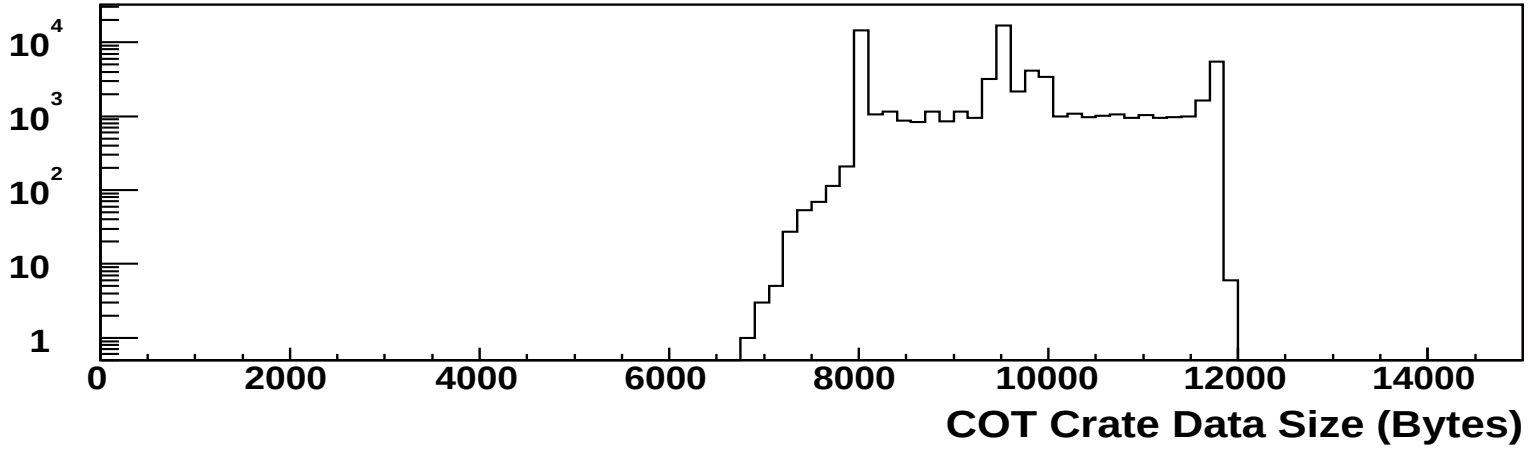
On average we had hits per channel on the inner 4 superlayers



With 4 hits/channel the DSP processing time takes longer than the readout time

Hit distribution when pulsing the COT





It looks like we always have at least one TDC with 5 hits

Readout time is driven by the slowest TDC

Target Rates

```
Number of TDCs/crate:     15 - 17
Number of channels/TDC:   96
Bytes (1 hit/channel):    17*(4+96*4)

Event Size/Crate:
1 hit/channel:            6596 Bytes
2 hits/channel:          13124 Bytes

Target Rate 1000 Hz:
1 hit/channel:             6.6 MB/s  * 2/3 = 4.4 MB/s
2 hits/channel:           13.1 MB/s  * 2/3 = 8.7 MB/s
```

MVME 5500 Evaluation

The MVME 5500 has two ethernet ports (fast and GigE)

Use the fast ethernet for command and control

Use the GigE for data transfer.

We got an evaluation board from Motorola and a trial license from WindRiver

Were able to run our existing software on the board and ran with the card in a front end crate for a couple of days during data taking.

We have ordered three boards in order to continue development, will need an *additional 20 → $60000*.

MVME5500 $3000
VxWorks 5.5 License $15000

We run in SPY mode when reading out the TDCs.

→ Data is caught on the backplane as the TDC is readout and shipped out through the TRACER. Does not require a Read/Write

With the MVME5500 we need to read the data over the backplane *and then* transfer over GigE.

```
GigE                    60 MB/s
TDC readout             15 MB/s
Read VME/Write GigE     12 MB/s

VMEbus  BLT             40 MB/s (Tundra Universe II ~25 MB/s)
VME64   MBLT            80 MB/s (Tundra Universe II ~50 MB/s)
VME64x  2eVME          160 MB/s
VME321  2eSST    320-500+ MB/s
```

Unless the VME readout rate is significantly higher that 15 MB/s it will be a challenge to achieve a sustained throughput near 15 MB/s

The MVME5500 will not improve the readout rate when using the existing TDCs - but it can allow us spread out the data across the more SCPUs reducing congestion further downstream

Conclusions

→ Had to rebalance the data volume to the VRB crates

→ Changes to the DSP code were very successful, involved a lot of work and coordination with offline (10 months...).

→ Readout rate is limited to the maximum of readout time over VME or DSP processing time.

→ For low occupancies the limiting factor is the VME readout...

→ *Readout over VME will be an issue for both the old and the new TDCs...*

→ For high occupancies (4 hits/channel) the DSP processing time starts to be an issue

→ MVME 5500 works with our existing software and we get good performance over GigE

Throughput will be degraded because we have to Read over VME *and* write over GigE (15 MB/s VME → 12 MB/s sustained rate)

Try to model the SL occupancy better to see when DSP processing becomes larger than readout times.

Possible Improvements

$\rightarrow$ Reduce the time between TDC Done and seting TRACER Done. *More than one memory location in static RAM to store header information*

$\rightarrow$ Reduce the data volume. With a compression of 1/3, the projected crate size at 330×10^{30} is 8638 bytes $\rightarrow$ 1380 Hz.

$\rightarrow$ Limit the number of hits on the inner most superlayer. *DSP processing time increases and takes longer than readout time for high occupancies.*