# Using the Michigan TDCs for COT in Run 2B

**Ron Moore**

*Fermi National Accelerator Laboratory*

# Baseline Configuration

- Keep the existing COT TDC configuration
  - Rev E/F TDCs with fast-clear in SL 1-4 (111 TDCs)
  - Rev D TDCs without fast-clear in SL 5-8 (204 TDCs)
- Implement new data format to reduce data volume (new DSP code)
- Buy and install MVME 5500 crate CPUs for COT crates
- Keep TRACER spy-mode readout for sending data to Event Builder
- VRB configuration stays the same

- Can add fast-clear to SL 5 & 6 Rev D TDCs, if occupancy warrants it

| SuperLayer | # TDCs | | Revision |
|---|---|---|---|
| 1 | 21 | 111 | E/F |
| 2 | 24 | | E/F |
| 3 | 30 | | E/F |
| 4 | 36 | | E/F |
| 5 | 42 | 90 | D |
| 6 | 48 | | D |
| 7 | 54 | | D |
| 8 | 60 | | D |

# New Data Format for COT TDCs

- In last report, TDC Committee recommended pursuing common data format for both TDCs
  - Done. (CDF Note 7228) Both TDC groups worked together on format, CPU algorithm for readout
- 2 hits words (time, width) packed into a single 32-bit word (vs 1 hit word/32 bits)
- No channel IDs - instead twelve 32-bit words w/ individual channel hit counts
- Event header word can distinguish Michigan/Chicago TDCs
- Both TDCs assume 4 hits/channel maximum, but format allows max = 7
- Max allowed start time = 306 ns (~500 ns previously)
- Max allowed pulse width = 212 ns (Michigan), 306 ns (Chicago)
- Requires shifting the $T_0$ to get more drift time within smaller window
  - Current $T_0$ = 130 ns → 50 ns
  - Easier for DSP to subtract 80 ns than to change trigger, clock timing
  - "user calibration constants" already in hardware database specify desired shift
- Min data size for single TDC = 56 bytes (0 hits/channel)
- Max data size for single TDC = 824 bytes (4 hits/channel)

# New Event Data Format (as read from TDC)

| Order | Michigan TDC | | Chicago TDC | |
|---|---|---|---|---|
| 1 | Hit data block | Hit data word | Hit data word (Chip 0) | Hit data block |
| 2 | | : | : | |
| : | | : | Hit data word (Chip 0) | |
| : | | : | Hit count word channels 07-00 | Hit count block |
| : | | : | Hit count word channels 15-08 | |
| : | | Hit data word | Hit count word channels 23-16 | |
| : | Hit count block | Hit count word channels 07-00 | Hit count word channels 31-24 | |
| : | | Hit count word channels 15-08 | Hit count word channels 39-32 | |
| : | | Hit count word channels 23-16 | Hit count word channels 47-40 | |
| : | | Hit count word channels 31-24 | Header word (Chip 0) | |
| : | | Hit count word channels 39-32 | Hit data word (Chip 1) | Hit data block |
| : | | Hit count word channels 47-40 | : | |
| : | | Hit count word channels 55-48 | Hit data word (Chip 1) | |
| : | | Hit count word channels 63-56 | Hit count word channels 55-48 | Hit count block |
| : | | Hit count word channels 71-64 | Hit count word channels 63-56 | |
| : | | Hit count word channels 79-72 | Hit count word channels 71-64 | |
| : | | Hit count word channels 87-80 | Hit count word channels 79-72 | |
| : | | Hit count word channels 95-88 | Hit count word channels 87-80 | |
| N-1 | | Possible pad word (0xFFFFFFFF) | Hit count word channels 95-88 | |
| N | | Header word | Header word (Chip 1) | |

# New Data Format (cont'd)

| Hit Data Word for Michigan TDC | | |
|---|---|---|
| | **Channel m, Hit j**<br>$0 \le m \le 95 \quad 1 \le j \le 7$ | **Channel m, Hit j+1**<br>***OR***<br>**Channel m+1, Hit 1** |
| **Bits** | **31-16** | **15-0** |
| | Data (ns) = 213*time + width | Data (ns) = 213*time + width |
| | MAX TIME = 306 ns<br>MAX WIDTH = 212 ns | Later hit on same channel<br>OR<br>First hit on next (higher) channel |

| Hit Data Word Definitions | | |
|---|---|---|
| **Time** | **Width** | **Definition** |
| 1 - MAX TIME | 1 – (MAX WIDTH-1) | Complete pulse (leading and trailing edges) |
| 1 - MAX TIME | MAX WIDTH | Unpaired leading edge (no trailing edge found) |
| 0 | 1 – (MAX WIDTH-1) | Unpaired trailing edge (no leading edge found) |
| 0 | MAX WIDTH | Input level "high" over possible width range |

# New Data Format (cont'd)

| Hit Count Word | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bits** | **31-28** | **27-24** | **23-20** | **19-16** | **15-12** | **11-08** | **07-04** | **03-00** |
| **Channel # modulo 8** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Notes**

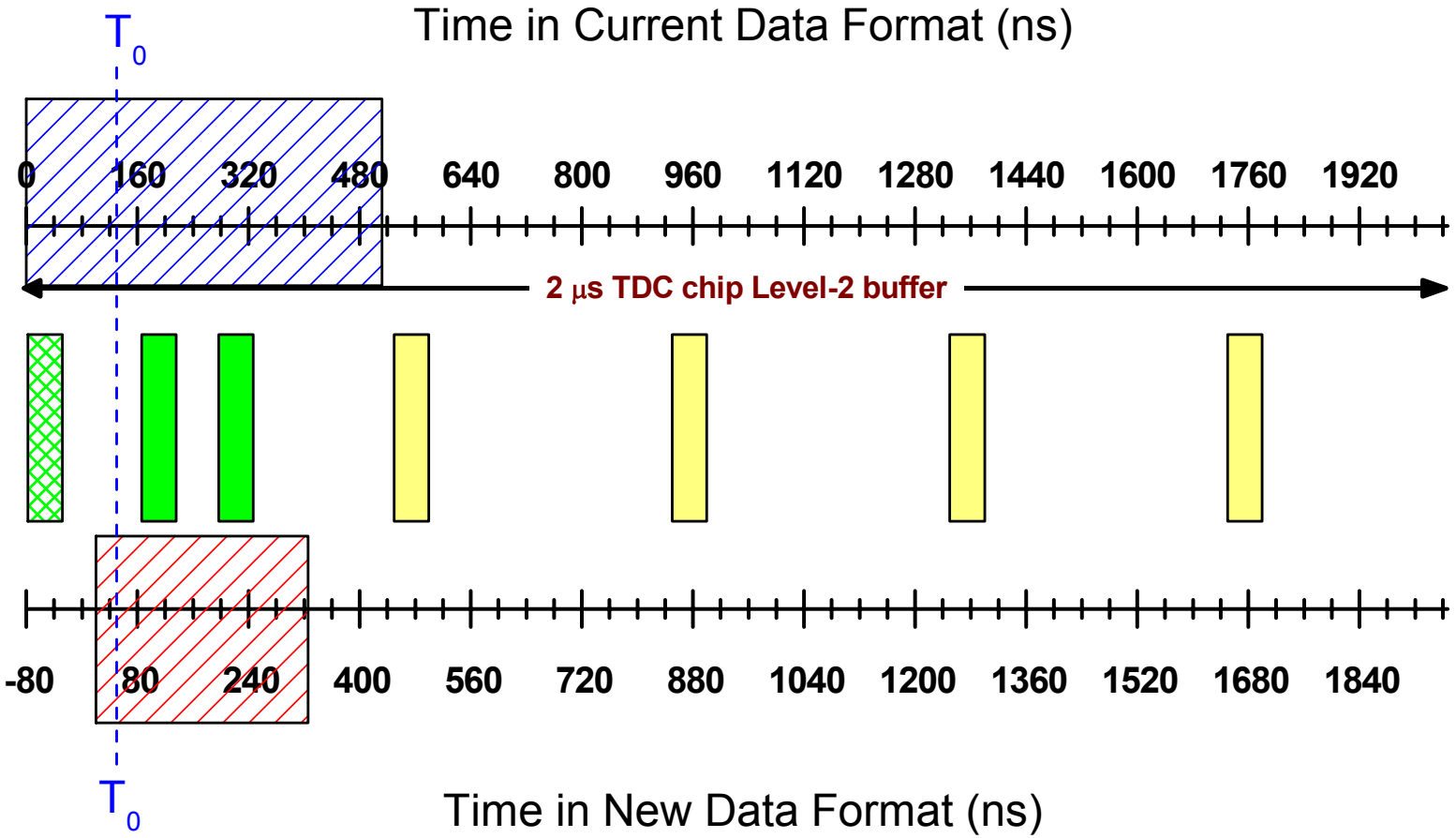
- Each channel hit count has 4 assigned bits, but only the lowest 3 bits are needed since the maximum # hits / channel = 4. (7 is the limit for this format.)
- The Chicago TDC uses the uppermost for each channel to indicate if the channel is enabled (1) or disabled (0).
- The Michigan TDC always sets the uppermost bit to 0 for each channel.

| Header Word | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bits** | **31-23** | **22** | **21** | **20** | **19-18** | **17-8** | **7-0** |
| | Module ID (User-Specified) | TDC type<br><br>0 = Michigan<br>1 = Chicago | Chip number<br><br>0 for TDC type = 0<br>0/1 for TDC type = 1 | Unused<br><br>always 0 | L2 buffer number (0-3) | # hits in hit data block | Bunch Crossing Counter |

**Notes**

- The Module IDs are the same as those specified in CDF note 4152.
- The TDC type simply distinguishes between the two TDC types.
- The chip number is relevant for the Chicago TDC only.

# Hits in the TDC L2 Buffers



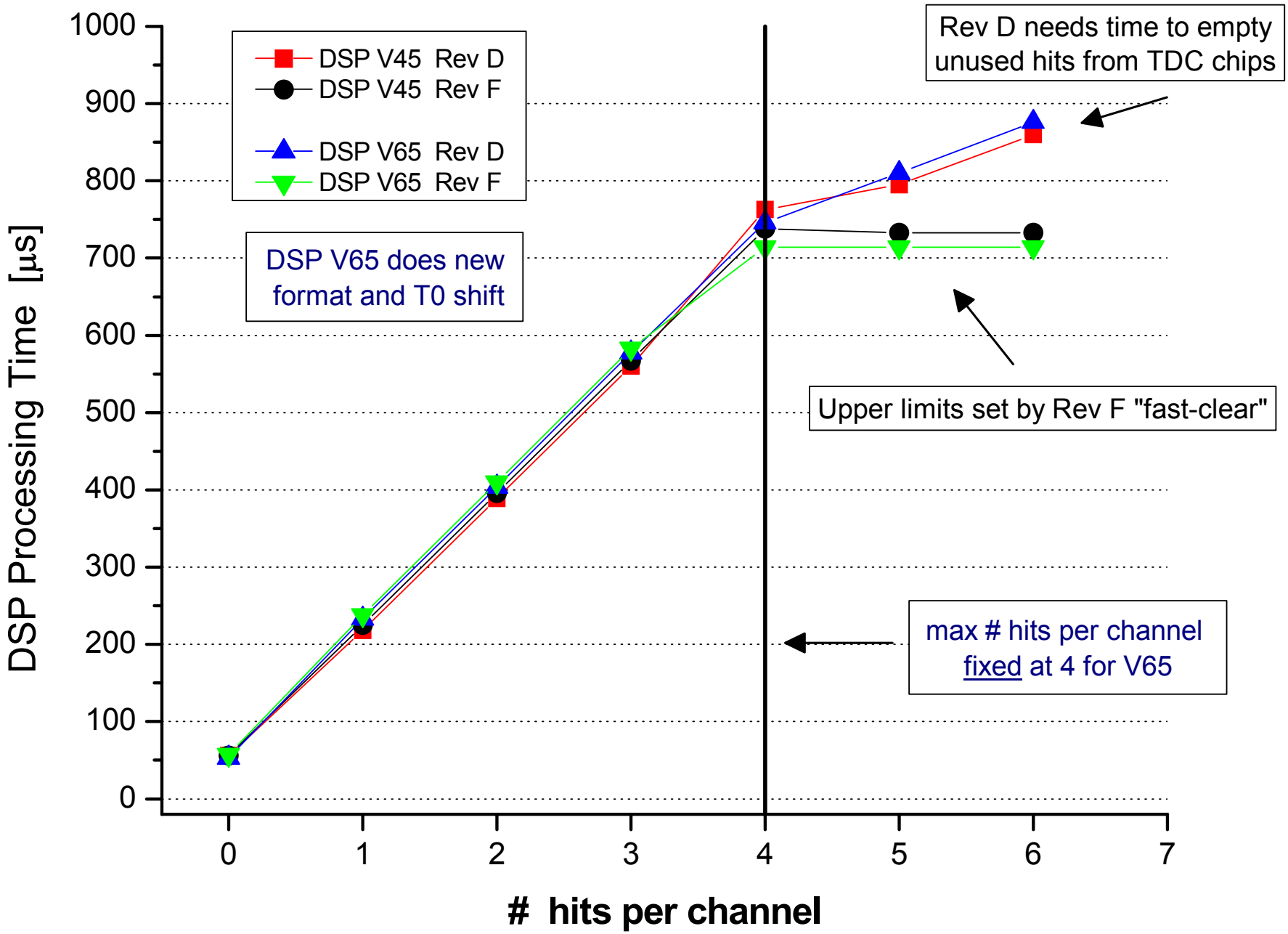

*$T_0$ shift = -80 ns*

allowed time window

in-time hits to be processed

early hit processed in old format, but thrown away in new format

hits from previous crossings to be thrown away


DSP Processing Time vs # hits per channel
DSP Processing Time [µs]
1000
900
800
700
600
500
400
300
200
100
0
0
1
2
3
4
5
6
7
# hits per channel
DSP V45 Rev D
DSP V45 Rev F
DSP V65 Rev D
DSP V65 Rev F
DSP V65 does new format and T0 shift
Rev D needs time to empty unused hits from TDC chips
Upper limits set by Rev F "fast-clear"
max # hits per channel fixed at 4 for V65

# DSP Processing Time Benchmarks

| | Time [μs] | | | |
|---|---|---|---|---|
| **Hits per channel** | **V45 Rev D** | **V45 Rev F** | **V65 Rev D** | **V65 Rev F** |
| 0 | 49 | 56 | 53 | 58 |
| 1 in-time | 218 | 225 | 233 | 238 |
| 2 in-time | 389 | 396 | 404 | 410 |
| 3 in-time | 560 | 567 | 578 | 583 |
| **4 in-time** | **763** | **737** | **746** | **714** |
| 5 in-time | 795 | 733 | 810 | 714 |

- Processing time = ~DONE→DONE after a L2A (measured on TRACER front panel)
- Max # hits/channel = 4 within allowed time window
- V45 is the current DSP code version
- V65 is the full-blown new format used in most recent readout rate tests
  - MAXSTART = 306 (max leading edge time), USERCONST = -80 ($T_0$ shift)
- Back of the envelope: Rev F max readout rate @ 4 hits/chan = (DSP Processing Time)$^{-1}$
  - Ignoring all overhead, deadtime, DSP V65 should be capable of 1400 Hz L2A rate

# More on DSP Processing Time

- How much time does it take to throw away unused hits?

- Hits > maximum time from previous events
  - Rev F = no time (fast-clear takes care of that)
  - Rev D = 110 μs for first one, then 65 μs thereafter (if # in-time hits < 4)
    65 μs per hit/channel (if # in-time hits >= 4)

  - Rev D V65: 2 in-time hits = 403 μs
  - Rev D V65: 2 in-time hits + 4 out-of-time hits in every channel = 708 μs

- Early hits with negative time after $T_0$ shift
  - Rev D and F = 110 μs per hit in every channel
  - Rev D V65: 2 in-time hits in every channel = 233 μs
  - Rev D V65: 1 early hit + 2 in-time hits in every channel = 343 μs

# COT Pulser Rate Measurements

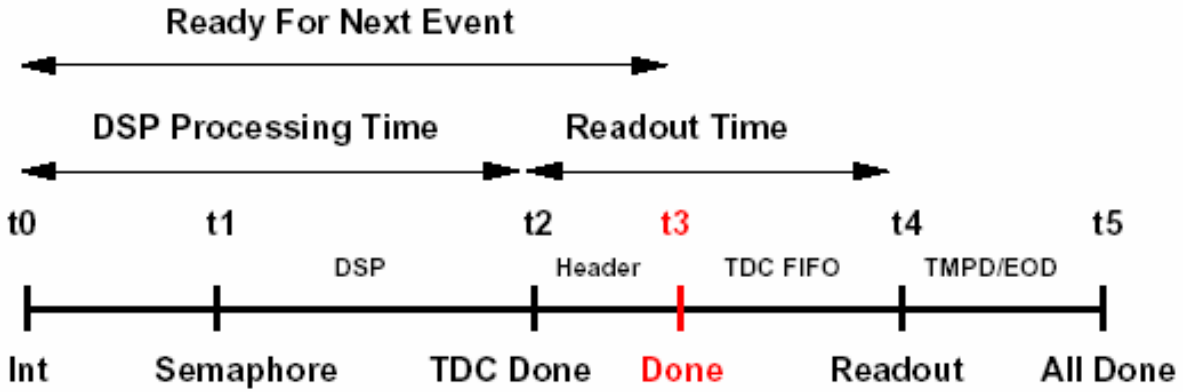
- Synchronized external pulser to put only in-time hits into calibration lines
  - Previous tests used free-running pulser that gave many out-of-time hits
- Run in "calib-continuous" mode, spy-mode readout, data to SEVB, ~100% deadtime
- Pulsing SL 1-4 only
  - As expected, rate determined by DSP + some overhead, not readout
  - Can that overhead be reduced?
- Pulsing all SL 1-8
  - Unrealistic data volumes
  - Rate consistent with readout, as expected

| SL 1-4 | | | | | |
|---|---|---|---|---|---|
| # hits/chan | # bytes/crate | ≈ readout time [μs] | DSP time [μs] | rate [Hz] | 1/rate [μs] |
| 0 | 952 | 150 | 58 | - | - |
| 1 | 2104 | 250 | 238 | 2414 | 414 |
| 2 | 3256 | 350 | 410 | 1739 | 575 |
| 3 | 4408 | 450 | 583 | 1374 | 728 |
| 4 | 5560 | 550 | 714 | 1179 | 848 |

| SL 1-8 | | | | | |
|---|---|---|---|---|---|
| # hits/chan | # bytes/crate | ≈ readout time [μs] | DSP time [μs] | rate [Hz] | 1/rate [μs] |
| 0 | 952 | 150 | 58 | 3119 | 321 |
| 1 | 4216 | 450 | 238 | 2200 | 454 |
| 2 | 7480 | 650 | 410 | 1595 | 627 |
| 3 | 10744 | 850 | 583 | 1237 | 808 |
| 4 | 14008 | 1050 | 746 | 953 | 1049 |

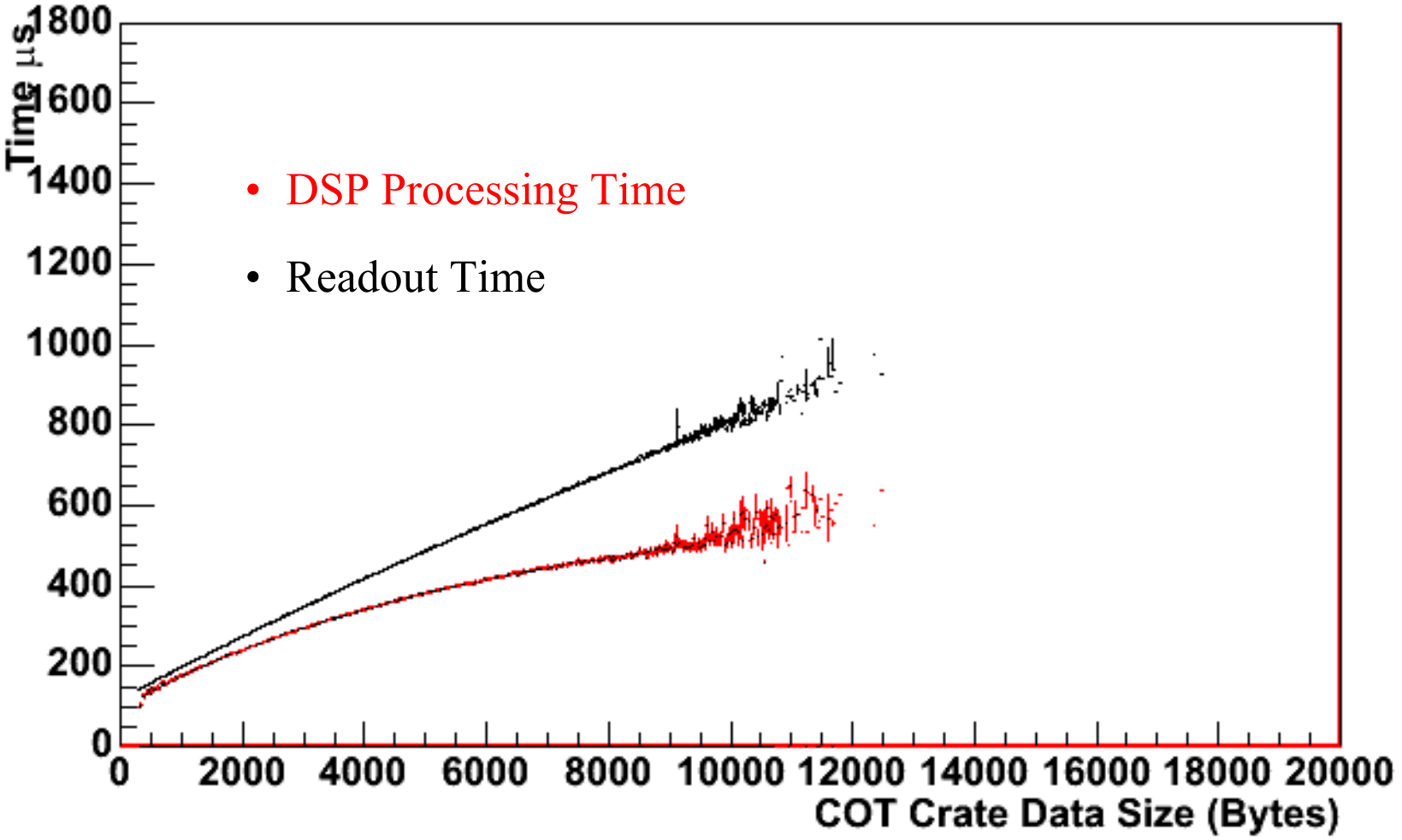
# Crate CPU Timing Measurements

Timing information is stored for each event in the TMPD bank



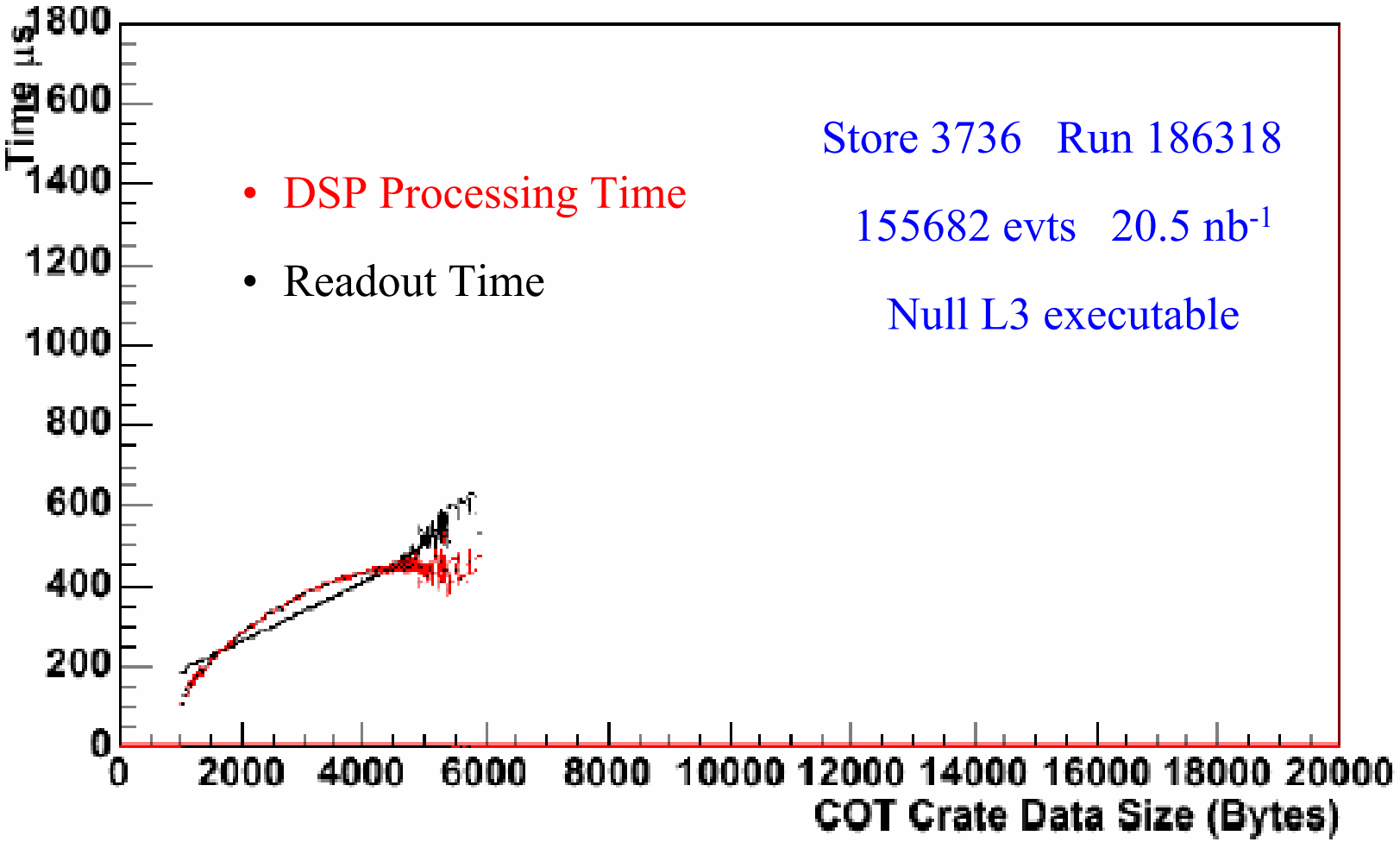

- DSP starts reading TDC chips when L2A detected, sets local TDC Done after filling FIFO
- Once all TDCs done, CPU reads pseudo-header from TDCs, then sets TRACER DONE
  - TS releases L2 Buffer after TRACER Done
- CPU reads event data from TDC FIFOs, TRACER spies on backplane, sends data to VRB

# DSP V45 Processing Time & Readout Time



rsm6

# DSP V65 Processing Time & Readout Time



rsm6

# Why the kink in readout time @ 4500 bytes?

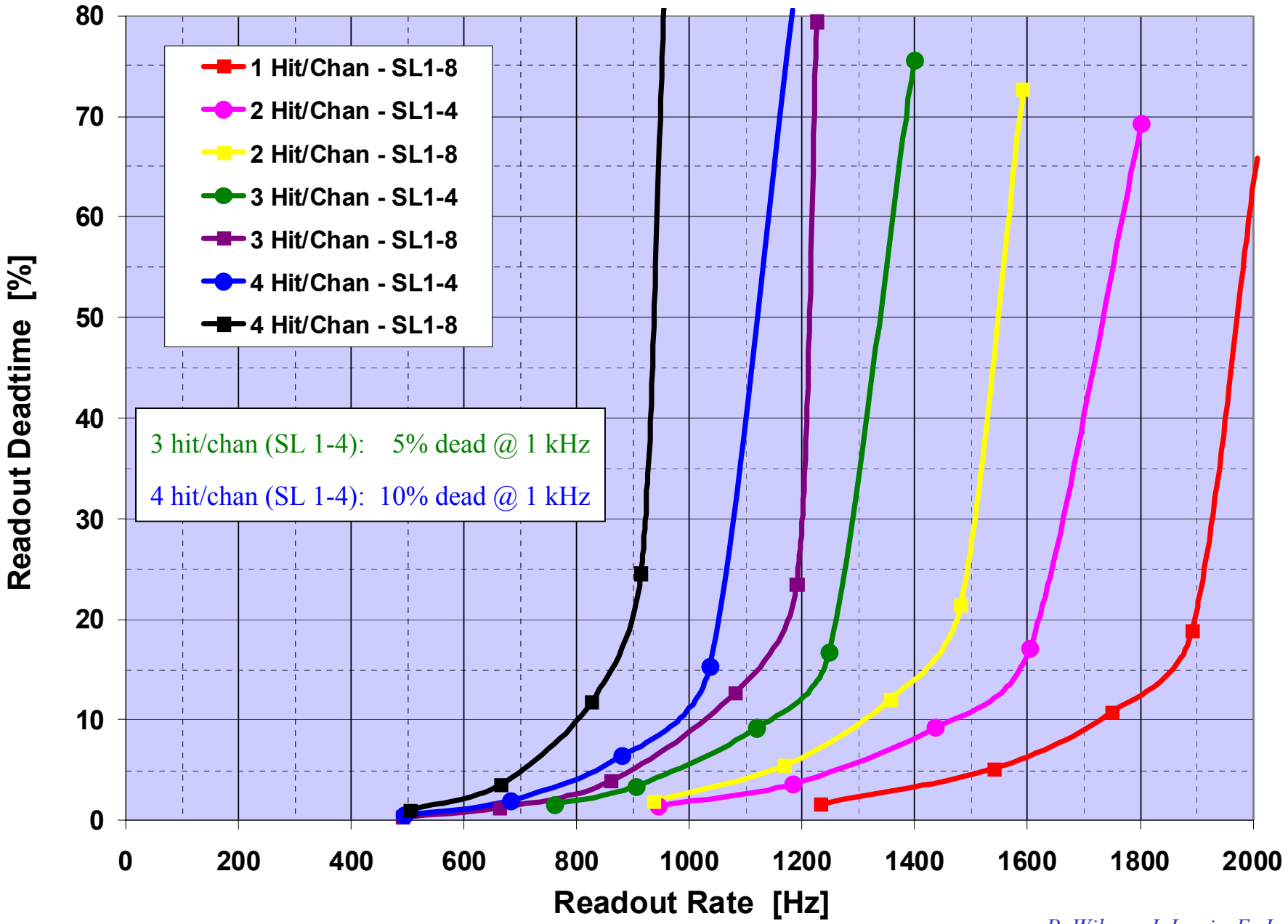
Ron Moore, 9/21/2004

# Trigger Rates using the Sparky the Phototube

- Sparky used as trigger for COT "in-time" pulsing and as L1 trigger input
- Vary Sparky's voltage to knob the trigger rate, then measure deadtime (Auto L2A)
- HEVB not used ⇒ not limited by current HEVB bandwidth (≈420 Hz)

| SL 1-4 | | | | SL 1-8 | | | |
|---|---|---|---|---|---|---|---|
| Hits/ Chan | FRED Rate (Hz) | L1 Rate (Hz) | Deadtime (%) | Hits/ Chan | FRED Rate (Hz) | L1 Rate (Hz) | Deadtime (%) |
| 2 | 962 | 945 | 1.5 | 2 | 957 | 937 | 1.9 |
| 2 | 1236 | 1184 | 3.7 | 2 | 1243 | 1168 | 5.5 |
| 2 | 1601 | 1436 | 9.2 | 2 | 1555 | 1356 | 12.0 |
| 2 | 1969 | 1604 | 17.1 | 2 | 1900 | 1481 | 21.4 |
| 2 | 6167 | 1802 | 69.3 | 2 | 6191 | 1592 | 72.7 |
| | | | | | | | |
| 3 | 774 | 760 | 1.6 | 3 | 492 | 490 | 0.3 |
| 3 | 941 | 905 | 3.4 | 3 | 674 | 663 | 1.3 |
| 3 | 1243 | 1119 | 9.2 | 3 | 898 | 860 | 3.9 |
| 3 | 1531 | 1248 | 16.7 | 3 | 1239 | 1080 | 12.7 |
| 3 | 6155 | 1398 | 75.6 | 3 | 1568 | 1190 | 23.5 |
| | | | | 3 | 5772 | 1226 | 79.4 |
| | | | | | | | |
| 4 | 496 | 493 | 0.5 | 4 | 510 | 503 | 1.1 |
| 4 | 699 | 683 | 2.0 | 4 | 691 | 664 | 3.6 |
| 4 | 948 | 880 | 6.4 | 4 | 941 | 825 | 11.8 |
| 4 | 1241 | 1036 | 15.3 | 4 | 1233 | 914 | 24.6 |
| 4 | 6158 | 1182 | 80.7 | 4 | 6146 | 956 | 83.5 |

*As expected, the L1 rates in highlighted rows are consistent with COT Pulser rate measurements on previous page.*




*P. Wilson, J. Lewis, E. James*

# Expectations based on TDC Occupancy Study

| Min bias + zero bias | | | | | |
|---|---|---|---|---|---|
| SL | avg # hits / wire | max # hits / wire | # TDCs in SL | avg data volume [bytes] | max data volume [bytes] |
| 1 | 2.2 | 3.0 | 21 | 10046 | 13272 |
| 2 | 2.0 | 2.6 | 24 | 10560 | 13325 |
| 3 | 1.8 | 2.5 | 30 | 12048 | 16080 |
| 4 | 1.4 | 2.1 | 36 | 11693 | 16531 |
| 5 | 1.2 | 2.0 | 42 | 12029 | 18480 |
| 6 | 1.0 | 1.8 | 48 | 11904 | 19277 |
| 7 | 0.8 | 1.6 | 54 | 11318 | 19613 |
| 8 | 0.6 | 1.3 | 60 | 10272 | 18336 |
| Total | | | | 89870 | 134914 |
| per crate | | | | **4494** | **6746** |

Above data from the XFT merged hit study @ lumi = 4 E32 $cm^{-2}$ $s^{-1}$

- SL 1 sets max DSP time
  - 3 hits/chan ⇒ 583 μs
  - 4 hits/chan ⇒ 714 μs
  - The truth must be between the two?
- Readout time based on per crate data volume and Frank's previous measurements
  - Avg ≈ 400 μs  Max ≈ 550 μs
  - Readout time < DSP time

# Do we need fast-clear on SL 5 & 6 TDCs?

- Want DSP processing time in Rev D SL 5, 6 < Rev F SL 1
- For SL 1: 3 hits/chan ⇒ 583 μs  4 hits/chan ⇒ 714 μs
- For SL 5: assume 2 hits/chan in trigger event (max), 4 hits/chan (avg) total for the four earlier events in the TDC chip buffers
  - Rev D DSP time = 707 μs > SL 1 3 hits/chan, pretty close to SL 1 4 hits/chan

| **Rev D V65 DSP Processing time [μs]** | | **# out-of-time hits/chan (to be emptied from TDC buffer)** | | | | | |
|---|---|---|---|---|---|---|---|
| | | **1** | **2** | **3** | **4** | **5** | **6** |
| **In-time hits/chan** | **1** | 343 | 408 | 473 | 538 | 603 | 668 |
| | **2** | 513 | 578 | 642 | 707 | 772 | 837 |
| | **3** | 688 | 753 | 818 | 883 | 948 | 1013 |
| | **4** | 810 | 875 | 940 | 1005 | 1070 | 1135 |

*Adding fast-clear to SL 5 & 6 TDCs is probably a good idea to ensure SL 1 TDCs are the slowest.*

# What else?

- Can additional improvements be made?
  - DSP L2A processing speed probably maxed out
  - Any other VME/Universe chip exploits?
    - Probably not…Bill B. already implemented those that helped
  - Apparent overhead between TDC done and TRACER done (≈150 μs)
    - CPU reading TDC pseudo-header = 26-28 μs
    - Could reduce/eliminate by using circular buffer of SRAM words to store > 1 pseudo-header
    - After TDC done, CPU sets TRACER DONE to release L2 buffer, then reads pseudo-headers, begins FIFO readout
    - Requires synchronization between DSP and CPU writing/reading pseudo-header location
    - Maybe a 20-30 Hz rate improvement
  - What causes the rest of the overhead, and can it be reduced? *(Trigger Manager improvements?)*
- What else needs to be done to implement DSP V65 into operations
  - Offline/L3 code
    - David Dagenhart already done with his part of offline code
    - Waiting for Aseet to wrap up new offline COT code
  - Modify COT calibration and TDC Test for new format
    - Already done, verified, Bill B?

# Miscellany

- *What is the spare situation at FNAL and at Michigan?*
- *Any more details on adding fast-clear to Rev D TDCs? Has it been done at Michigan, is there a written procedure?*
- *No need to commission a new system if staying with Michigan TDCs.*
  - *Lots of experience (not all good), but we understand them well.*
- Myron has already affirmed Michigan's institutional responsibility to maintain the Michigan TDCs throughout the remainder of Run 2.

# Summary

- Propose to continue using Michigan TDCs for COT readout for rest of Run 2
- Implemented common, compact data formats for both TDCs
  - Data volume is reduced by almost a factor of 2
- DSP processing time well under 1 ms with 4 hits in every channel for inner SL
  - DSP time, not readout time, is the performance limitation
- Probably want "fast-clear" installed onto SL 5 and 6 Rev D TDCs
- Obtained a set of consistent readout rate measurements
  - 3 hits/chan max in SL 1-4: 5% deadtime @ 1000 Hz
  - 4 hits/chan max in SL 1-4: 10% deadtime @ 1000 Hz
- Additional modest performance gain possible by reducing overhead

- Michigan TDCs are viable for the COT readout for the rest of Run 2