



TDC DSP Updates

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Extra FIFO Read with PPC Solved

- After RTFM, the “read-ahead” cycle with PPC block transfers won’t occur if ending address is on 256-byte boundary
- Use any address in $0x80000 - 0xFFFFFFFF$ to read TDC FIFO
- If you know the # words in FIFO, you can shift the starting address for BLT such that above condition is satisfied
- For DMA, starting address also needs to start on 8-byte boundary
- Satisfying both address conditions requires total # words is even



Extra FIFO Read with PPC Solved

- Changes to DSP code
 - Writes a dummy word to FIFO if # (data words + header) is odd
 - Write the total word count (including the dummy word) to SRAM
- Changes to front-end readout code
 - First read total word count from SRAM
 - Calculate starting address to satisfy the above conditions
 - $\text{Offset} = 256 - ((\text{total_word_count} * 4) \bmod 256)$
 - Do a block read of `total_word_count` words using calculated start address
- Can now exploit “dual-portedness” of FIFO without deleting the header word of subsequent event



DSP Speed Improvements (no format changes)

- I had an epiphany over Memorial Day weekend...
- L2A processing faster than I thought it could ever be, yet full formatting is retained.

Algorithm	Overhead	Time per processed hit in <u>every</u> channel	Time per unprocessed hit in <u>every</u> channel
Current V36	83	282	65
DEV38 (full formatting)	50	220	65

- Had to eliminate min width checking (not used?) for space
- Retained separate readout list for no calibrations added
- Not fully tested (unpaired edges), but it will work



DSP Speed Improvements (format changes)

- Gain 3 more cycles / hit word if “first-hit” bit removed
- Gain 2 more cycles / hit word if header word follows the data words
 - Write directly to FIFO, rather than using stack for temporary storage
 - Dummy word would still be at very end
- JDL says reformatting can be done in L3 without penalty

Algorithm	Overhead	Time per processed hit in <u>every</u> channel	Time per unprocessed hit in <u>every</u> channel
DEV38 (full formatting)	50	220	65
DEV38 (no first hit bit, header after data) ??	50	197	65



DSP L2A Processing Time Summary

Algorithm	Overhead	Time per processed hit in <u>every</u> channel	Time per unprocessed hit in <u>every</u> channel	Time for 1 hit/channel in window + 2 hits/channel outside of window
Current V36	83	282	65	495
DEV38 (full formatting)	50	220	65	400
DEV38 (no first hit bit, header after data) ??	50	197	65	376
Rev E/F with other improvements + fast clear ??	55	197	0	251
Previous best I thought could achieve with minimal formatting and writing directly to FIFO (doubled data volume)	59	213	65	402



Summary

- New readout scheme solves the “extra FIFO read” problem with PPC controllers’ block transfer
 - Can now exploit “dual-portedness” of FIFO without deleting the header word of subsequent event
- DSP code speeded up greatly without format changes
- Additional speed to be gained by changing data format
 - Eliminate “first hit” bit in data words
 - Event header word comes **after** data words
 - Reformat to expected bank structure in L3
- DSP code with “fast clear” for Rev E/F ready for testing
- Started writing CDF Note on these issues