



New TDCs, New DSP Code

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Rev E / Rev F TDC Testing

- OK in diagnostic crate, TDC Test
 - 2 of 17 Rev F boards have bunch counter problems
- Had 2 Rev E + 7 Rev F in hadron crate for couple stores
 - OK, saw ~couple ns timing shift. Confident to install in COT.
- Had 2 Rev E + 8 Rev F in COT 18 for last 3 stores
 - ~Chan 70-75 noisy, bad widths in data (not cable problem)
 - Saw noise in COT Calibration, too?
 - OK with XTC Mezzanines (not checked upstairs)
- Now have 2 Rev E + 15 Rev F in COT 18

- All seems OK in spy mode with latest modified Tracers
 - See comments by Frank and Bill



DSP Code Modifications

- Recall from last meeting, there were several steps...
 1. Faster L2A processing – no format changes
 2. Support Rev E/F TDC chip “fast-clear”
 3. Dual-port FIFO support (addition of padding word to readout)
 4. Even faster L2A processing – via format changes

– #1 and #4 are essentially independent (benefits add directly)

Version	Features
V37 (default)	None of the above
V40	Faster processing – no format changes
V41	Like V37, with L2A counters
V42	Like V37, with fast-clear and dual-port FIFO
V43	Fast-clear, dual-port FIFO, faster processing WITH format changes, no mods for faster processing without format changes



DSP V40 – Faster, no format changes

- Looked OK in diagnostic crate, hadron TDC crate
 - Programmed every TDC in system with V40
- Used in one HEP store, saw problems in COT
 - Reverted back to V37 in every TDC
- In COT, saw 20-30 ns time shift in channel 66
- Now understood to be excess of unpaired trailing edge hit words (width = 0) with time > 1000 ns
 - Predominantly chan 66, but others, too
 - But, data from trigger event time window OK?
 - Could be single bit corruption???
 - Similar symptoms seen in V37, but on a much lower scale
- Have not reproduced symptoms elsewhere, not yet understood how DSP could cause it



Dual-Ported FIFO Operation

- Allows simultaneous reading/writing to/from TDC FIFO
 - Eliminates PPC controller's Universe VME "read-ahead" cycle that would clobber header word of subsequent event's data
 - Can use any address in 0x80000 – 0xFFFFF to read FIFO
 - Force DMA block transfer addresses to begin on 8-byte boundary and end on 256-byte boundary (total word count must be EVEN)
- DSP V42 + Bill Badgett's readout code modifications
 - DSP adds a padding word (0), if needed, to make the total word count even, then writes the total word count to TDC SRAM
 - Readout code gets word count from SRAM, calculates the starting address, performs the block transfer accordingly
- I would like to make this default ASAP
 - Have 2 cosmic runs with COT 00 read out this way
 - L3 still needs some code patches?
 - TDC Test needs modification, too. (Kirby, I presume?)



DSP V43 – Faster, via format changes

- Remove “first-hit” flag from hit words (highest order bit)
- DSP writes hit words directly to FIFO (reverses word order in FIFO)
- Let L3 code convert data back to the expected bank structure

Order of data read from TDC FIFO	
DSP V37 (current)	Proposed (e.g., DSP V43)
Header word	Chan 0 – first (earliest) hit
Chan 95 – last (latest) hit	:
:	Chan 0 – last (latest) hit
Chan 95 – first (earliest) hit	:
:	Chan 95 – first (earliest) hit
Chan 0 – last (latest) hit	:
:	Chan 95 – last (latest) hit
Chan 0 – first (earliest) hit	Header word
-	Possible padding word = 0



DSP L2A Processing Time Summary

Algorithm	Overhead	Time per processed hit in <u>every</u> channel	Time per unprocessed hit in <u>every</u> channel	Time for 1 hit/channel in window + 2 hits/channel outside of window
V37 (default) (All Revs)	83	282	65	495
V40 (Rev D)	50	220	65	400
V43 (Rev F)	87	233	0	320
Combine V40/V43 mods (<u>measured</u> for Rev F)	55	193	0	250



Bunch Counter Mismatch Investigation

- Based on data provided by Bill Badgett, it appears that bunch counter mismatches occur when TDC “missed” a L2A (board remains DONE from previous L2A)
- I made a special DSP code (V41) that implements L2A counters in SRAM (1 for each buffer)
- Bill B. made readout code that puts these counters into TMPD back (just for DSP V41)
- Ran 2-3 stores with DSP V41 in COT 01 crate

- No bunch counters mismatches occurred in that crate during those stores, so there is no additional info about the L2A – mismatch link



Improving Test Configurations

- Our location sequence for testing (LVDS) boards has been:
 1. Diagnostic crate
 2. Hadron timing crate
 3. COT crate
- Can only run 12 TDCs in diagnostic crate
 - Need beefier power supply (new supply to be installed soon)
- The hadron timing crate not read out in spy mode because of laser TDC not used in normal runs
 - Hadron crate is **not** “just like a COT crate”
 - Found problems in COT crates that could have been caught upstairs
- I propose moving that laser TDC somewhere else so we can readout hadron crate in spy mode, especially for testing
 - JDL thinks moving it should not be a problem
 - Who will take charge?