

## New COT TDC Data Formats for the Michigan and Chicago TDCs

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A truly common format shared by the two TDCs has been deemed impractical, although certain features such as channel ordering for the hit data and hit count words can be accommodated. Based on readout procedure and format, the Michigan TDC looks like a single 96 channel TDC, whereas the Chicago TDC appears to be two 48-channel TDCs.

The following formats are assumed to be used when reading out both TDC types during the commissioning phase of the Chicago TDCs. Once only Chicago TDCs are used for COT readout, a new format may be implemented to exploit a faster readout scheme, but that format is not described here.

Unless noted otherwise, both TDC types already implement this format. For the Michigan TDC, DSP code V61 is required. (Can I get FPGA version numbers for the Chicago TDC???)

### Format of data readout from TDCs

Order		Michigan (Run 2A)	Chicago (Run 2B)	
1	Hit data block	Hit data word	Hit data word (Chip 0)	Hit data block
2		:	:	
:		:	Hit data word (Chip 0)	
:		:	Hit count word channels 07-00	Hit count block
:		:	Hit count word channels 15-08	
:	Hit data word	Hit count word channels 23-16		
:	Hit count word channels 07-00	Hit count word channels 31-24		
:	Hit count word channels 15-08	Hit count word channels 39-32		
:	Hit count block	Hit count word channels 23-16	Hit count word channels 47-40	Hit data block
:		Hit count word channels 31-24	Header word (Chip 0)	
:		Hit count word channels 39-32	Hit data word (Chip 1)	
:		Hit count word channels 47-40	:	
:		Hit count word channels 55-48	Hit data word (Chip 1)	
:		Hit count word channels 63-56	Hit count word channels 55-48	Hit count block
:		Hit count word channels 71-64	Hit count word channels 63-56	
:		Hit count word channels 79-72	Hit count word channels 71-64	
:		Hit count word channels 87-80	Hit count word channels 79-72	
:		Hit count word channels 95-88	Hit count word channels 87-80	
N-1		Possible pad word (0xFFFFFFFF)	Hit count word channels 95-88	
N		Header word	Header word (Chip1)	

- The Chicago TDC chip FPGAs will need to be modified to put the header word at the end of the hit count block. Mircea indicated it is not difficult to do.

Hit Data Word for Michigan TDC		
	<b>Channel m, Hit j</b> $0 \leq m \leq 95 \quad 1 \leq j \leq 7$	<b>Channel m, Hit j+1</b> <i>OR</i> <b>Channel m+1, Hit 1</b>
<b>Bits</b>	<b>31-16</b>	<b>15-0</b>
	Data (ns) = 213*time + width	Data (ns) = 213*time + width
	MAX TIME = 306 ns MAX WIDTH = 212 ns	Later hit on same channel <i>OR</i> First hit on next (higher) channel

Hit Data Word for Chicago TDC				
	<b>Channel m, Hit j</b> $0 \leq m \leq 95 \quad 1 \leq j \leq 7$		<b>Channel m, Hit j+1</b> <i>OR</i> <b>Channel m+1, Hit 1</b>	
<b>Bits</b>	<b>31-24</b>	<b>23-16</b>	<b>15-8</b>	<b>7-0</b>
	Time (count)	Width (count)	Time (count)	Width (count)
	MAX TIME = MAX WIDTH = 255 * 1.2 ns/count = 306 ns		Later hit on same channel <i>OR</i> First hit on next (higher) channel	

Hit Data Word Definitions		
Time	Width	Definition
1 - MAX TIME	1 – (MAX WIDTH-1)	Complete pulse (leading and trailing edges)
1 - MAX TIME	MAX WIDTH	Unpaired leading edge (no trailing edge found)
0	1 – (MAX WIDTH-1)	Unpaired trailing edge (no leading edge found)
0	MAX WIDTH	Input level “high” over possible width range

**Notes**

- The channel and hit time order within the hit data blocks are identical for both TDCs.
- The Chicago TDC reported time/width is in counts – 1.2 ns/count.
- When there are an odd number of hits, the last word in a hit data block will contain 0 (Michigan) or data from a previous event (Chicago) in the lower 16 bits.
- Michigan TDC DSP code V61 does not implement the described time/width packing, but it has been partially implemented and tested in development code.
- The Chicago TDC currently has a different channel/time order, but Mircea has indicated the above order can be implemented easily. (Bit swaps in TDC FPGA)

Hit Count Word								
Bits	31-28	27-24	23-20	19-16	15-12	11-08	07-04	03-00
Channel # modulo 8	7	6	5	4	3	2	1	0

**Notes**

- Each channel hit count has 4 assigned bits, but only the lowest 3 bits are needed since the maximum # hits / channel is 4.
- The Chicago TDC uses the uppermost for each channel to indicate if the channel is enabled (1) or disabled (0).
- The Michigan TDC always sets the uppermost bit to 0 for each channel.

Header Word							
Bits	31-23	22	21	20	19-18	17-8	7-0
	Module ID (User-Specified)	TDC type 0 = Michigan 1 = Chicago	Chip number 0 for TDC type = 0 0/1 for TDC type = 1	Unused always 0	L2 buffer number (0-3)	# hits in hit data block	Bunch Crossing Counter

**Notes**

- The Module IDs are the same as those specified in CDF note 4152.
- The TDC type simply distinguishes between the two TDC types.
- The chip number is relevant for the Chicago TDC only.
- The Michigan TDC will implement this format in future DSP code release.
- The Chicago TDC chip FPGA will need modification to implement. It should be easy, but that has not yet been confirmed.

<b>Pseudo-Header Word (Michigan TDC only)</b>							
<b>Bits</b>	<b>31-23</b>	<b>22</b>	<b>21</b>	<b>20</b>	<b>19-18</b>	<b>17-8</b>	<b>7-0</b>
	Module ID (User-Specified)	TDC type 0 = Michigan 1 = Chicago	Chicago TDC chip number 0 or 1 (always 0 for TDC type = 0)	Unused always 0	L2 buffer number (0-3)	Total # words in VME FIFO	Bunch Crossing Counter
<p>The crate CPU reads this special word from static ram during readout. This word differs from the header word only in bits 17-8.</p>							

Assuming max # hits/channel = 4, the maximum amount of data to readout from a given TDC is  $(96 \times 4) / 2 + 12 + 2 = 206$  words. (32-bits in length)