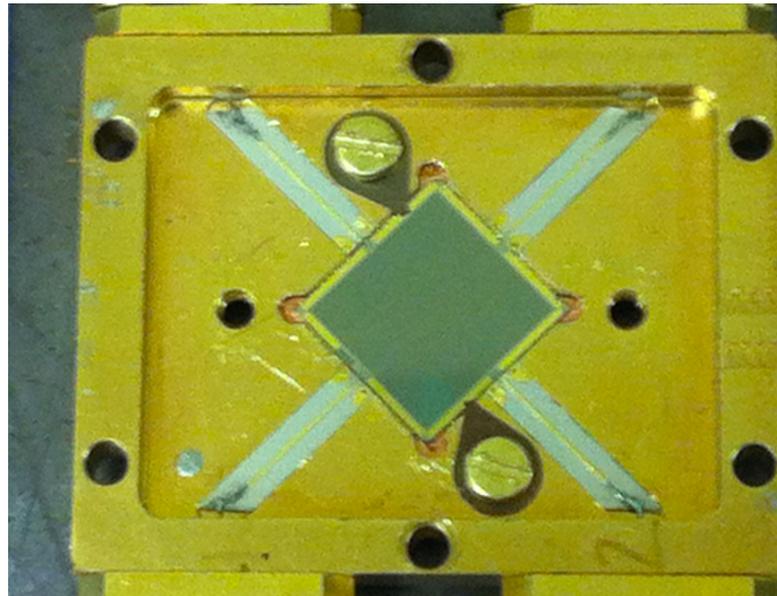


UCSB MKID

Part 2



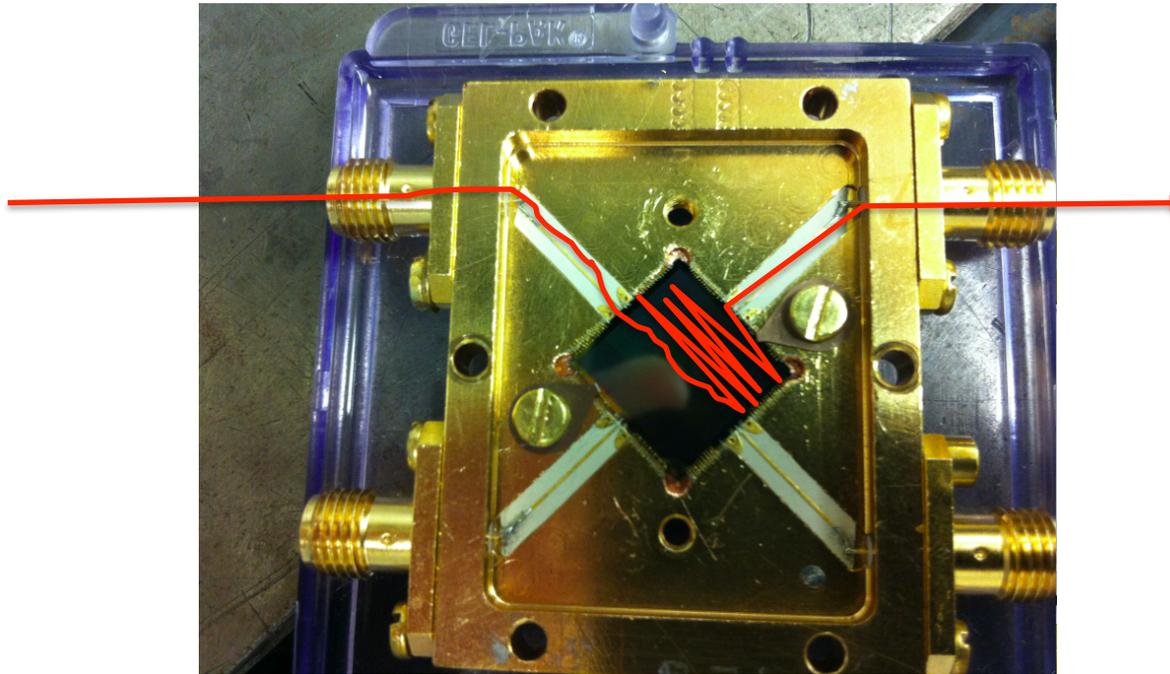
Donna
20Sep2013

Learning about UCSB MKID

- Thank you to Ben and Seth for patiently answering our questions
- This is the second presentation discussing the construction of the UCSB MKID.
- More photos and explanations were presented last week:
<http://projects-docdb.fnal.gov:8080/cgi-bin/ShowDocument?docid=2656>

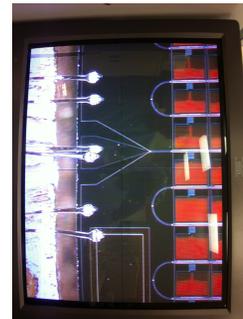
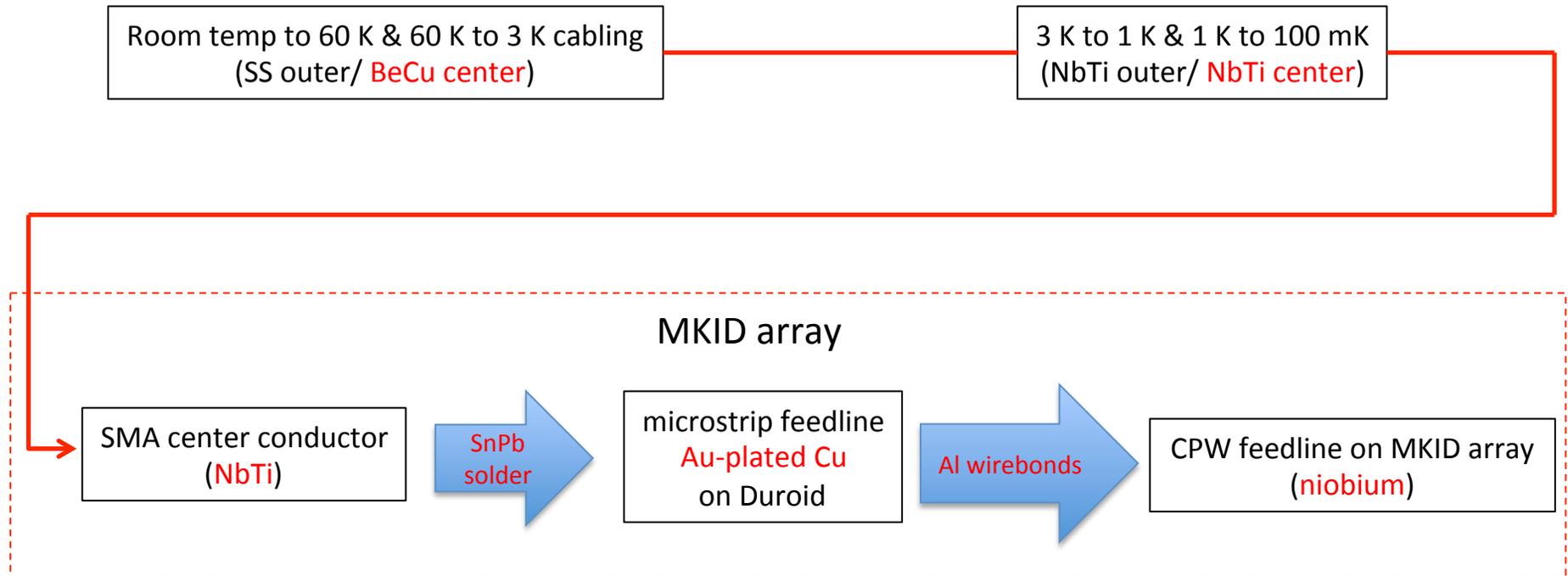
Feedlines

GOAL: Understand the path of the RF signal and the materials that carry the signal



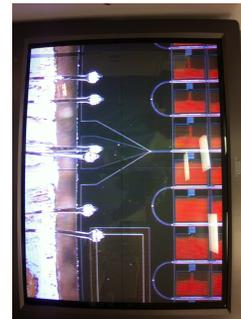
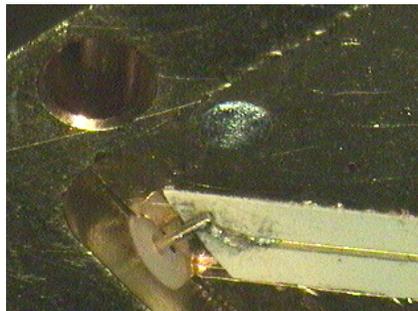
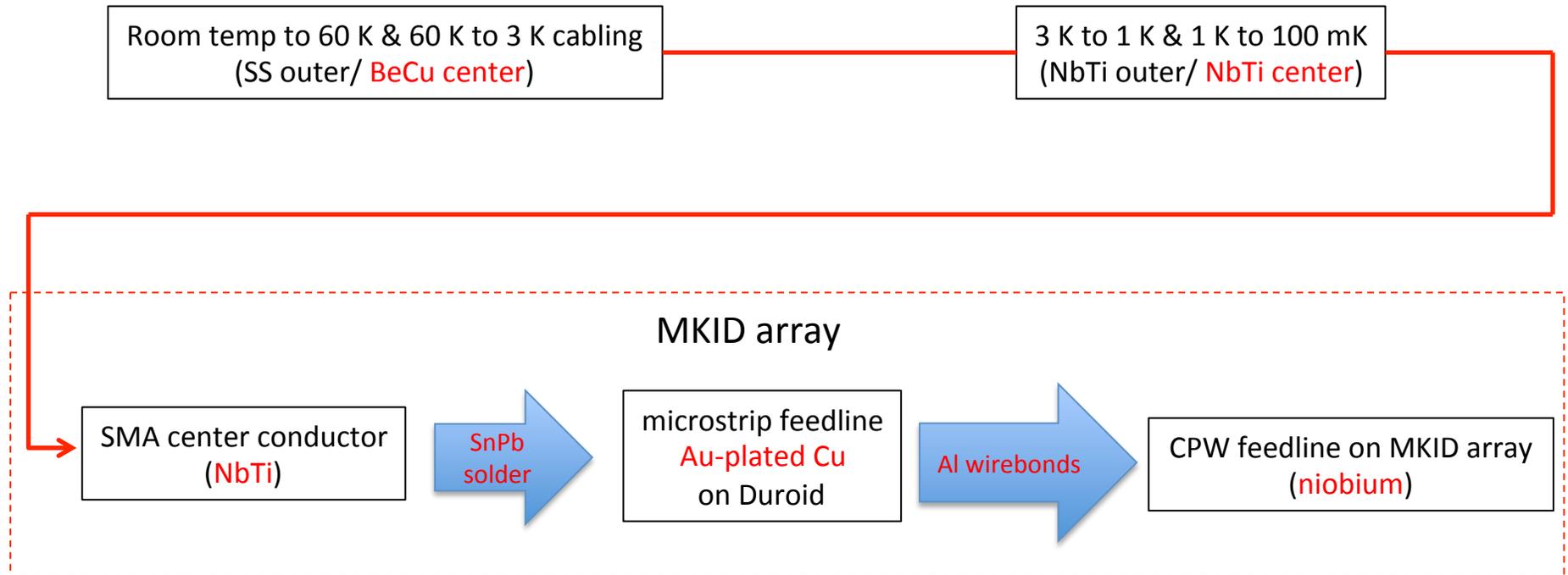
Feedlines

GOAL: Understand the *path* of the RF signal and the *materials* that carry the signal



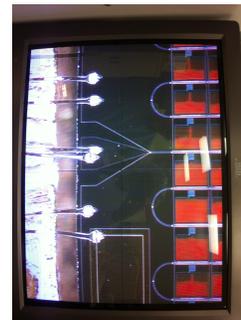
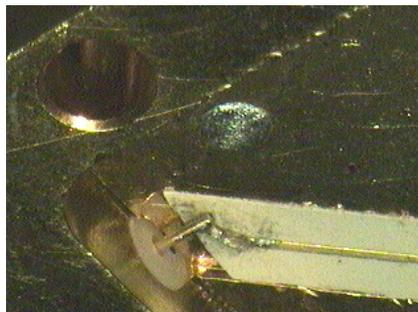
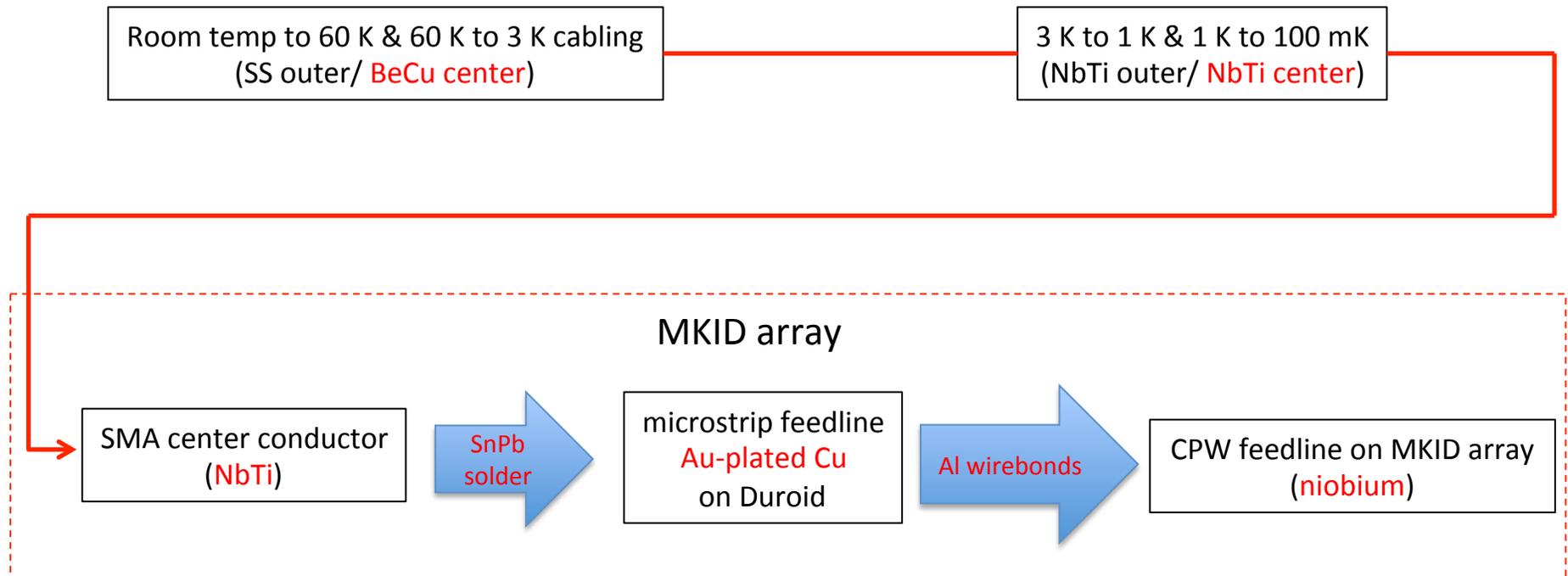
Are these the coax cables you use?

SETH: Yes, those are the coax we use for both of those stages. The 100 mK ones are a smaller diameter than the warmer ones, if I remember correctly. If you need the dimensions I will have to look those up.



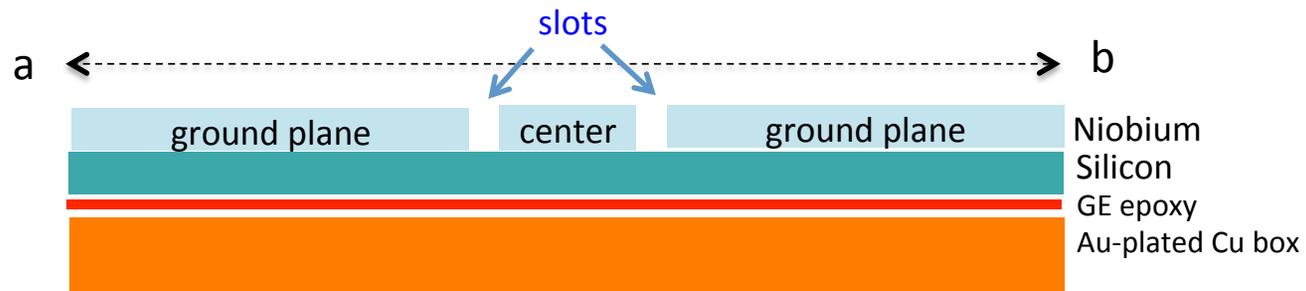
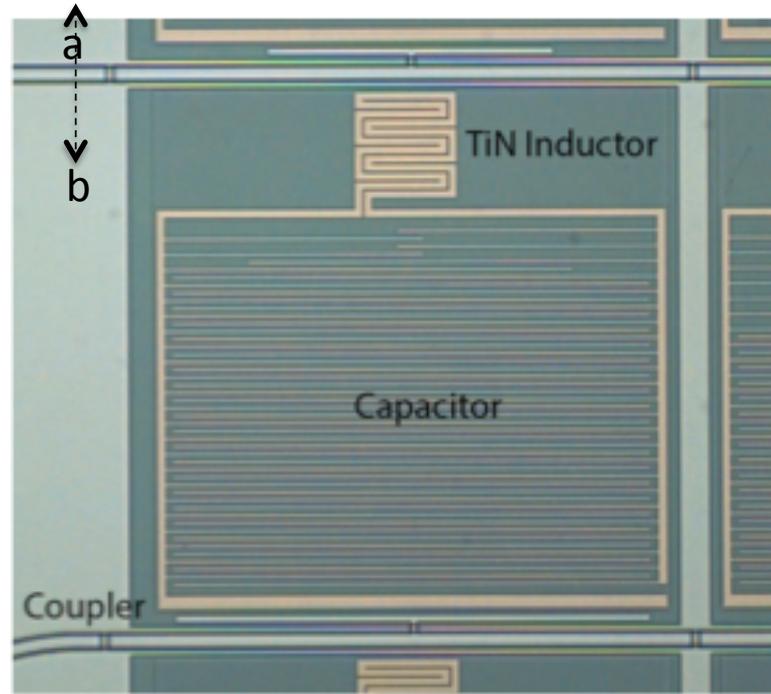
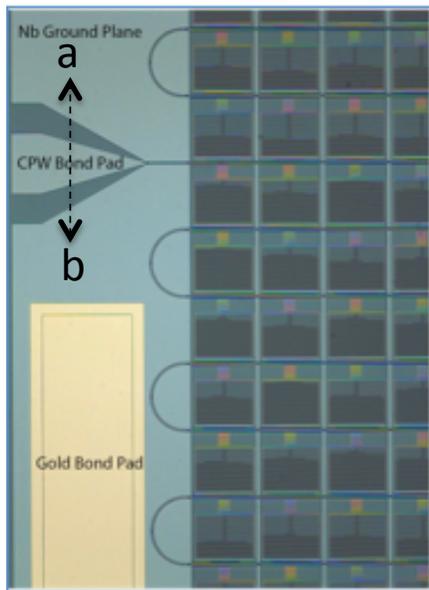
Is it OK to use Al wire to bond to Au and Nb?

SETH: We typically use Al wirebonds, and had been using them exclusively until recently. Using the Al to connect the Au on duroid microstrips to the Nb on the MKID is not a problem.



What is the construction of the CPW?

SETH: CPW is Nb ground plane with Nb center and bare Si in the slots.
Your cross-section drawing looks perfect. :-)



What are the white outlines?

SETH: The white appears to be highlighting the edges of the metal films. Everywhere I see a white line on the chip is where there is some step in film thickness. So the white that traces the feedline is due to the very small Si slots between the Nb center and ground layers.

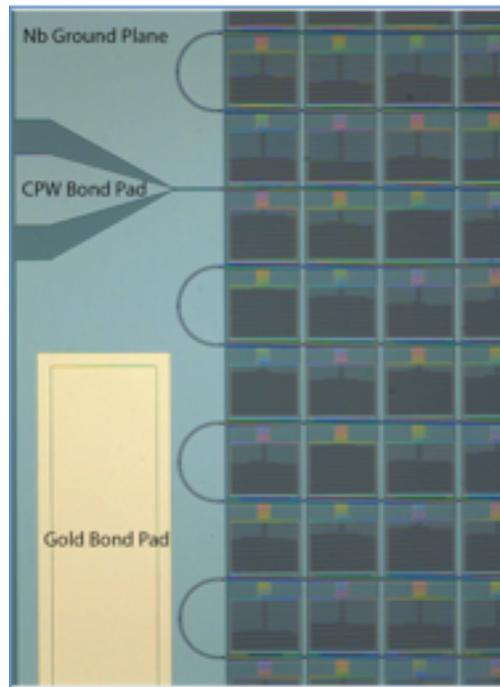
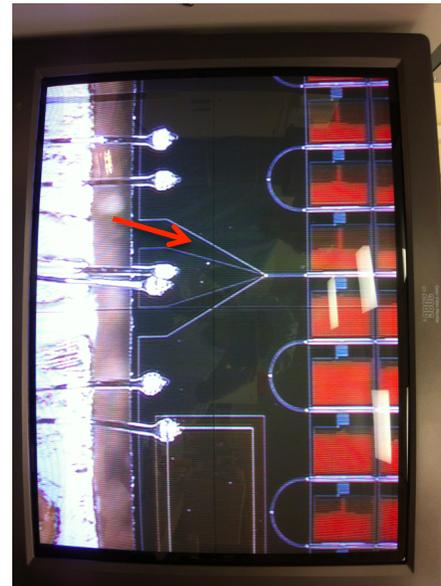


Image from Seth's MKID workshop talk



Zeiss + iPhone photo

What is the big Gold Bond Pad for?

SETH: We introduced the Au wirebonds though when it appeared that thermalization was a problem. Regarding the gold bond pads: They are part of the ground plane (overlapping the Nb ground plane) and there we use gold wirebonds to connect the gold plated box to the gold pads on the chip. This was done to ensure better thermal contact with the chip.

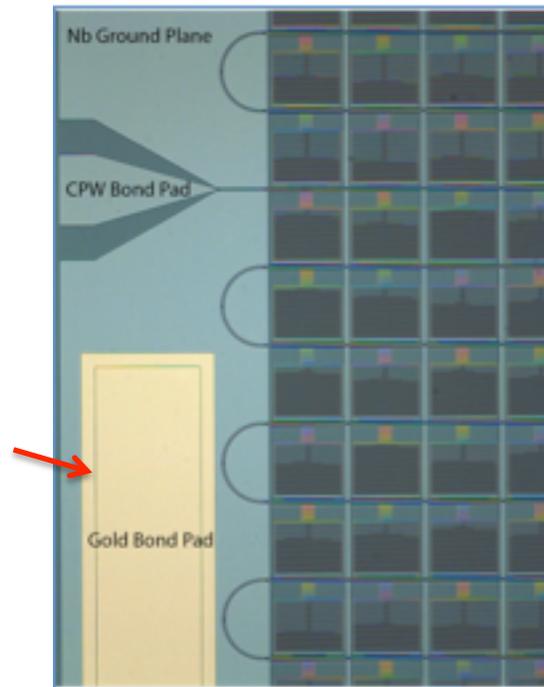
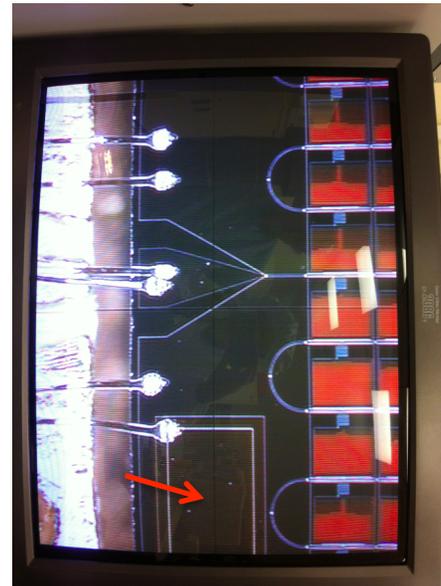


Image from Seth's MKID workshop talk



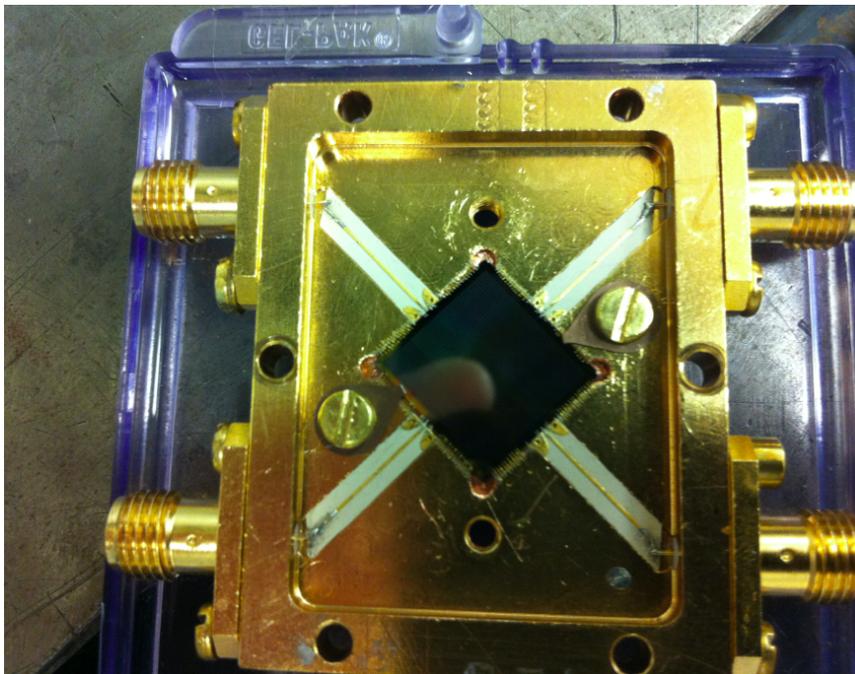
Zeiss + iPhone photo

What are these circles?

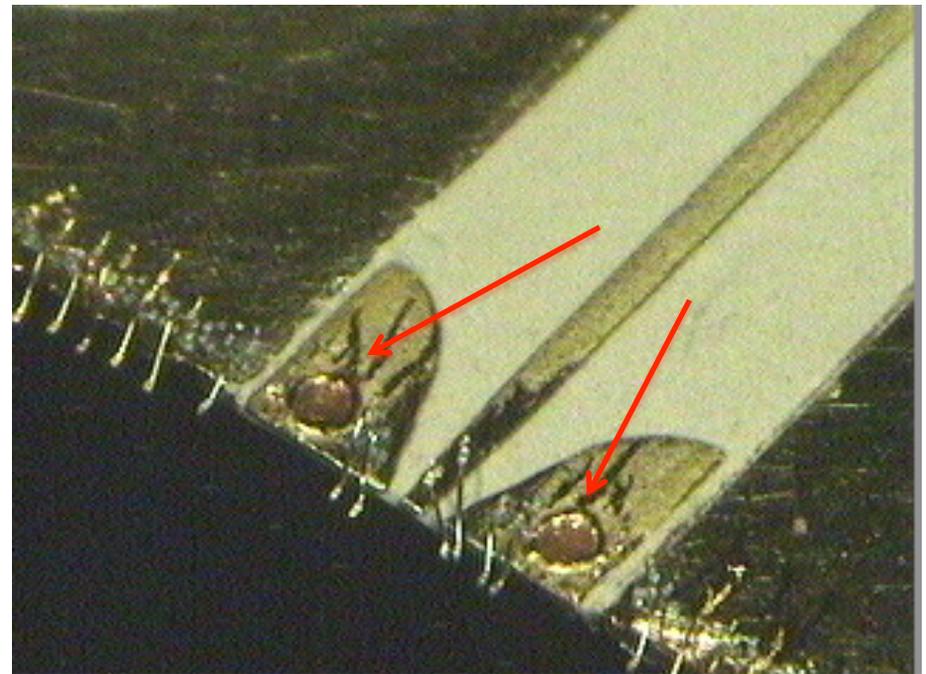
SETH: Those holes are feed-throughs to the gold on the back of the microstrip which is the connection to ground. Since the ground plane on the chip cannot be wirebonded to backside of duroid microstrip, those feedthroughs let us bond to the topside ground pads on the duroid and then connect through to the bottom (see next slide)

Q : But there are wirebonds to ??? – they don't connect to GND?

Q: How is microstrip connected to box – GE varnish?



iPhone photo

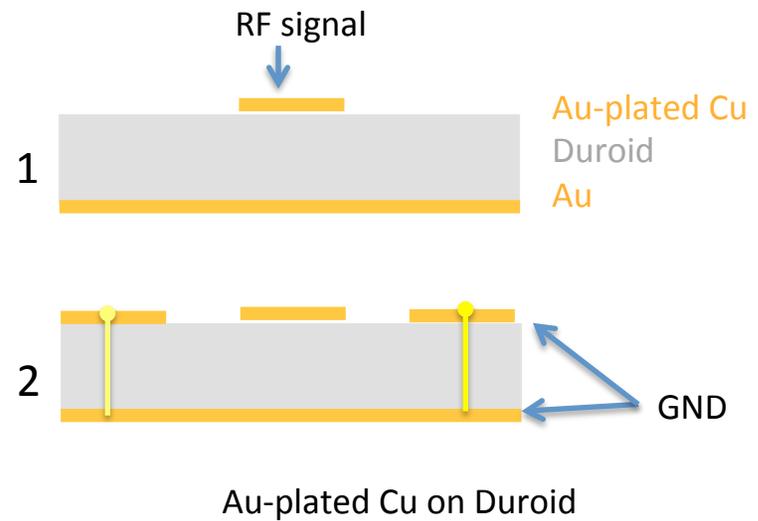
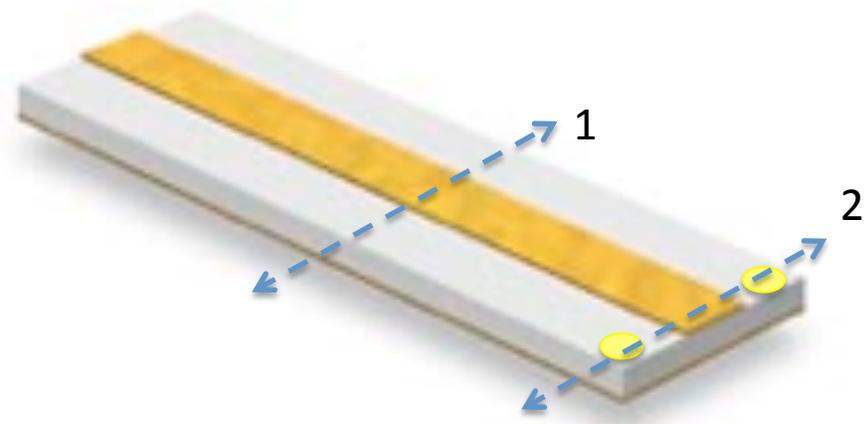
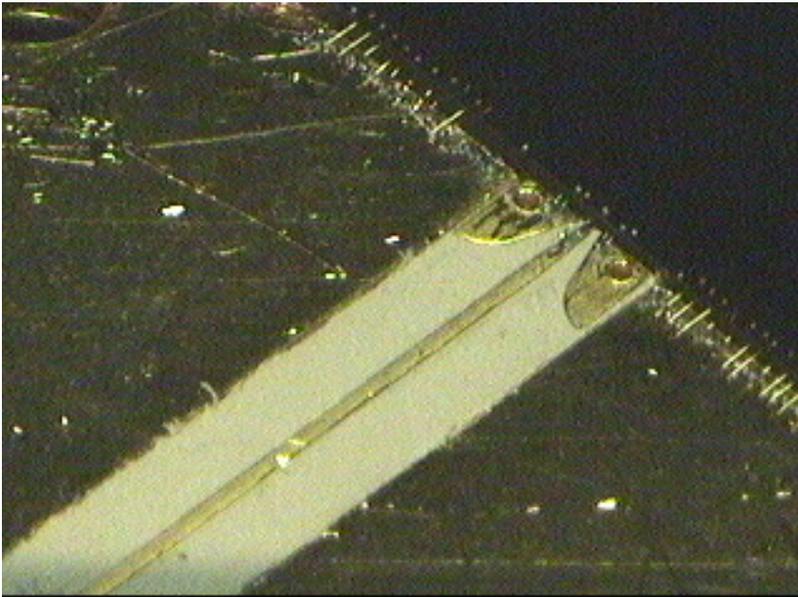


Techno-Look photo

Microstrip Transmission Lines

Duroid is a trademark of Rogers Corp

- RT/duroid high frequency circuit
- materials are filled PTFE (random glass ceramic) composite laminates



Review of a few comments from Ben at last week's meeting

GE varnish has poor thermal conductivity so the gold bonds (slide 10) are important!

- GE varnish does not have good thermal conductivity

Specifications

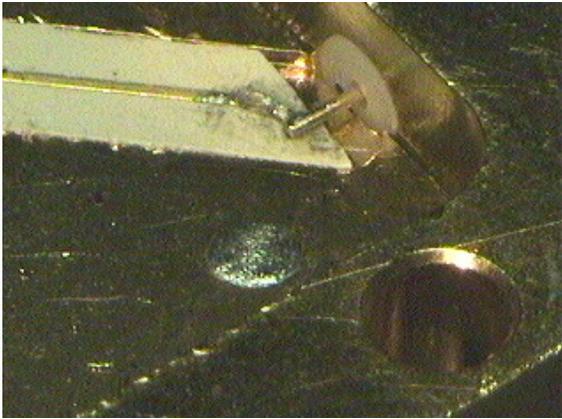
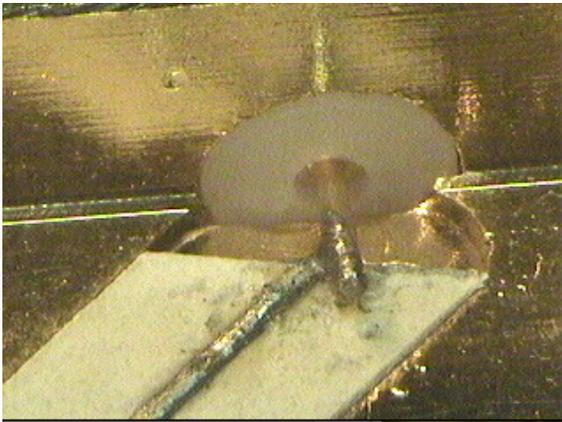
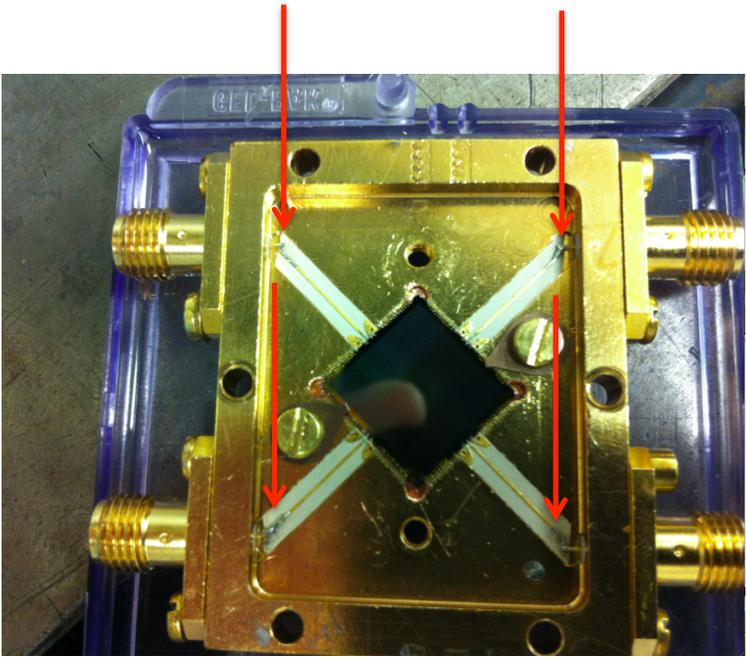


	Conductive Epoxy	Stycast® Epoxy	Apiezon Grease		Varnish
			Type N	Type H	
Max temperature	573 K	403 K	316 K	523 K	423 K
Thermal conductivity					
1 K	—	0.0065 W/(m · K)	0.001 W/(m · K)	—	0.034 W/(m · K)
4.2 K	—	0.064 W/(m · K)	0.005 W/(m · K)	—	0.062 W/(m · K)
77 K	—	—	—	—	0.22 W/(m · K)
100 K	—	—	0.11 W/(m · K)	—	0.24 W/(m · K)
300 K	1.7 W/(m · K)	1.3 W/(m · K)	0.26 W/(m · K)	0.22 W/(m · K)	0.44 W/(m · K)
Thermal expansion (1/K)	>360 K: 150×10^{-6} <360 K: 43×10^{-6}	29×10^{-6}	0.00072	0.00072	—

Material Properties	Phosphor bronze	Copper	
Melting range	1223 K to 1323 K	1356 K	
Coefficient of thermal expansion	1.78×10^{-5}	20×10^{-6}	
Chemical composition (nominal)	94.8 % copper, 5% tin, 0.2% phosphorus	—	
Electrical resistivity (at 293 K)	11 $\mu\Omega\cdot\text{cm}$	1.7 $\mu\Omega\cdot\text{cm}$	
Thermal conductivity (W/(m·K))	0.1 K	NA	9
	0.4 K	NA	30
	1 K	0.22	70
	4 K	1.6	300
	10 K	4.6	700
	20 K	10	1100
	80 K	25	600
	150 K	34	410
	300 K	48	400

Compare to thermal conductivity of Phosphor Bronze (quad wire) and Cu, for example.

SMA to stripline PbSn solder connection is the most likely point of failure
(Check first if you have problems!)

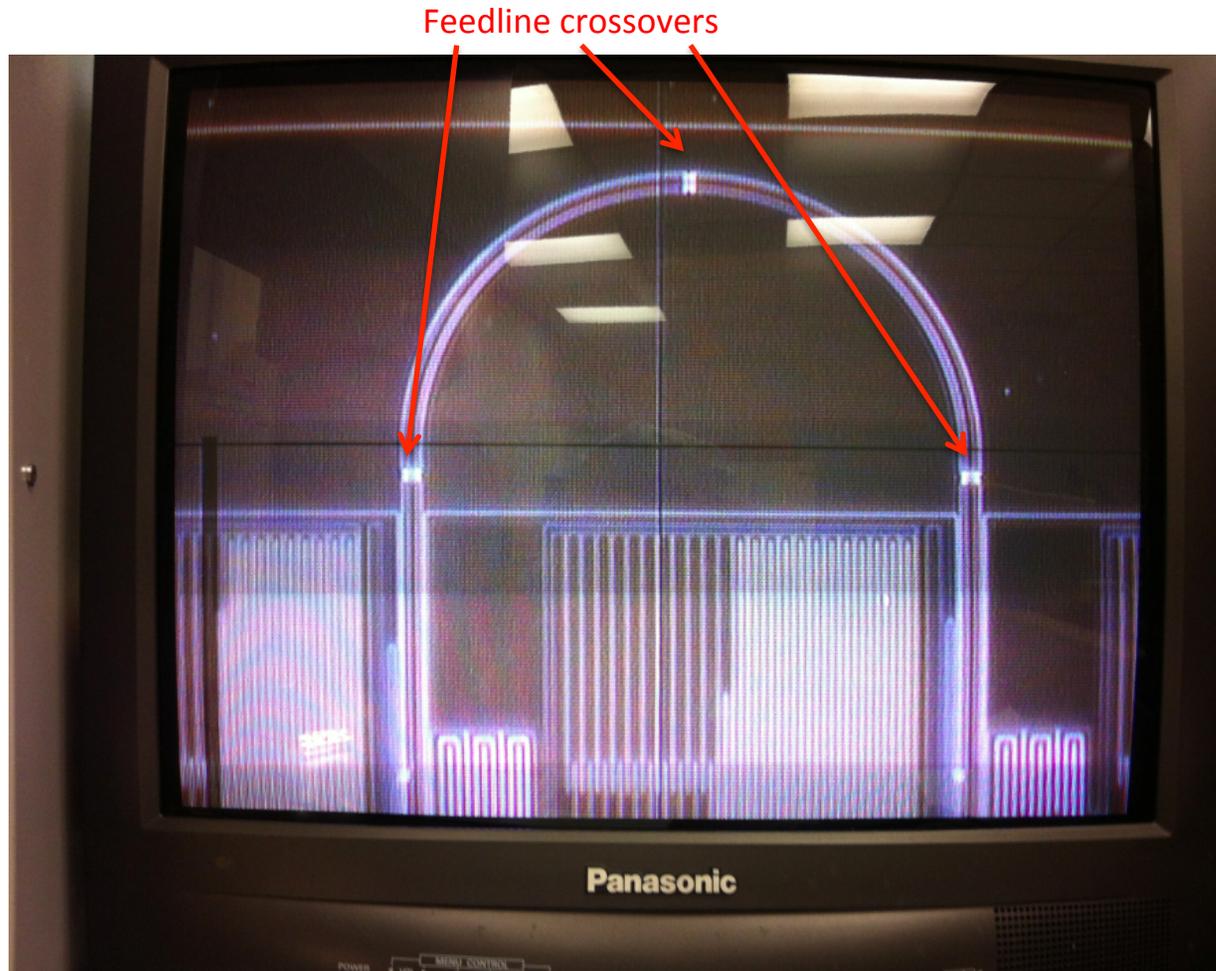


Feedline crossovers (shown on next 2 slides)

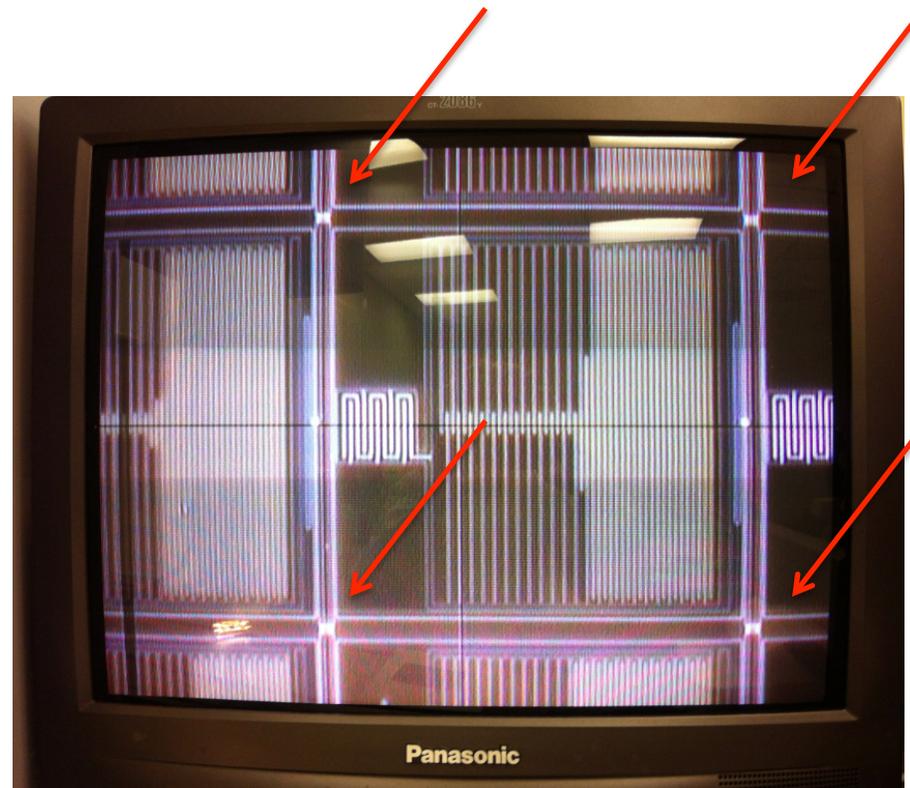
- The feedline crossovers help suppress different modes, as the slotline mode.
- The feedline crossovers are perhaps the most difficult part of the fabrication.

Feedline crossovers

These serve to connect the ground plane across the chip into one big ground plane instead of a bunch of separate ground planes.



More feedline crossovers



thank you