TDC Readout and the CDF DAQ

Arnd Meyer
Fermilab
May 23, 2002

- Implementation of the TDC readout in the CDF DAQ
- Current performance
- Limitations and potential improvements

See CDF notes 5824 (5889 for COT occupancy) for details, but most of what I show today is updated and new information

Introductory Remarks

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Fermilab
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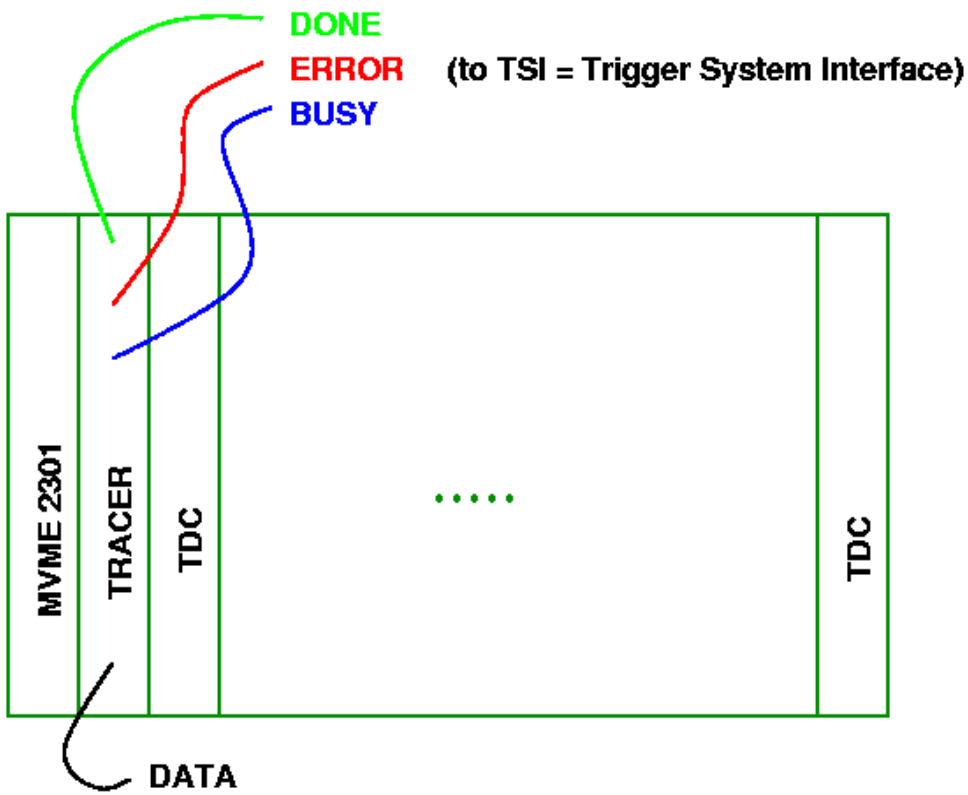
- Will not talk about muon TDC's, CLC TDC, hadron timing TDC's
  - In general much lower occupancy
  - Not as much looked at
- Spares are a major concern, but not for this talk
- Crate layout: MVME2301 + TRACER + ~16TDC's (+ DAC + FADC)
  - FADC's are assumed to be relocated. Most data shown here are without FADC's

- To run at 1kHz, the slowest crate needs to return DONE after 500μs
  - After DONE has been returned, the corresponding L2 Buffer can be reused by the TSI
- Crates contain a mix of inner and outer superlayer channels
  - All crates behave similarly in readout



1kHz L2A

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Fermilab
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- TDC's are the only component that does significant processing after the L2 accept
- TDC's are the only component showing a significant dependence of processing time / data volume as a function of luminosity
- All other boards/crates have a straightforward upgrade path to 1kHz
  - Zero suppression, and/or more compact data format
  - Faster crate controllers
  - Drop "diagnostic" data unless required ("readout lists")

1kHz L2A

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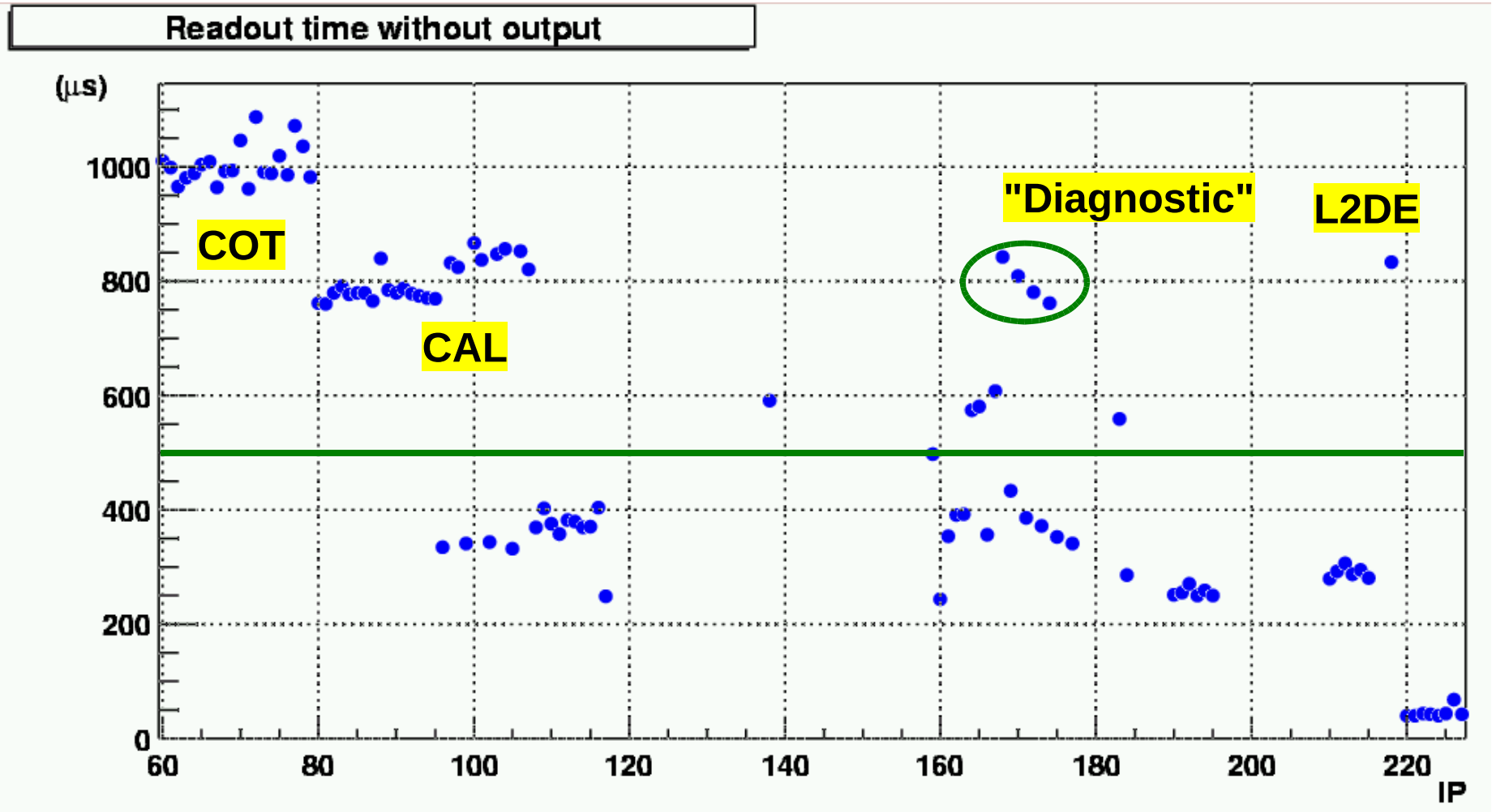

TDC Readout ("Global DONE")

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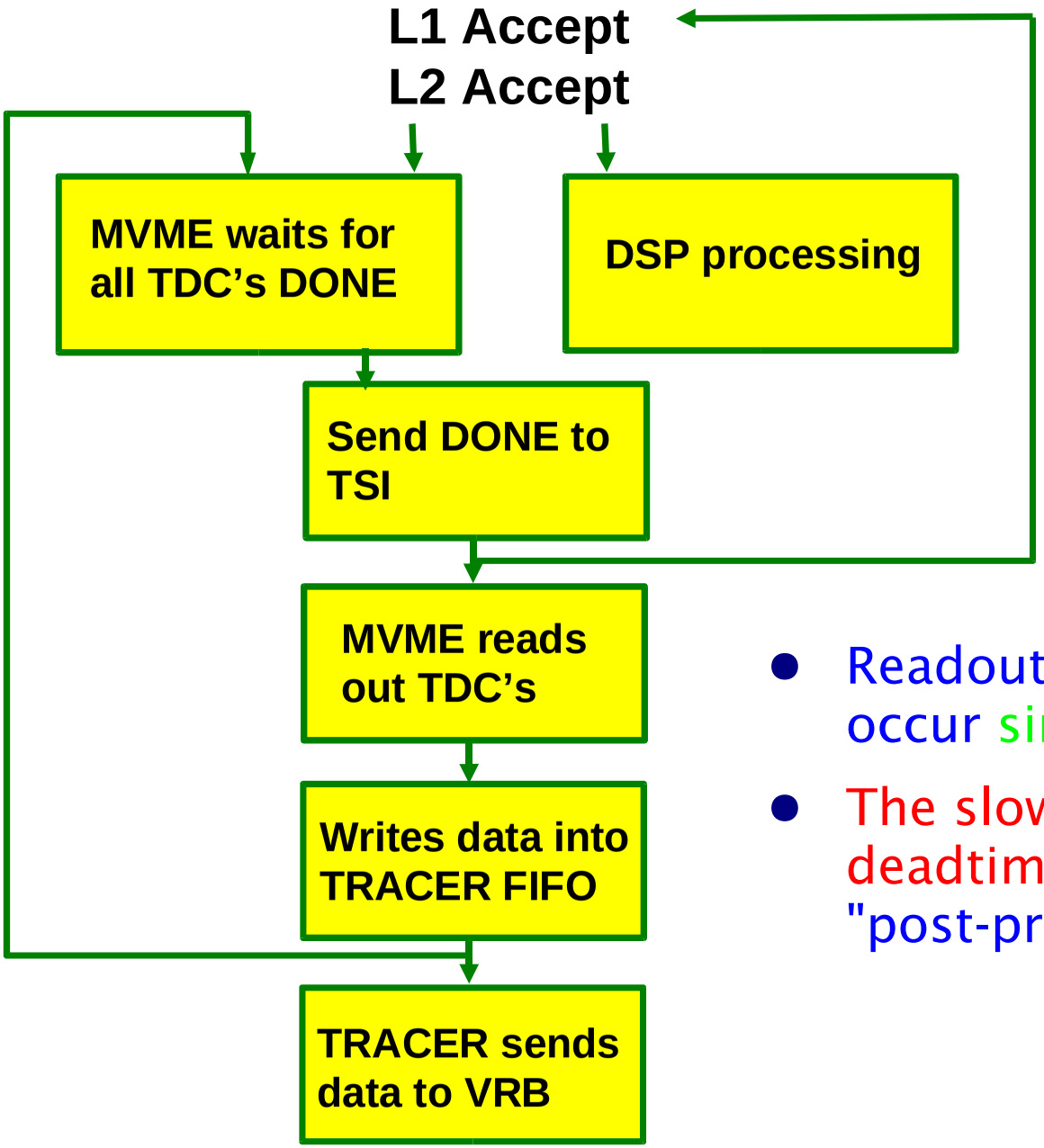

- Readout and DSP processing can occur simultaneously - do they?
- The slowest TDC DSP determines deadtime (or the crate with most "post-processing"?)

Another TDC Readout ("Local DONE")

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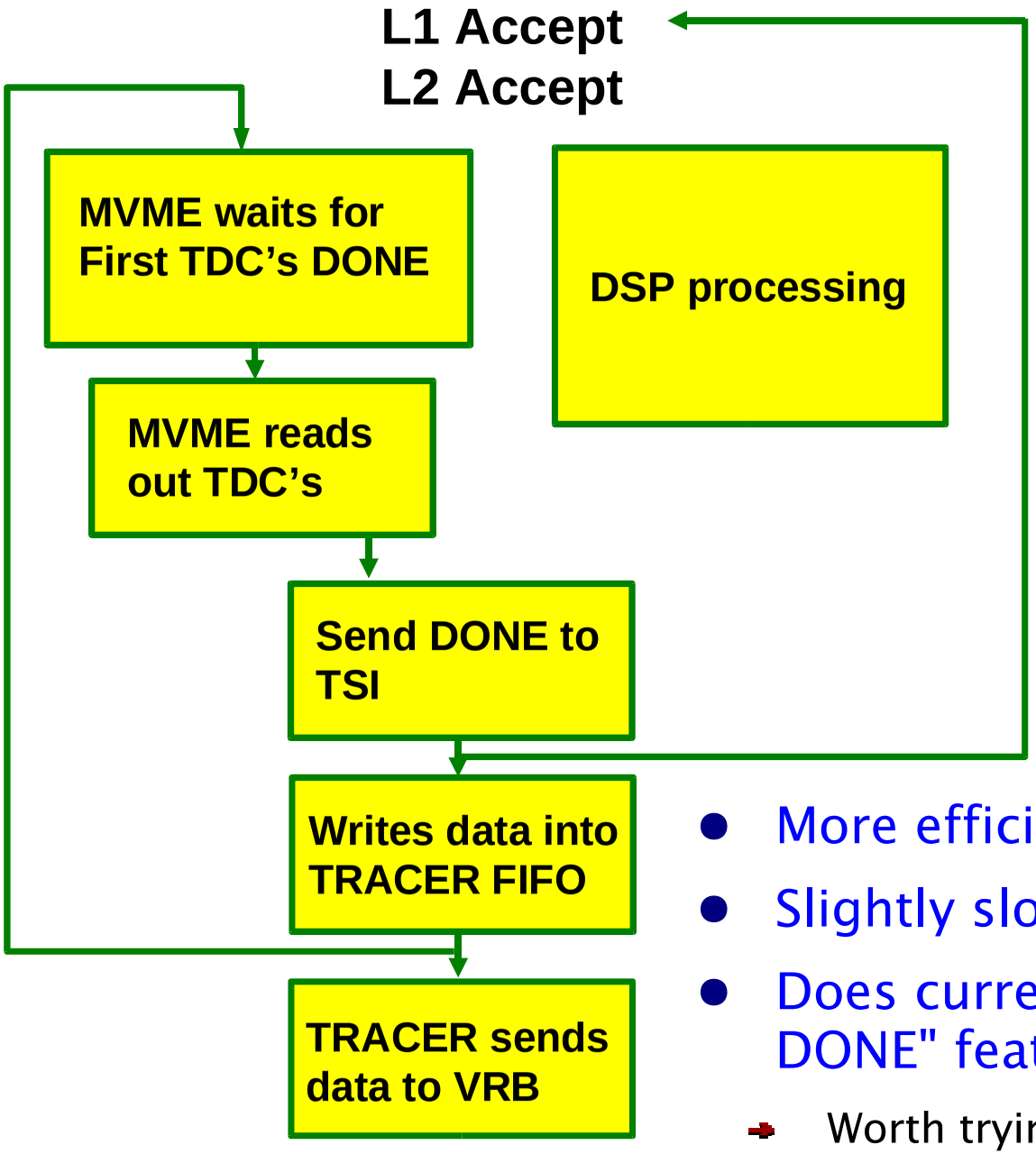

- More efficient utilization of crate CPU
- Slightly slower than default
- Does currently not exploit "Early DONE" feature
  - Worth trying

Measurements

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- Two main methods to establish readout performance here:
- Event-by-event, the crate controller takes timing measurements at five strategic points in the readout
- The TSI scalers record the average time that is spent in the DONE handshake ("Readout Latency")
  - How long is a certain L2 buffer unavailable because of readout?
  - Obviously only useful here when the COT crates are the slowest in the DAQ
- From "Readout Latency" to maximum rate with acceptable deadtime:

$$f \approx \frac{1}{(2...2.5) \times \text{readout latency}}$$

(Note that this agrees pretty well with the Yale group simulations, ~450μs for 1kHz)

- Some dependence on L2 latency and L1 accept rate
- Some dependence on trigger mix, and special configurations (recently much data without Silicon → fewer track triggers)

Basic Numbers

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- Single-word reads (already optimized routines): ~3.5μs
  (at most x2 faster possible)
- Block transfers from TDC board: ~14MB/sec
  write to TRACER FIFO: ~12MB/sec
  r/w MVME: ~20MB/sec
- Ideally, readout itself takes 32x3μs + 2.5kB / (14MB/sec) ≈ 280μs
- On average, at current luminosities ($1.5\text{-}2 \cdot 10^{31} cm^{-2} s^{-1}$):
  - 400-450μs DSP processing time for the slowest TDC in a crate
  - 600-650μs DSP processing time for the slowest TDC overall
  - ~500μs readout time (TDC's → MVME)
  - 200-250μs writing data back into TRACER FIFO (MVME → TRACER)
  - ~100μs overhead (check data integrity, assemble bank header, etc.)
- All numbers except "overhead" increase with luminosity

Readout Latency

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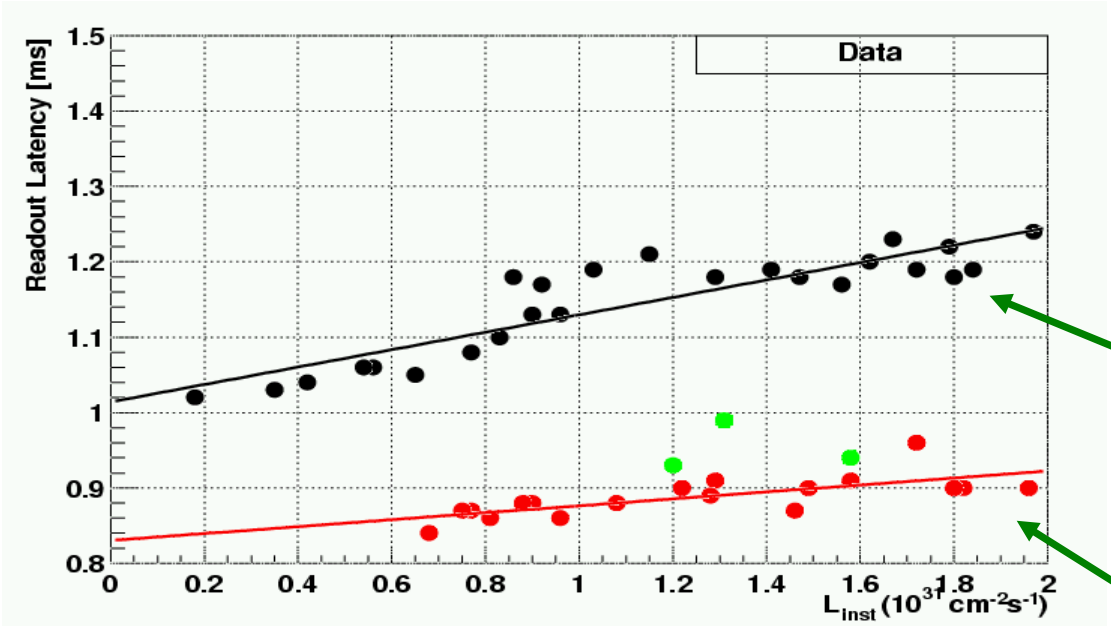

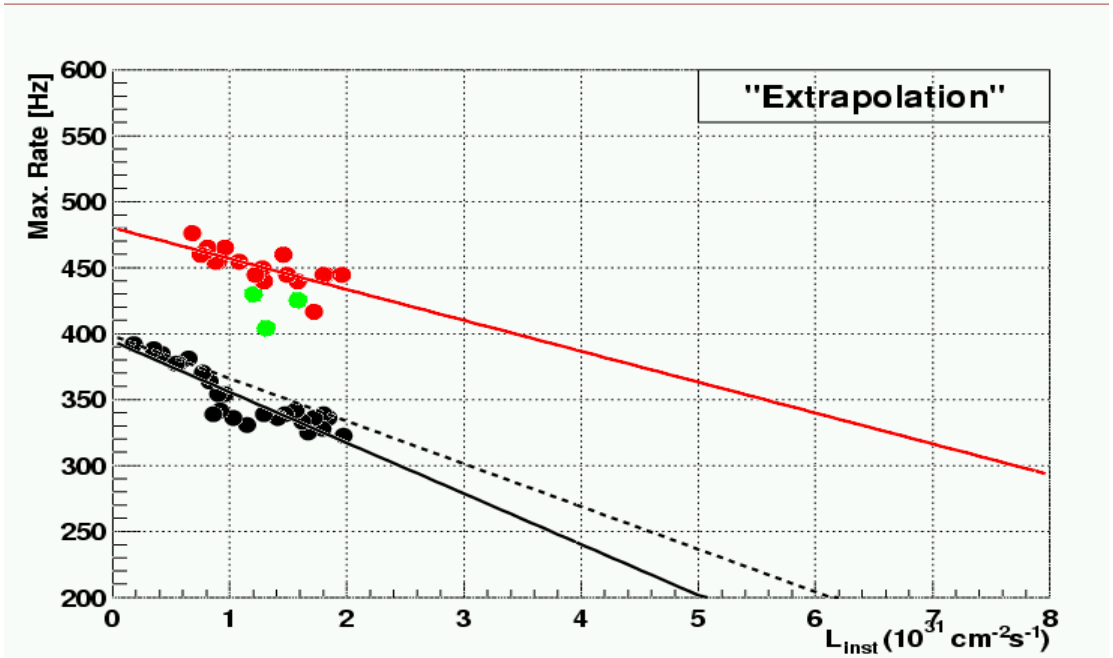

Measured by the TSI scalers, this is the relevant number for overall performance

Default readout for some time. Almost only COT crates contribute to the black points.

Current fastest: all crates using "global" DONE, FADC's out of readout.

Red points are dominated by non−COT crates → don't rely on the shape!

Sanity Check

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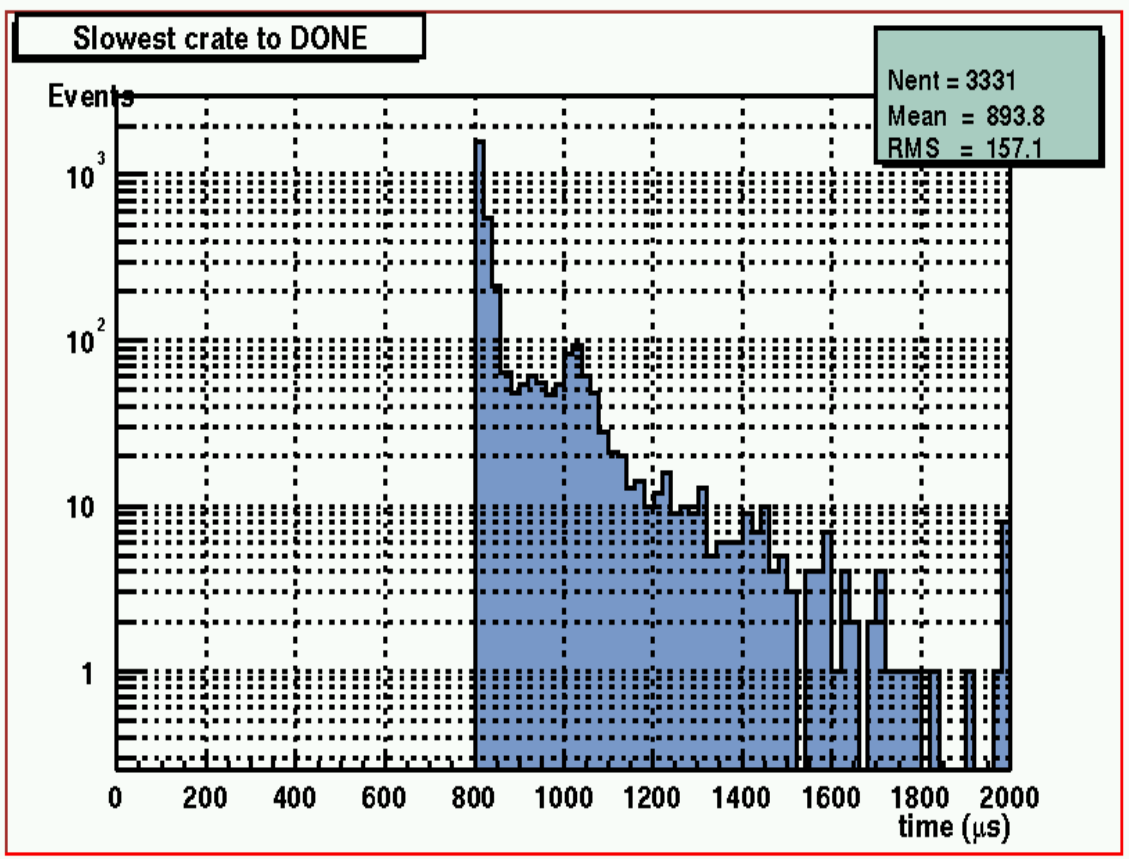
- Compare latency seen in TSI with measurements in ~100 CPU's: good agreement, Scaler number typically ~30μs high (includes effects of e.g. DONE timeouts, front-end errors)



crate CPU: **894μs**

TSI scalers: **909μs**

DSP Processing

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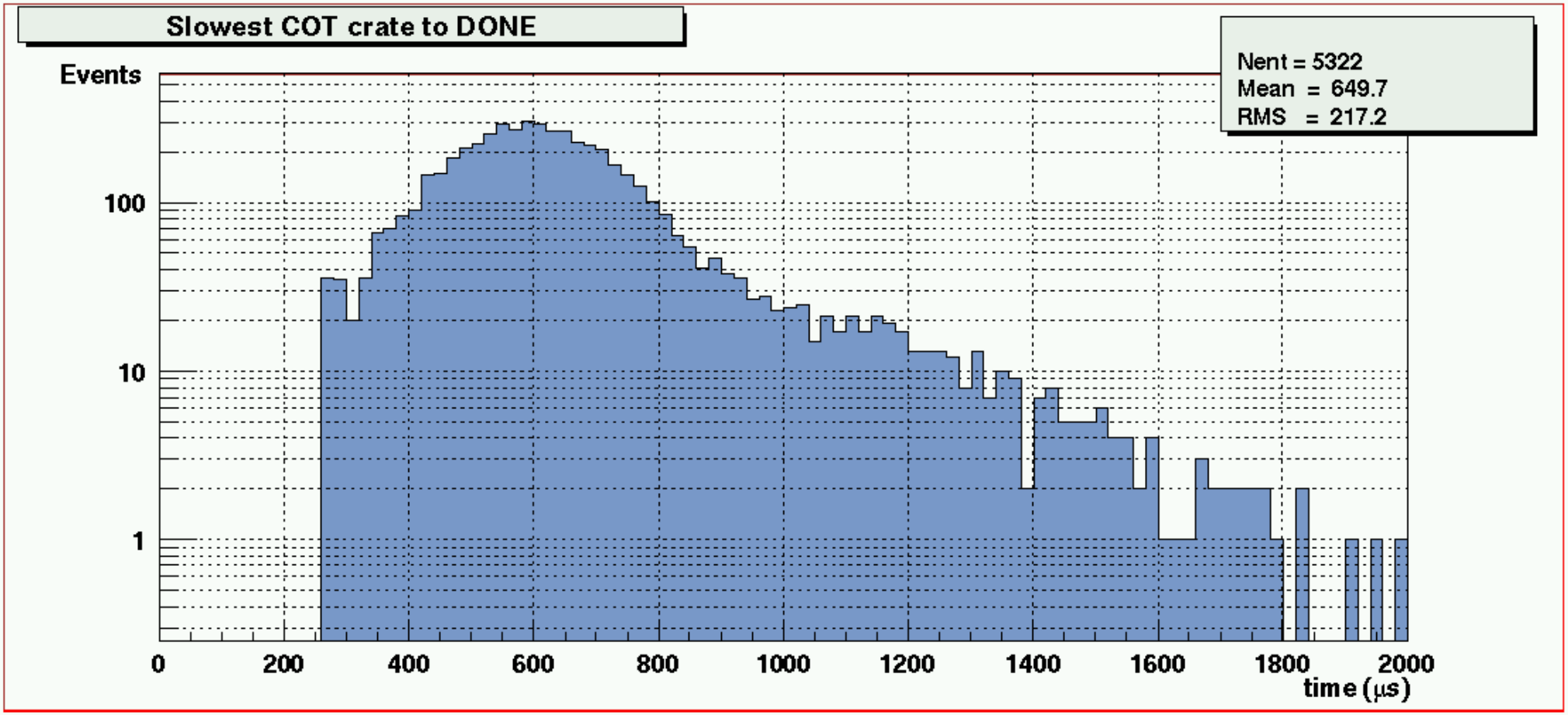
Run 145023, L~2•10^{31}cm^{-2}s^{-1}, no Silicon



DSP− or Post−Processing?

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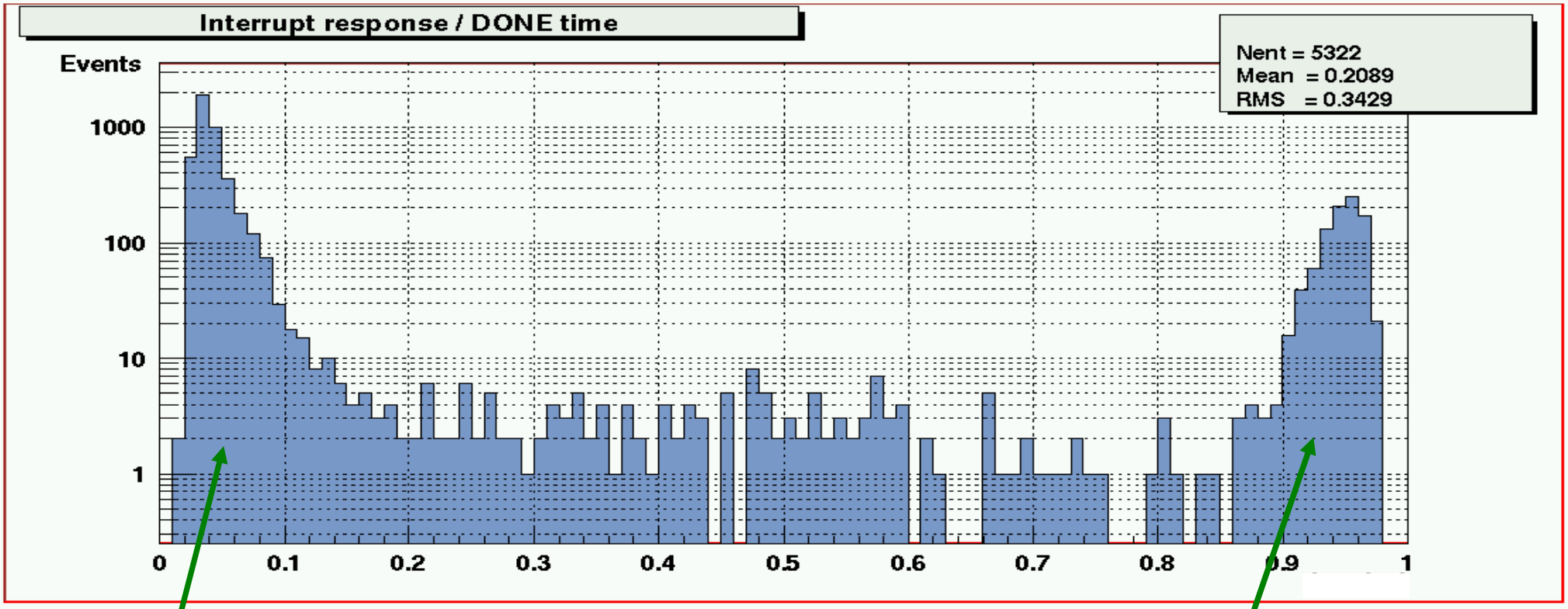
- Readout of previous event and DSP processing can proceed in parallel
- For slowest COT crate to return DONE: $\frac{\text{time until CPU starts processing a L2A}}{\text{total time until DONE}}$



Post−processing finished first

DSP finished first

Higher rate at same luminosity → shift to the right
(but not necessarily at higher luminosity)

DSP Processing vs. Luminosity

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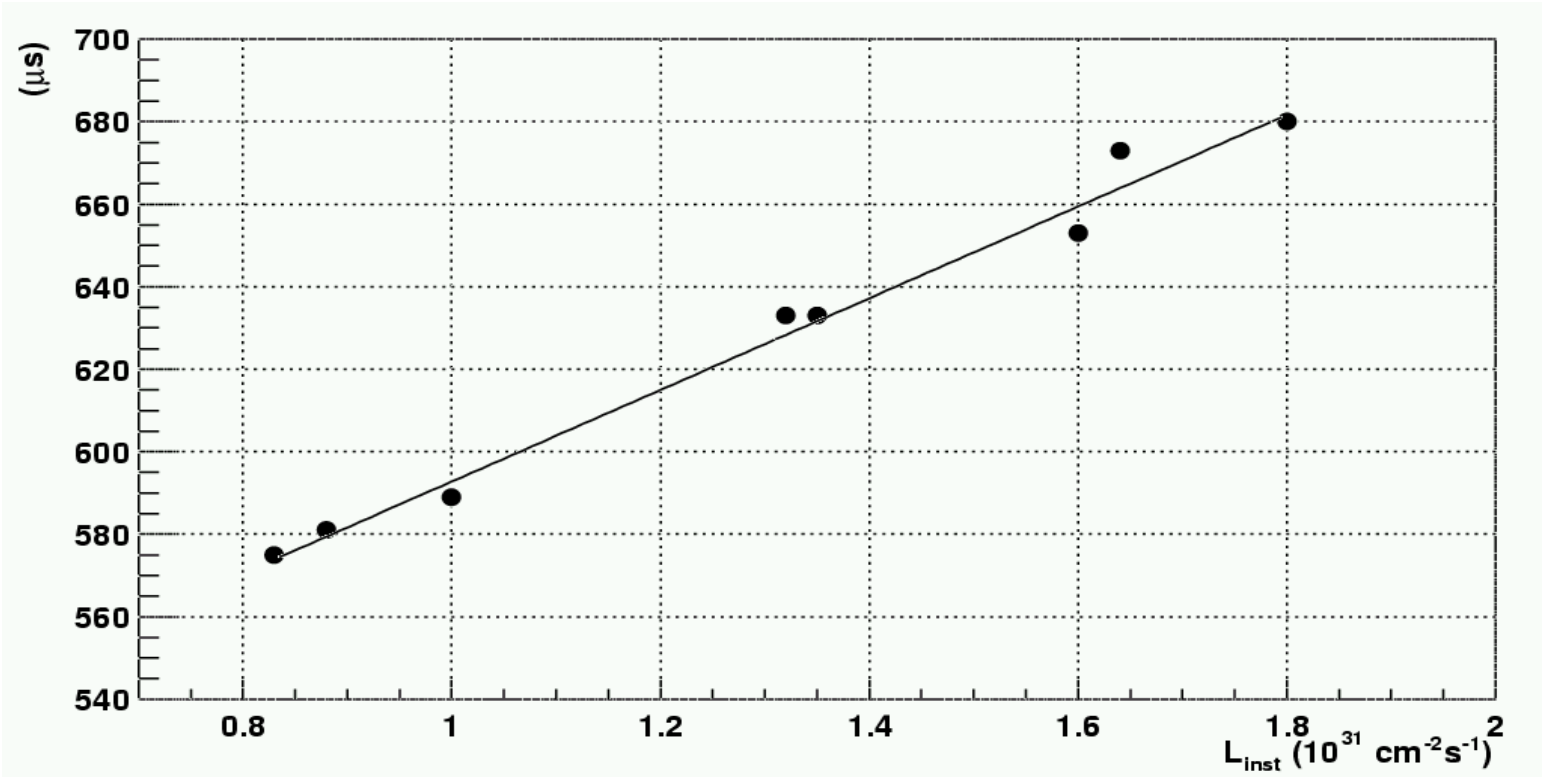

- Some "contamination" from events where postprocessing is slower than DSP-processing

Output Time

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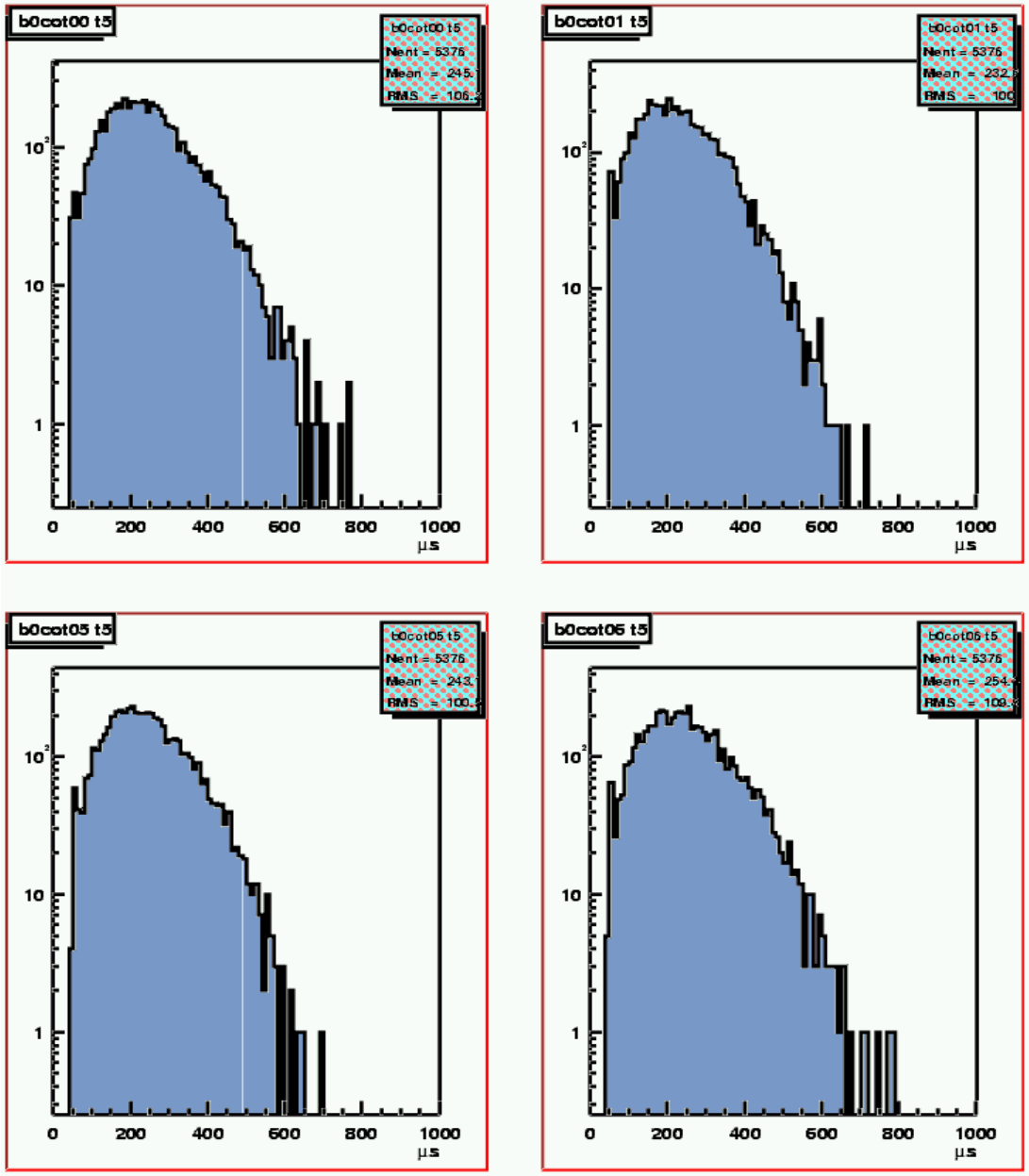
- Basically the time it takes to write the data at ~12MB/sec into the TRACER event FIFO (limited by TRACER VME interface and TAXI link)
- On average approaching ~250µs now
- This can be eliminated with "Spy Mode" (but some overhead added)
- DONE has been returned at this point in time → gain depends on how much DSP processing for the next L2A overlaps



Overall Readout Time

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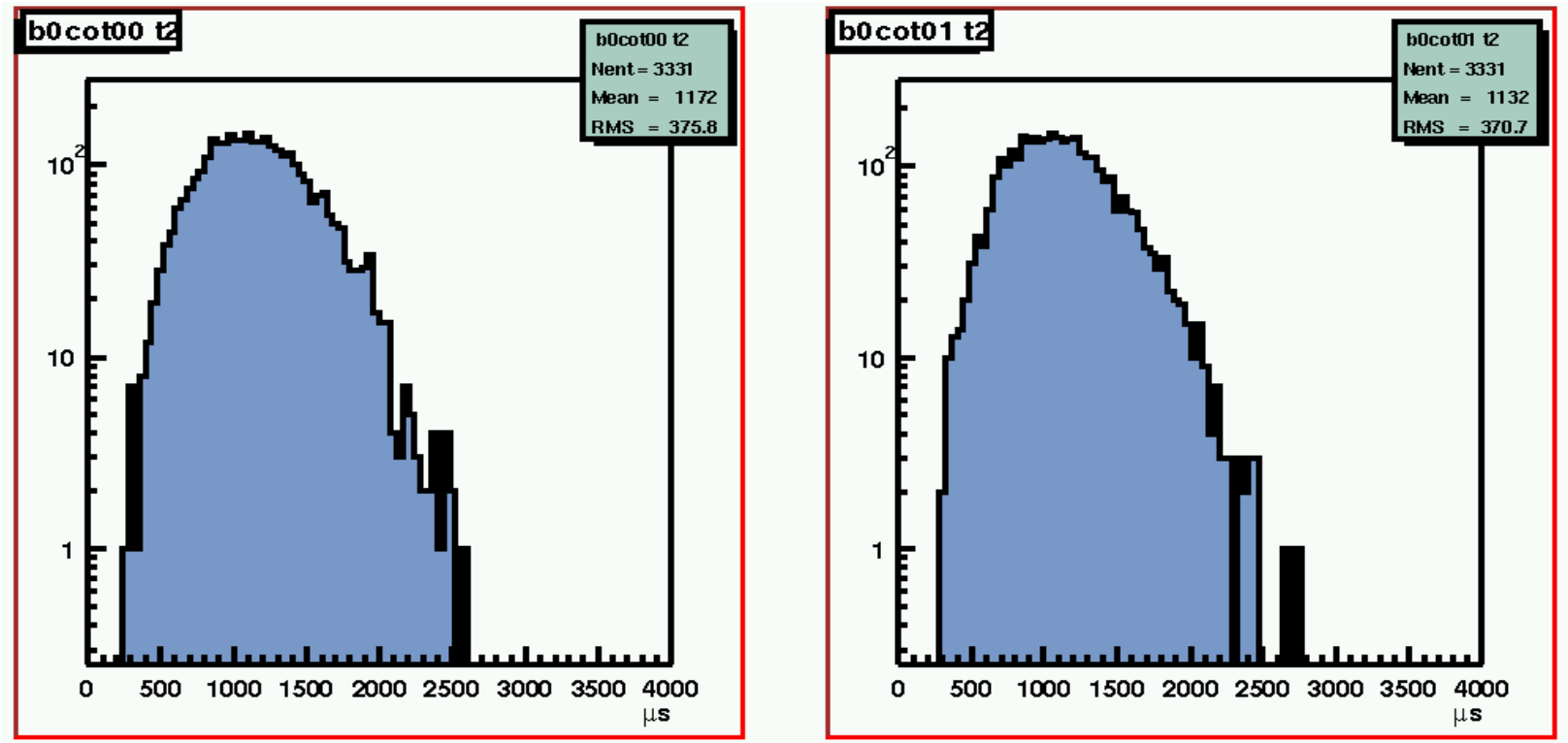
- Adding it all up... this should probably be of the order of 600μs for 1kHz readout rate
- Was never simulated



Some Popular Misconceptions

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- "The TDC DSP processing time can always be hidden behind the MVME readout time"
  - Assume a Minimum-Bias event followed by a ttbar event - the readout of the MBIAS event will long be finished while the DSP is still attacking the 3-hits-per-channel of the ttbar event
- "Spy-mode will improve the readout by a factor of 2"
  - More like "up to 20%": the DSP processing time remains unchanged, and the gain is only in the one single block transfer to the TRACER FIFO, all the smaller transfers from the TDC's remain

Features not working

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- Dual-ported event FIFO
  - The crate controller is supposed to be able to read out the TDC event FIFO while the DSP is writing into it
  - Due to the faulty prefetch logic in the VME interface of the MVME, an additional word is clocked out of the FIFO at the end of the readout, thus corrupting the data in the FIFO
  - Workarounds have been thought of (buffer words etc.) but never implemented
  - Likely not worth it (few μs? Maybe should check for worst case)
- Spy mode
  - To reduce overall readout time, the TRACER can be configured to "spy" on the backplane as data are read out by the crate CPU
  - These data then do not have to be written by the CPU into the TRACER FIFO
  - Still have to assemble header information, write header and trailer into the TRACER FIFO

Spy Mode Failures

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Fermilab
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- Other boards (XFT Finders regularly, others for tests) have been read out successfully with Spy mode
- For TDC crates, data are corrupted when using fast (DMA BLT) readout
- Symptom: end-of-event transmitted over the TAXI link after 4 hit words
- (Misleading) In COT crates, the ~4 TDC's closest to the TRACER are not affected. Much less systematic in Muon crates.
- Two theories
  - Backplane noise / reflections
  - TDC→MVME transfer "too fast" for data to be clocked into the TRACER FIFO
- Data corruption also observed with fast memory module, but different pattern.
- Potentially have to modify TRACER's and/or TDC's
- A side note: TRACER does not follow its specs - should actually ignore data at TDC FIFO address (it is outside the L2 buffer space). For optimal performance, this needs to be changed (to avoid switching on/off spy mode all the time)

Spy Mode Failures

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Fermilab
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Now reproducible in teststand

Bug in TRACER logic discovered yesterday (Myron, Terri)

... but other problems are likely to appear!

COT Occupancy

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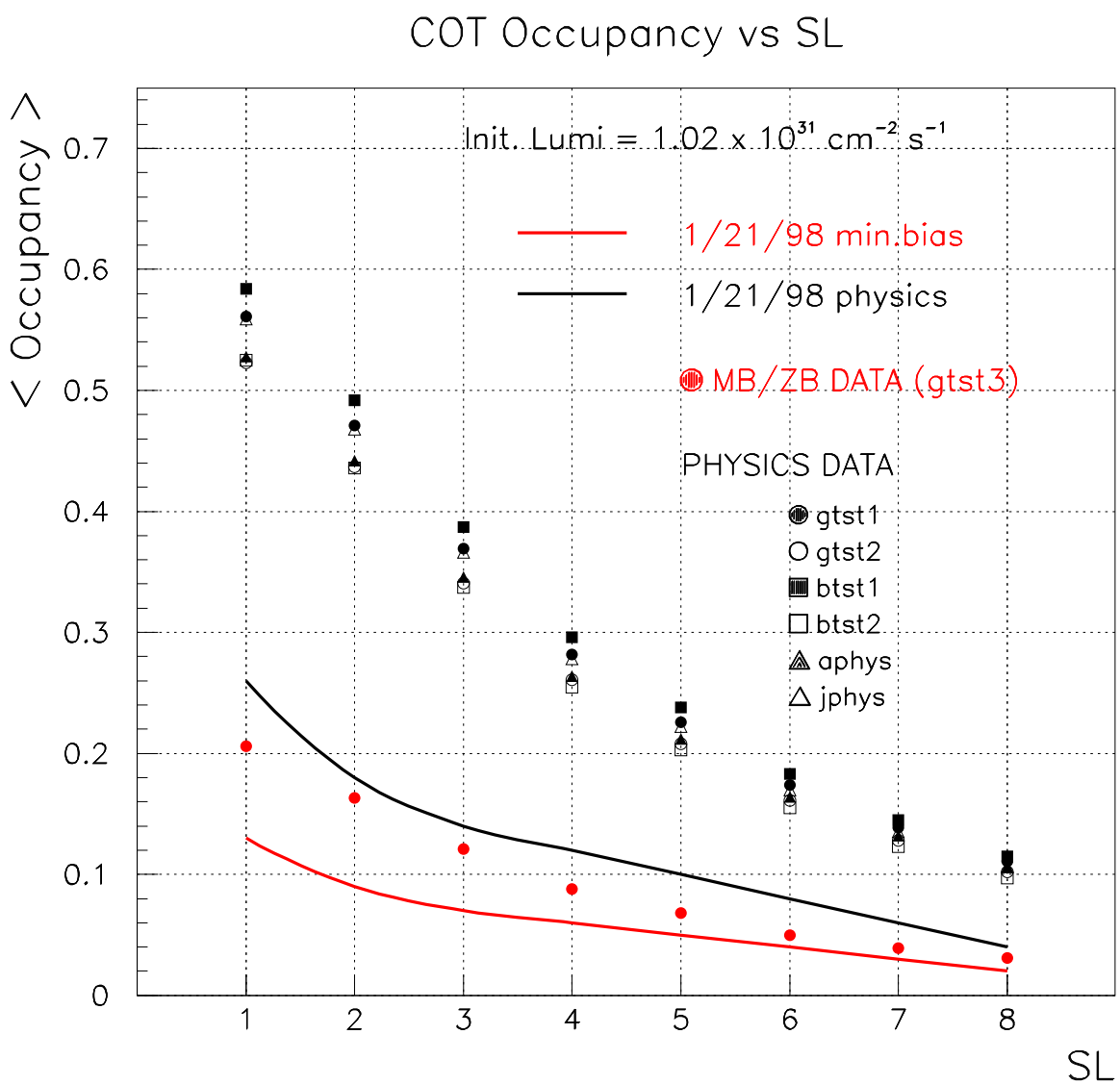
Observed occupancy is about a factor of 2 higher than expected, likely due to additional material



COT Occupancy

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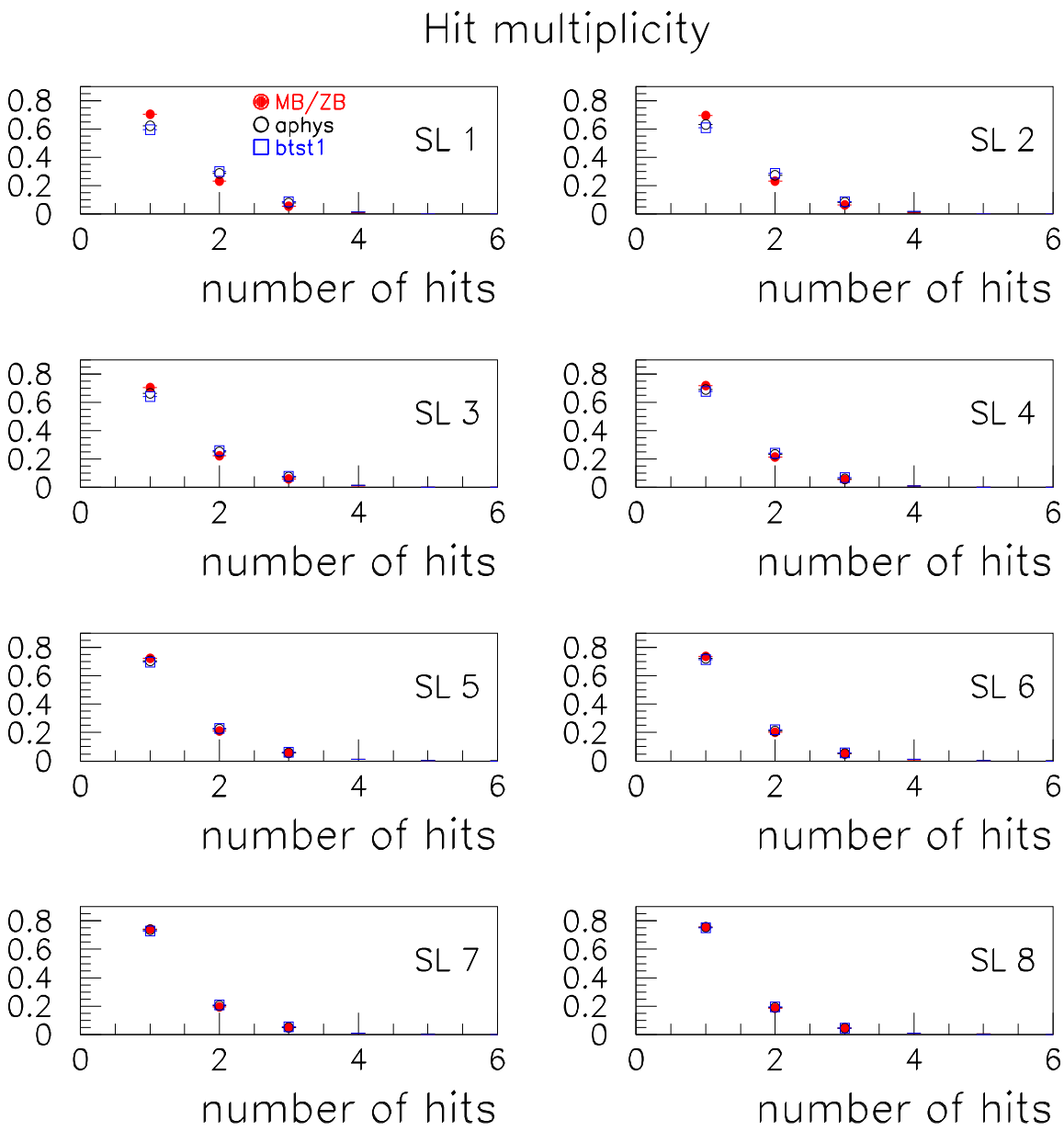

Data Transfer and Data Size

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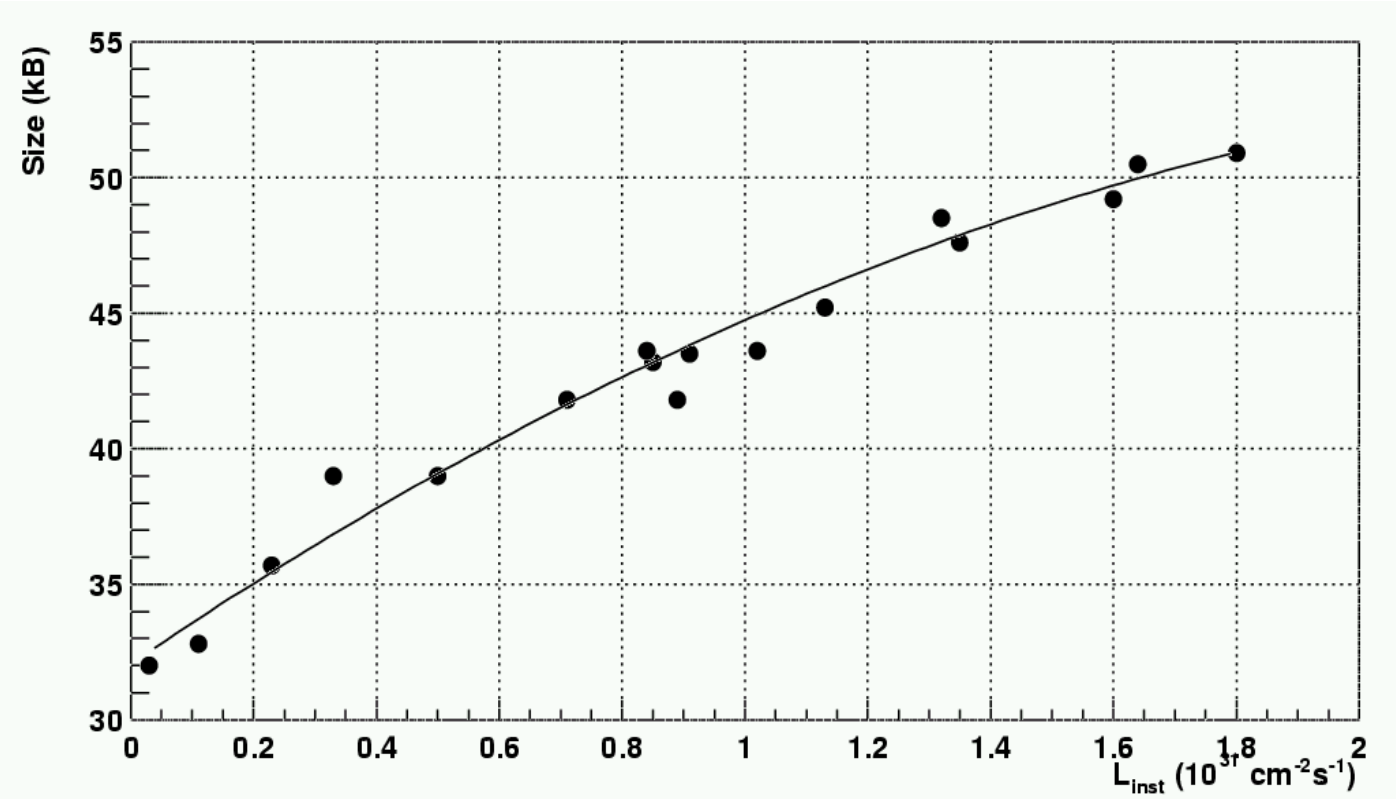
- Data transfer rate (Taxi link from TRACER to VRB) is **12.1MB/sec**
- This corresponds to ~12kB per crate at 1kHz readout rate (in other words, ~1.8 hits/channel). We are at ~2.5kB now.
- Don't have a precise idea when "pile-up" becomes a problem
  - Readout has to check occasionally state of the TRACER FIFO, wait if too full
  - Size of the TRACER FIFO is 32kB



Expected (1998):

<n>	kB
1	15
3	25
5	38
10	68

Missing Information

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Fermilab
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Quite hard to make an informed decision without answers to these questions:

- Given the current information, at what values of the instantaneous luminosity do the inner superlayers of the COT fail to contribute to pattern recognition? This could be answered with existing data!
- What is the relation between
  - maximum number of hits per channel allowed in readout
  - track reconstruction efficiency
  - instantaneous luminosity
- Updated information on expected data volume as function of luminosity

Potential Improvements

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Fermilab
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	~gain relative to current
• Spy mode:	5 - 20%
• More compact data format: (e.g. 21 bits/hit: 7 bits channel ID, 8 bits for start time, 6 bits for width; now 32 bits/hit)	up to 20% ???
• Remove FADC's	~ 15%
• Reduce overhead (eliminate data integrity checks, bunch counter checks etc.)	~ 5%
• Faster VME routines	~ 5%

- done for the tests shown here
- add another 200μs or so to the readout
- work in spy mode

All of the above will NOT be sufficient for 1kHz running

Conclusions

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Fermilab
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- TDC's are working very reliably at current design Level 2 accept rates of 300Hz
- Some features (spy mode) were never made to work (yet)
- The unexpectedly high COT occupancy will make it necessary to further optimize the readout and DSP code, in order to sustain the rate capability during run 2a
- In contrast to the rest of the DAQ, the TDC's are very vulnerable to occupancy fluctuations
  - The slowest TDC (of 315) determines overall performance
  - Occupancy hits in (at least) 2 places: DSP processing + VME readout
- The DSP processing time at current luminosities (0.6ms on average for the slowest TDC) will have to be
  - reduced to well below 0.5ms
  - stay there for 10x today's maximum luminosity
- Even with negligible DSP processing time, the VME readout will need to be improved to achieve 1kHz L2A rates