Triggering on detached vertices

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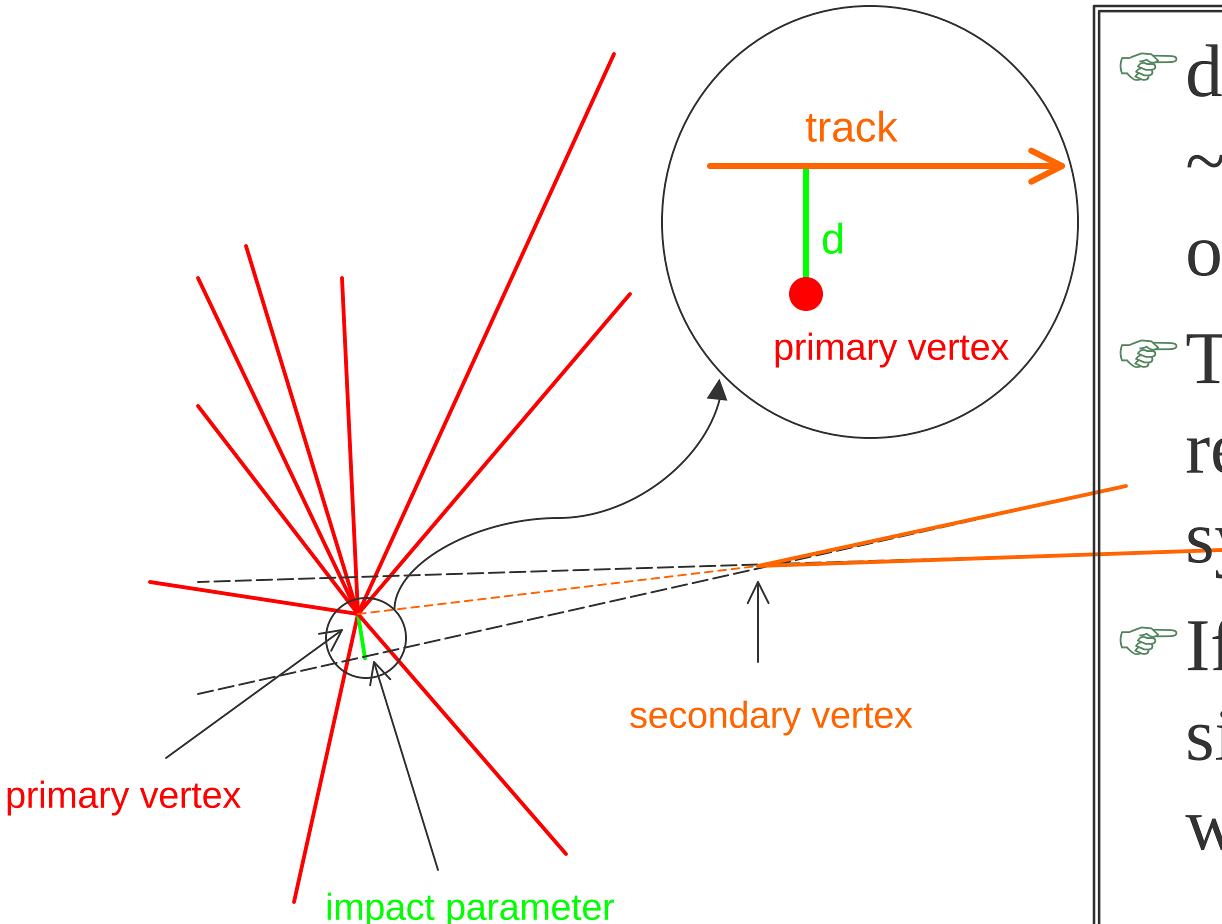
Outline of this lecture

- ☞ Why detached vertices?
- ☞ Introductory considerations
- ☞ Early ideas / implementations
- ☞ Today: CDF & the Associative Memory
- ☞ Today: D0 more recent project
- ☞ Towards the future: L1 V-trigger@BteV
- ☞ Towards the future: ideas for LHC

Why detached vertices ?

- Heavy Flavors play a central role in HEP
  - Charm physics
  - B physics, CP violation, Bs oscillation
  - New physics at high Pt often couples to HF
- c and b lifetimes ~10^{-12} s - distinctive signature
  - Many decays have no leptons !
- Need for *large* samples/specific hadronic channels
- **Detached decay vertexes a crucial handle**
  - Specially important in hadronic collisions
  - High rates/high backgrounds/limited BW to tape:
  - need to select HF *before* writing data out

Impact parameter



- d from b/c decays: ~100μm (independent of Pt)
- Tipical offline d resolution from Si systems: 10-50μm
- If relaxed, distinction signal - background washes out quickly

Detached vertices, how to ?

- Often look for a number of detached tracks rather than a vertex
- Need track reconstruction with almost-offline quality in a very small time
- A more recent development in the art of triggering
  - A race between state-of-the art electronics and design and increasingly challenging experimental environments
  - Large parallel systems, new tracking ideas

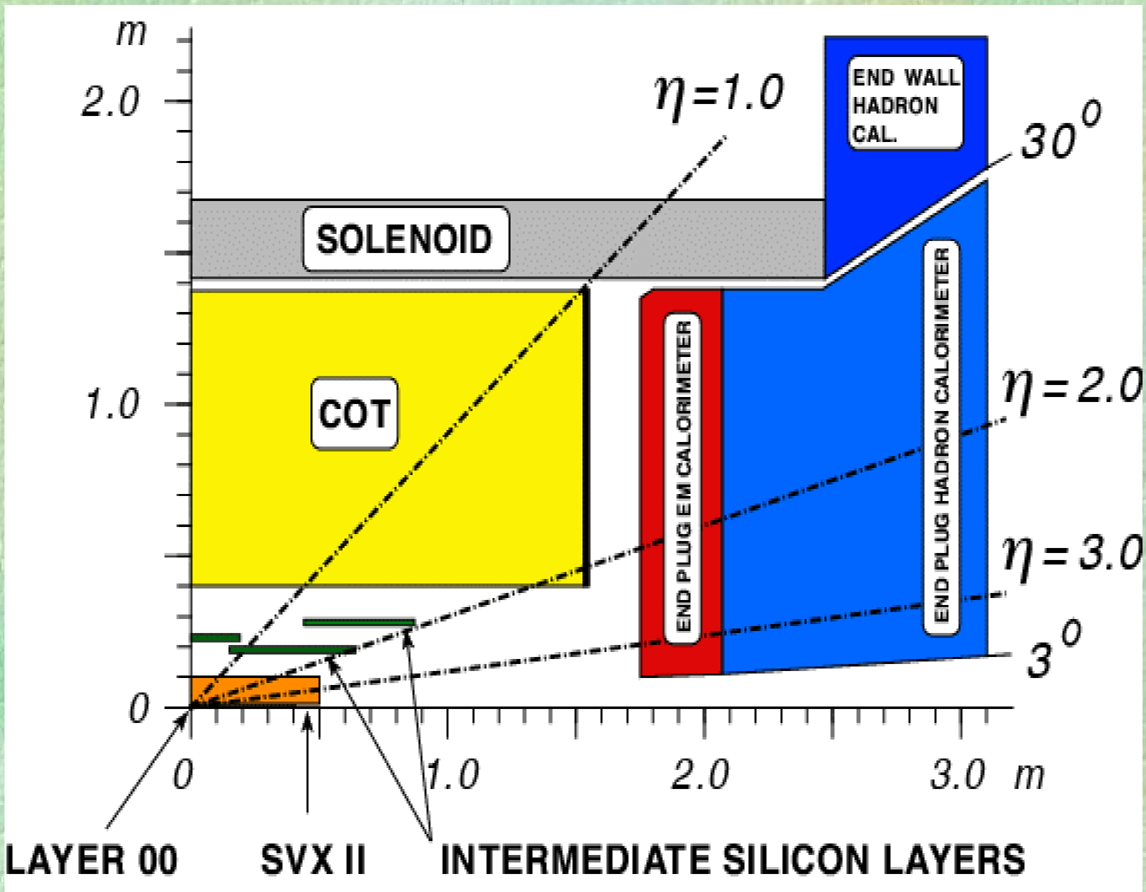
WA82/WA92: an early example ('90)

- Fixed target experiment, looks for c and b production in p-N collisions at 350GeV in the lab frame. ~MHz input rate
- Uses 6 planes*48 bins (25kchannels total) to reconstruct tracks coming from the primary vertex, then iterates scanning for secondary vertices.
- Trigger: 3 primary + 2 secondary tracks
- Uses ASIC , makes a FASTBUS crate. 35μs total time, used at asynchronous L2, independent of occupancy.
- Rejection ~10 for b/c, a modest improvement (initial S/B ~10^{-6}). Only useful in conjunction with other triggers.
- Close to the limits at the time - **how can one deal with much more complicated collider experiments** ?

V-trigger comes of age @CDF

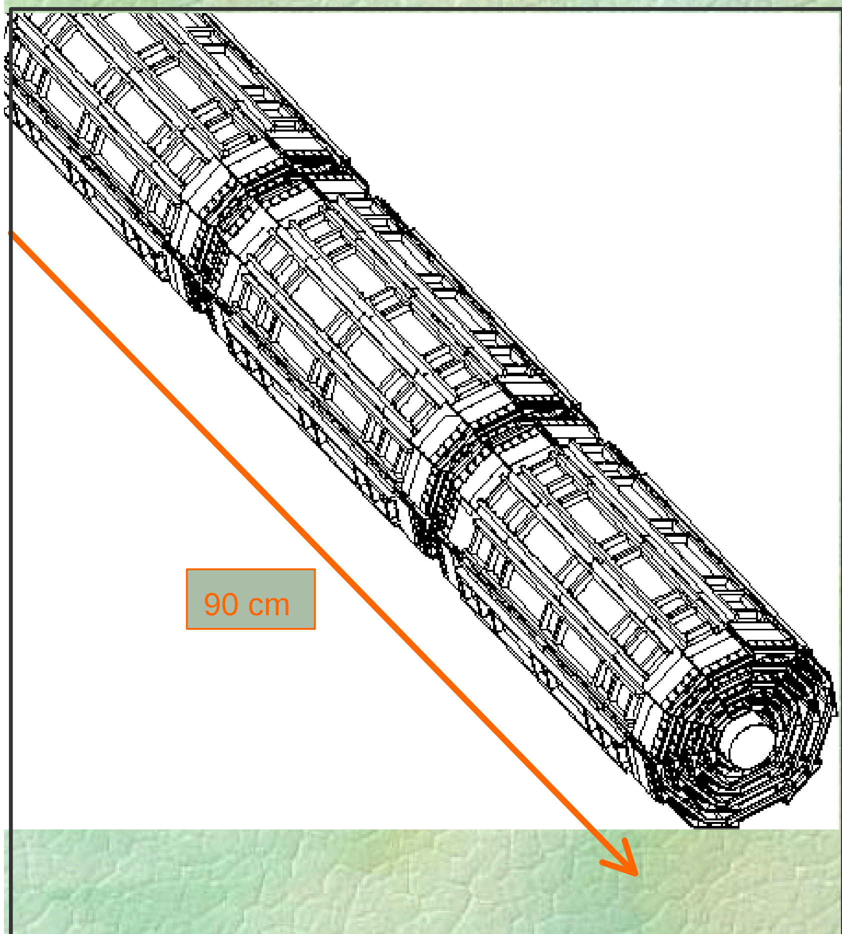
- **GOAL: Boost CDF B-physics reach**
- B production at Tevatron large (10^{11}/year) but:
  - QCD background is 1000x larger
    - RUN I trigger on (stiffor 2) leptons ⇒ low efficiency
- **Solution:** Build a fast device to reconstruct SVX tracks *online*

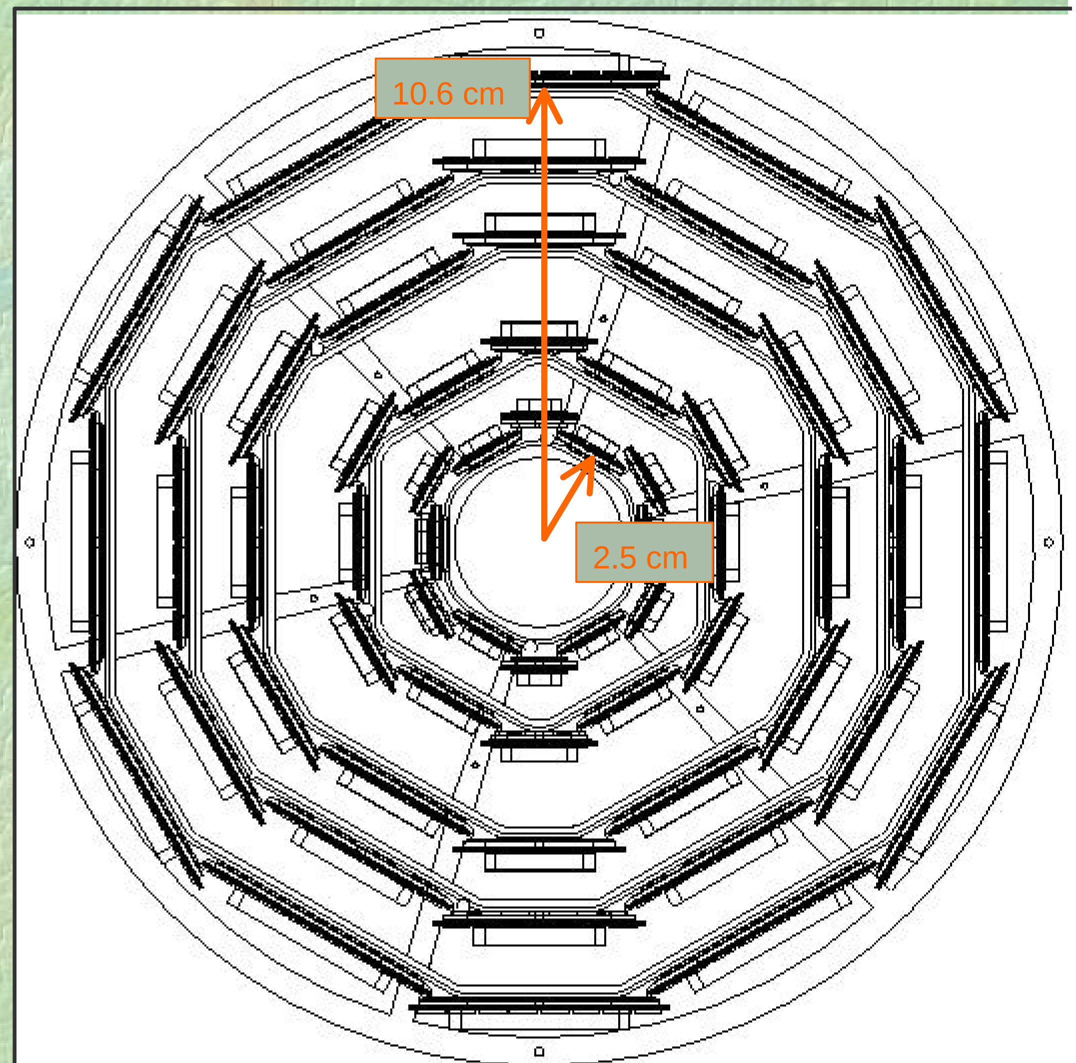
Quadrant of CDF II Tracker



- -COT: Drift chamber
  axial+stereo wires
- -SVXII + ISL layers
  6+3 Si microstrip
  2-sides
  90deg/stereo
- -L00:
  Innermost, 1-sided

SVX II

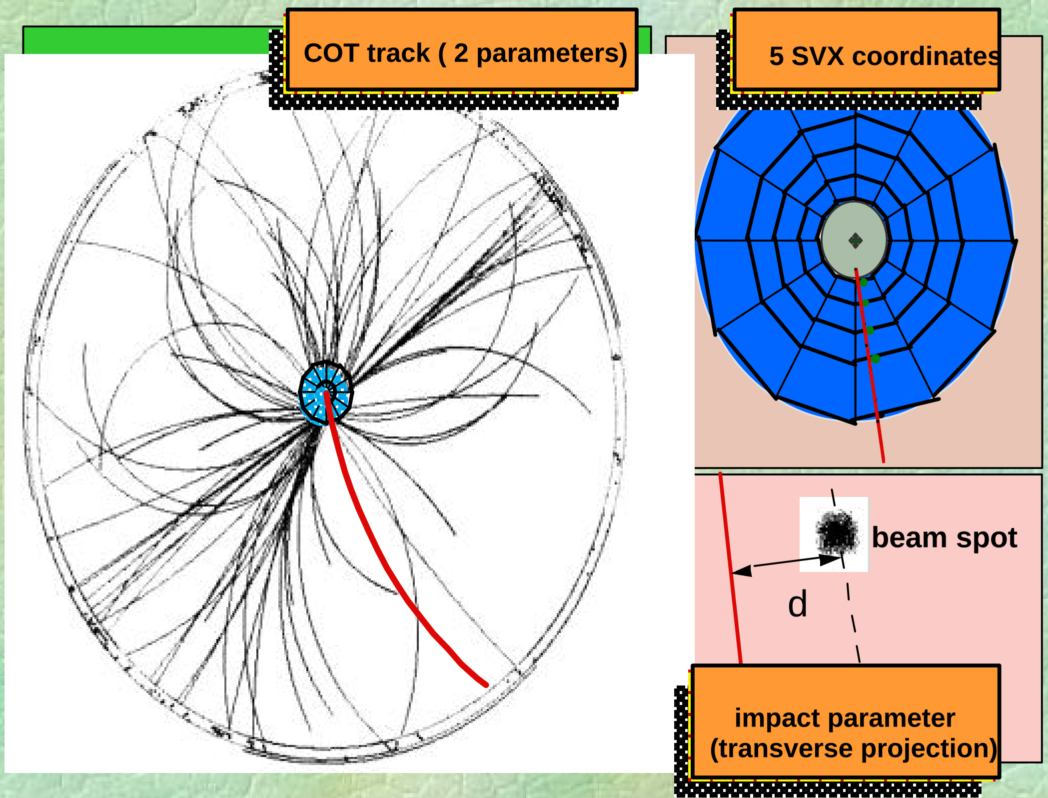




Point resolution ~12µm

L1 analog pipeline and digitization in Front-End - Read out at L1 accept

SVT: Silicon Vertex Trigger



The Catch:

SVX has a small lever arm

=> low Pt resolution

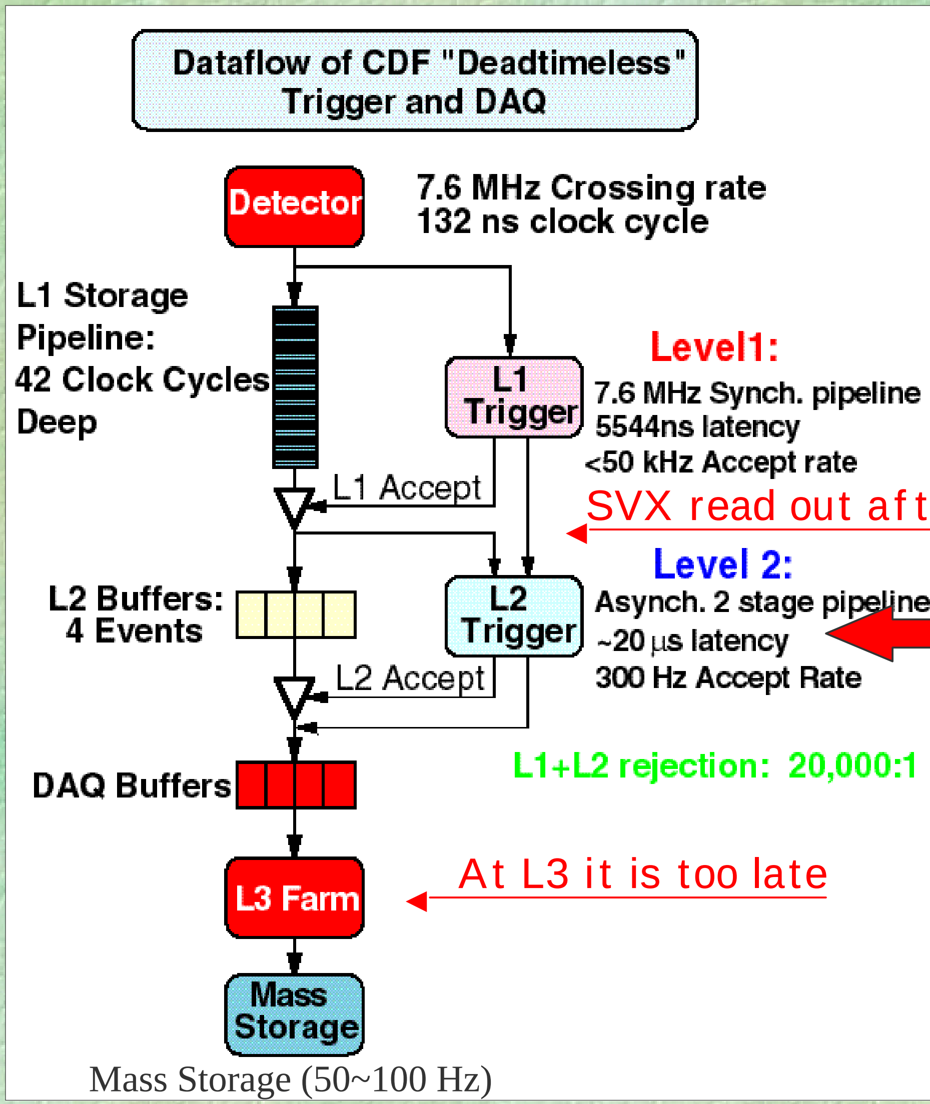
=> bad extrapolation to origin

=> need <u>*additional*</u> input

<u>SVT Inputs:</u>

- COT tracks from Level 1 XFT (f, P_t)
  - 2D, Pt resolution 2%*Pt, Pt>1.5
- Digitized pulse height in SVXII strips

CDFII trigger/DAQ



- CONSTRAINTS to SVT:
  - $O(10^5)$ SVX channels
  - $O(10^3)$ fired channels/event
  - 50 kHz input rate
  - Latency <10 μsec
  - No Dead Time allowed

Trigger on Hadronic B decays

Two paths

- L1:
  - Two XFT tracks
  - P_{t1}>2 GeV P_{t1}+P_{t2}>5.5 GeV
  - $\Delta\phi$<135°
- L2:
  - d_0>100 μm for both tracks
  - Validation of L1 cuts with $\Delta\phi$>20°
  - $P_t \bullet X_v$ > 0
  - $d_0(B)$<140 μm

High Mass

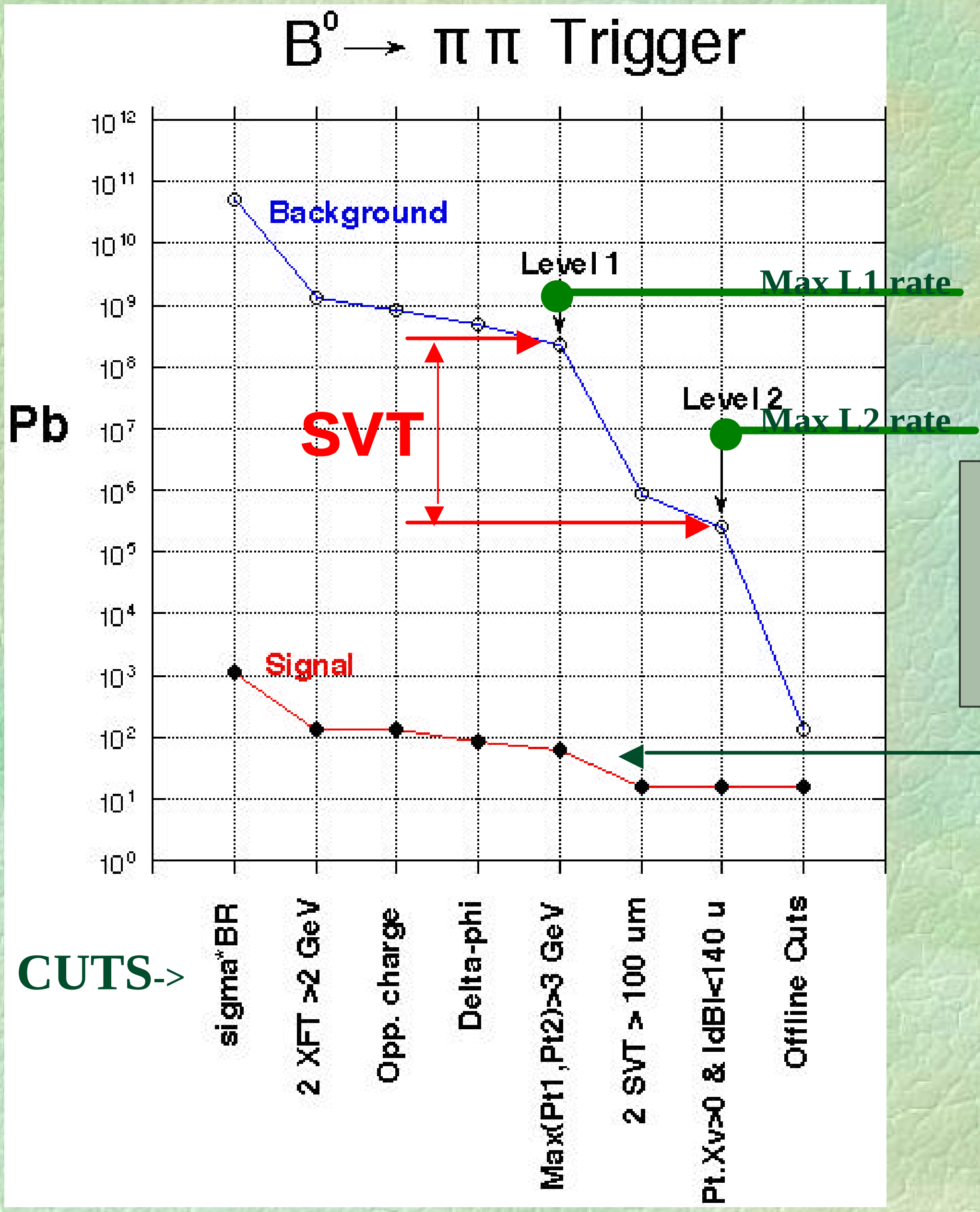
Two body decays

- L1:
  - Two XFT tracks
  - P_{t1}>2 GeV P_{t1}+P_{t2}>5.5 GeV
  - $\Delta\phi$<135°
- L2:
  - d_0>120 μm for both tracks
  - Validation of L1 cuts with $\Delta\phi$>2°
  - $P_t \bullet X_v$ > 0
  - ~~$d_0(B)$<140 μm~~

Low Mass

Many body decays

Hadronic B trigger

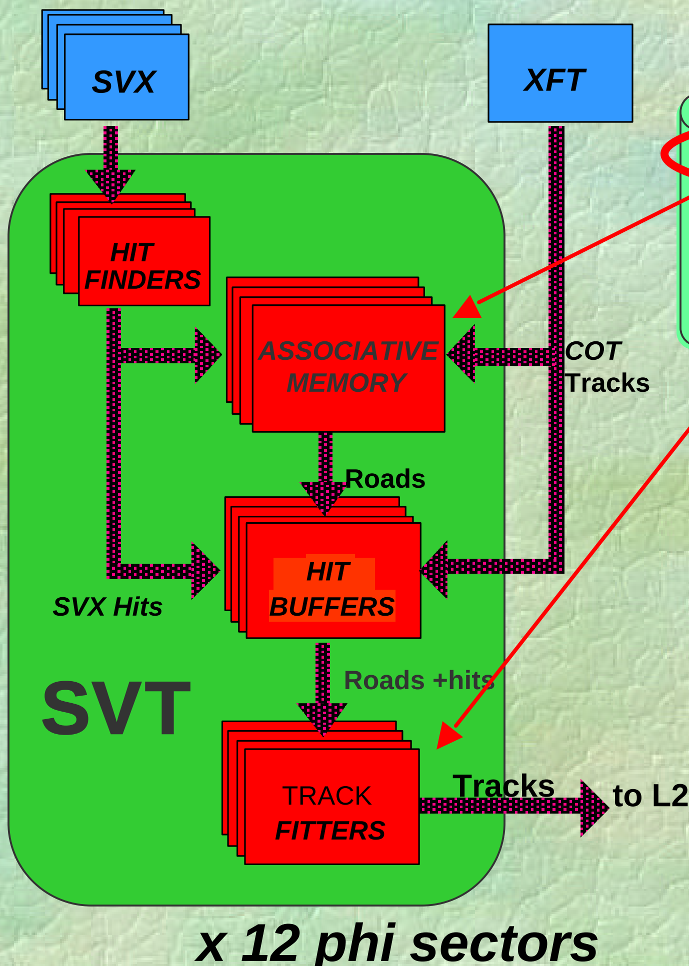


CUTS->

SVT rate reduction:
3 orders of magnitude

Little signal loss

SVT: Silicon Vertex Trigger



The SVT way

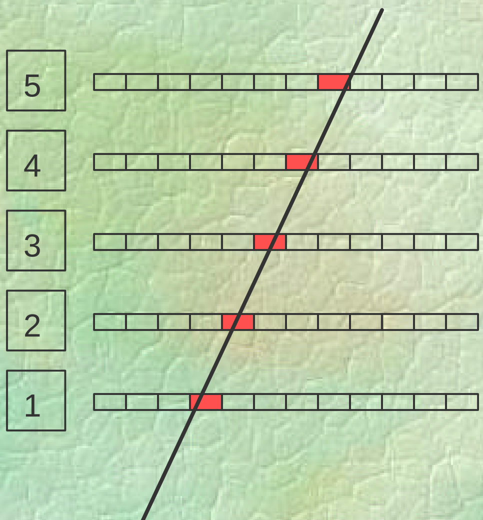
1st: find low-res tracks
2nd: fit for best resolution

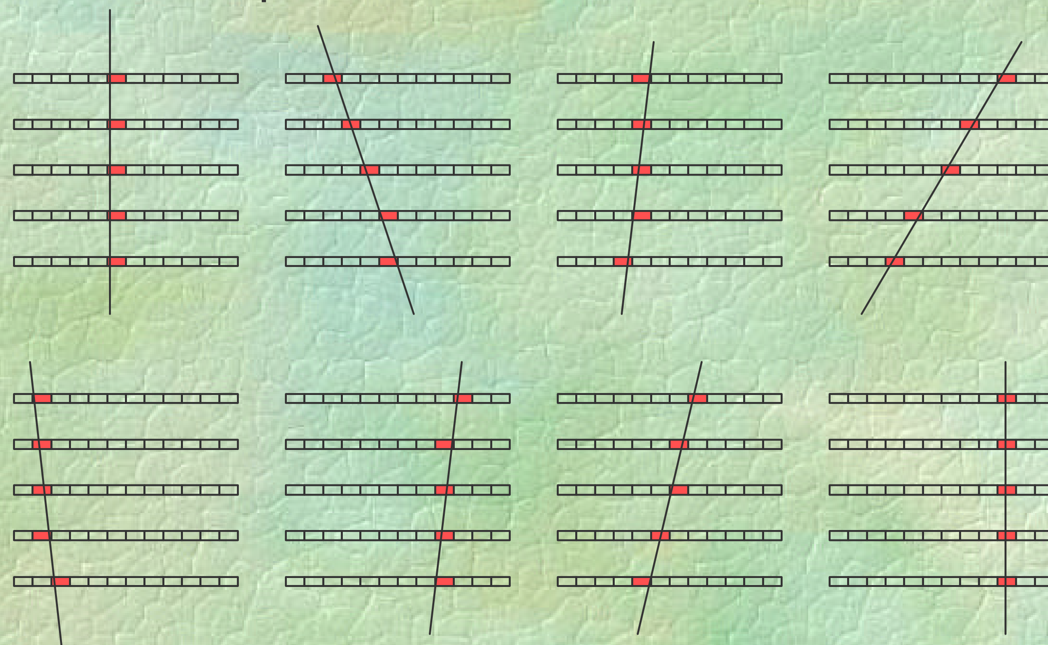
- **Asynchronous data-driven pipeline**
- Hit Finder: "on the fly" cluster finding
- Associative Memory: real-time pattern recognition at low resolution
- Hit Buffer: associates hits to the roads found by the Associative Memory.
- Track Fitter: full-resolution fit

Step I: match precalculated "Patterns"

Instead of looking for hit combinations such that *f(x1,x2,x3,…) = 0*

1. Build a database with all patterns corresponding to "good" tracks
2. Compare hits in each event with all patterns to find track candidates





In this example:
Straight lines, 5 layers, 12 bins/layer

⇨ Total number of patterns grows as Nbins^Npars

Building a “Pattern Bank” for CDF

- ☞ Divide in 12 phi wedges
- ☞ Limit to 2-D, and Pt>2GeV
  - It means the beam must be parallel to the detector !
- ☞ 6 layers: 5 SVX + 1XFT
- ☞ AM flexibility: XFT is just another layer
  - use f(Pt,phi)= phi@SVX
  - Optimized for minimal AM size

Used 4 SVX + 1 XFT (no miss) up to date - now moving to 5 SVX + 1 XFT (1-miss) to increase efficiency.

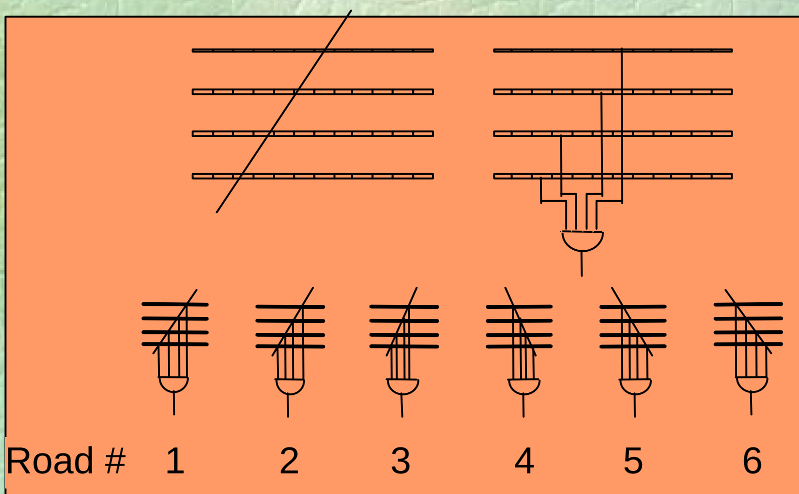
Building a “Pattern Bank” for CDF

☞ Important Tradeoff:

- Smaller bins=>more patterns
- Larger bins
  - Þ more fired patterns/event
  - Þ larger combinatorics inside each pattern
- Þ More work in fitting stage
- CDF optimum: ~300 µm bins
  Þ **32k roads *12 sectors**

Massively parallel pattern matching: the **Associative Memory**

A set of patterns is stored in the Associative Memory. Each pattern (ROAD) contains the coordinates of hit at each detector layer of a possible track.

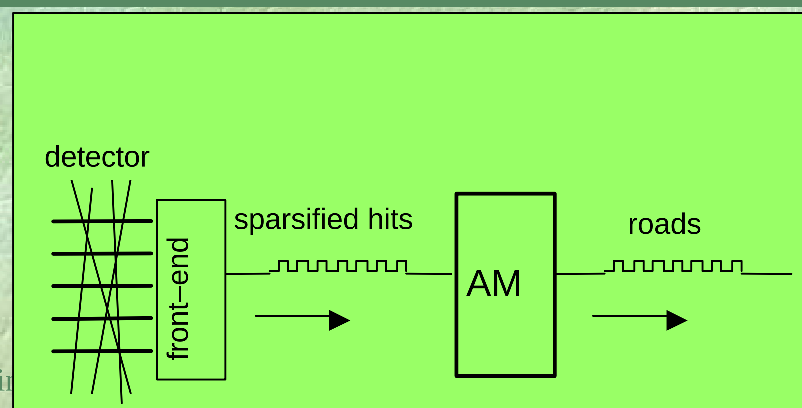


Hit coordinates are read out sequentially into the AM.

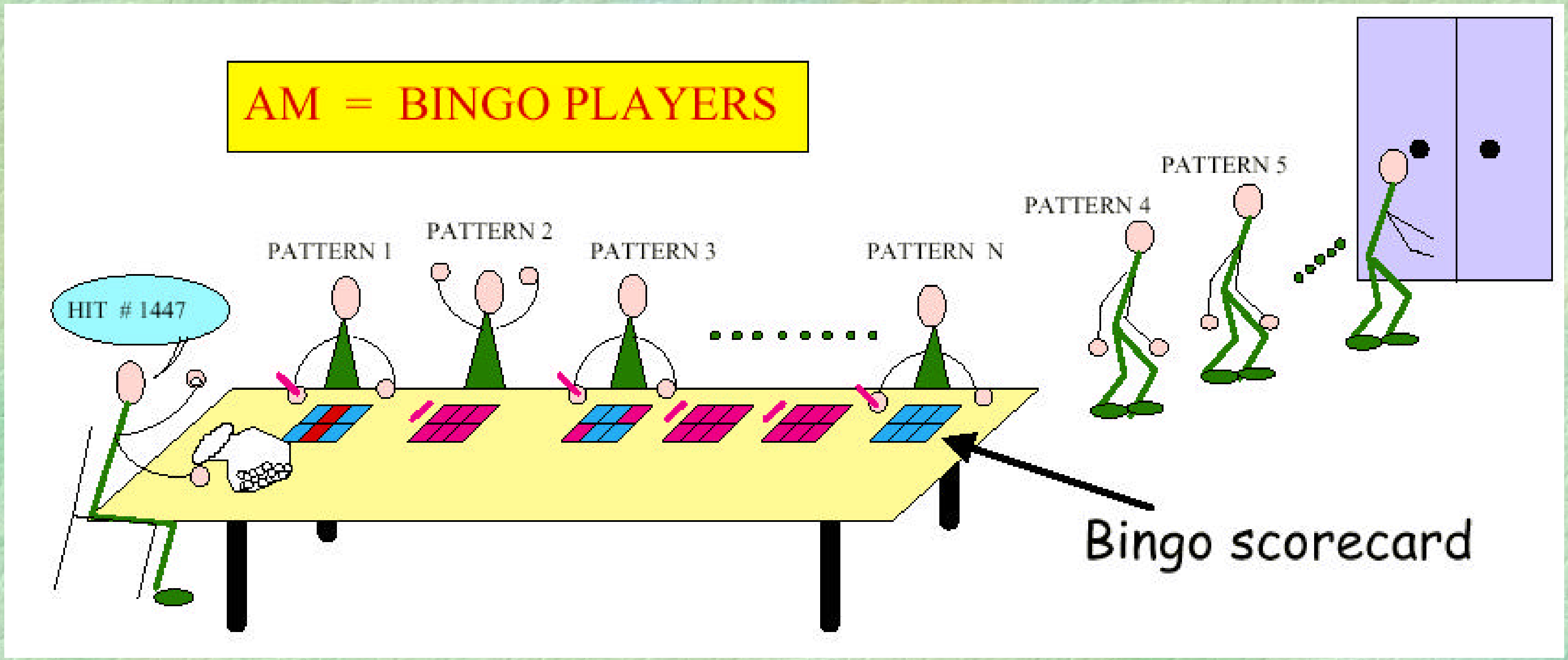
In the AM, each coordinate is compared to all the patterns in parallel.

Pattern recognition is complete as soon as the last hit is read.

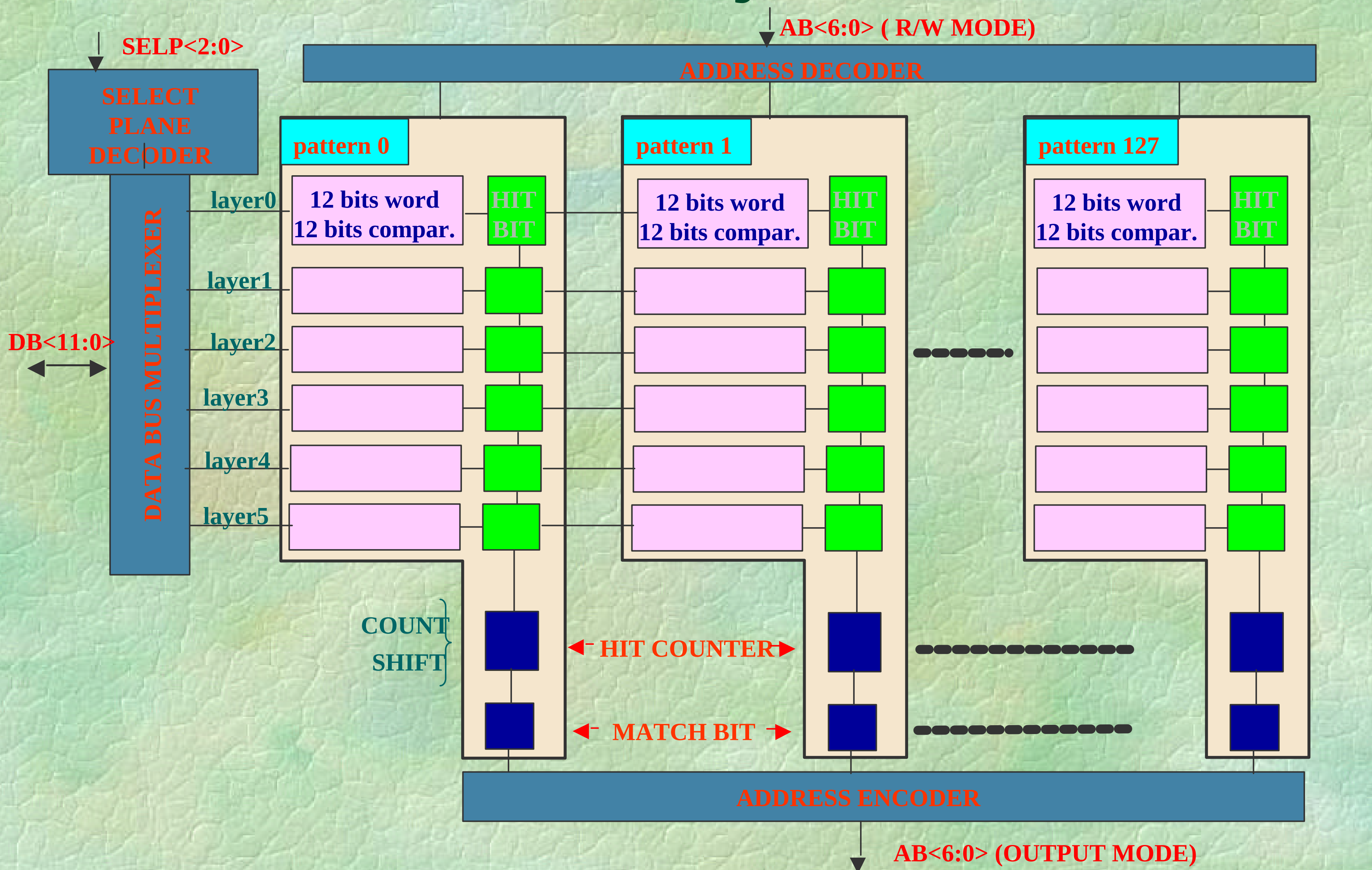
Roads found by the AM are output sequentially.



Associative Memory and bingo...

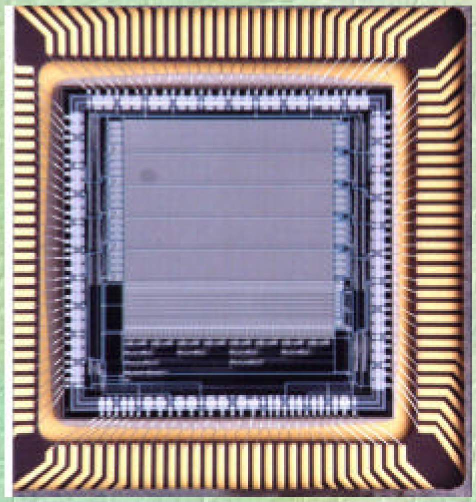


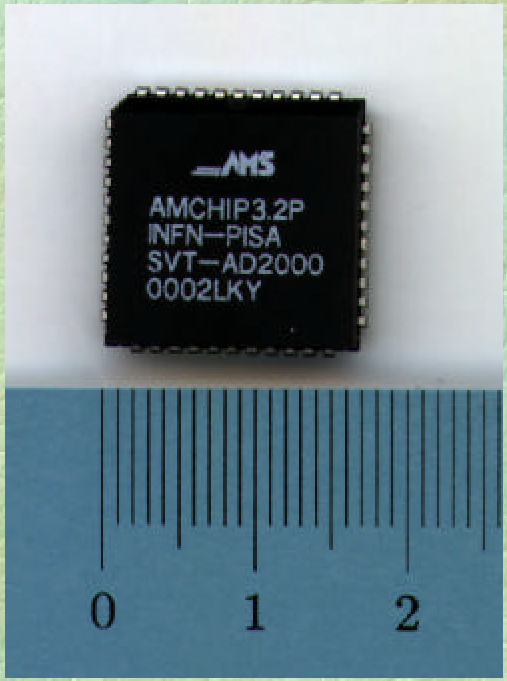
Associative Memory internal structure



Custom AM Device

Special electronics was needed to implement the functionality required by SVT

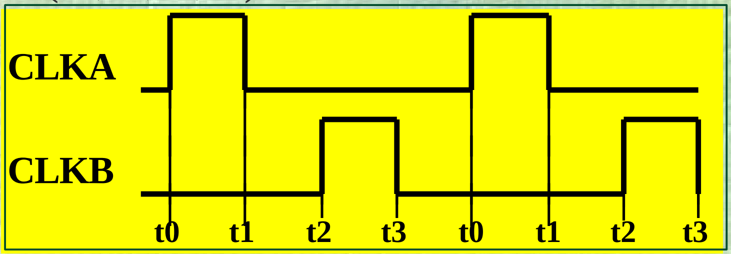




- **<u>Full custom</u>** VLSI chip, developed at INFN-Pisa (started in the '80!)
- 0.7μm technology
- 35mm^2
- 180000 transistors
- 128 patterns, 6x12bit words each
- majority logic
- Working up to 40MHz

AM chip

- Full custom VLSI, 0.7 μ technology, 2 metal layers 1 poly, 35 mm^2 die surface, ~ 180,000 transistors, PLCC44 package, 128 patterns stored, 6 layers of 12 bit each
- Not overlapping 2 phase clock, CLKA & CLKB, using leading and trailing edge of both signals (t0,t1,t2,t3).

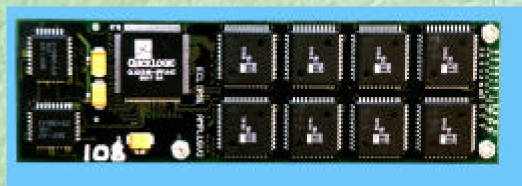


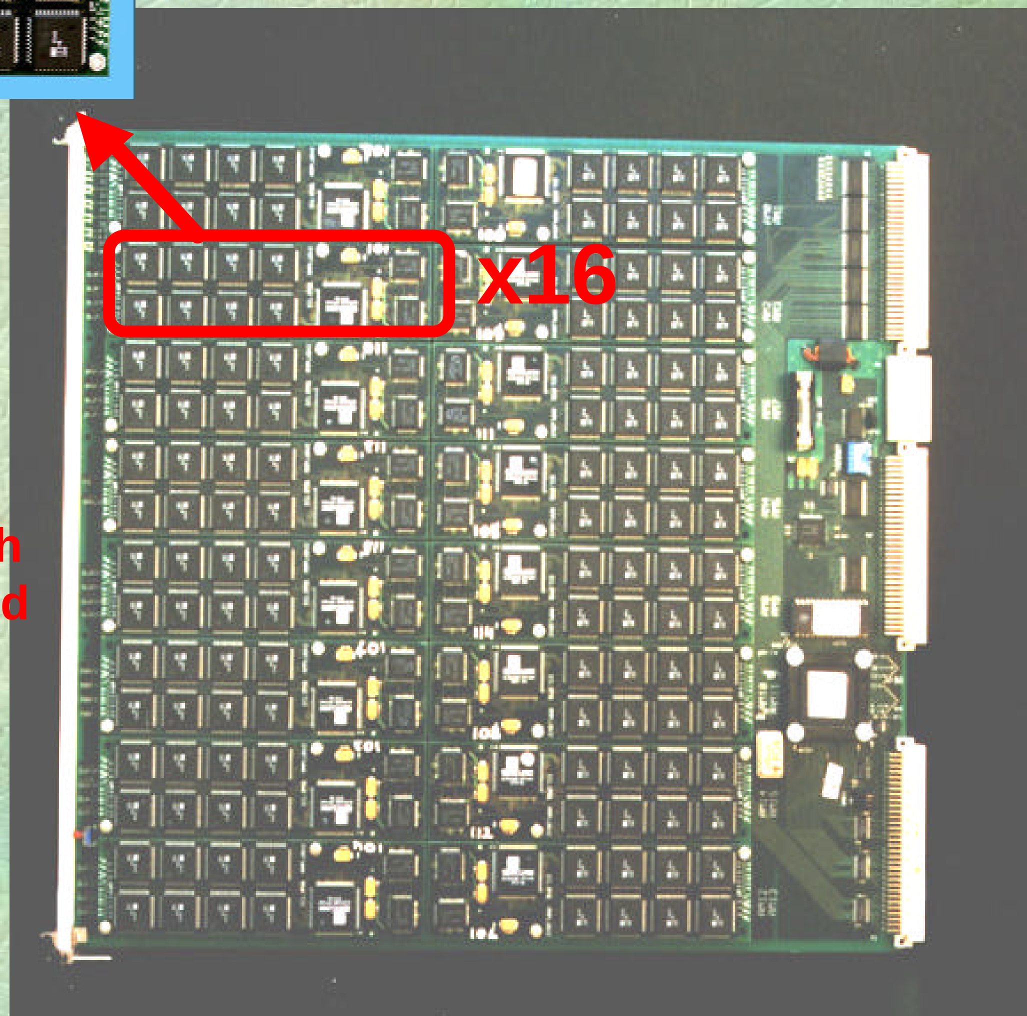
- Maximum output frequency ~ 40 Mhz => $t_{i+1} - t_i$ ~ 6 nsec => need very good control of clock edges. Maximum input frequency > 100 Mhz
- 16 operation codes:

0	***No Operation (NOP0)***	**9**	***Clear Counter and Load Shit Registers***
1	***Read***	**10**	***Init***
2	***Output***	**11**	***Disable***
3	***Write***	**12**	***Reset Handshake***
4	***Input***	**13**	***Enable***
5	***Clear Hit-Registers***	**14**	***No Operation (NOP14)***
6	***No Operation (NOP6)***	**15**	***No Operation (NOP15)***
7	***Shift***		
8	***Count***		

Great flexibility:
It is possible to fine tune the matching algorithm, asking 6/6 layers, or majority logic (e.g. 5/6 layers)

AM board (1998)



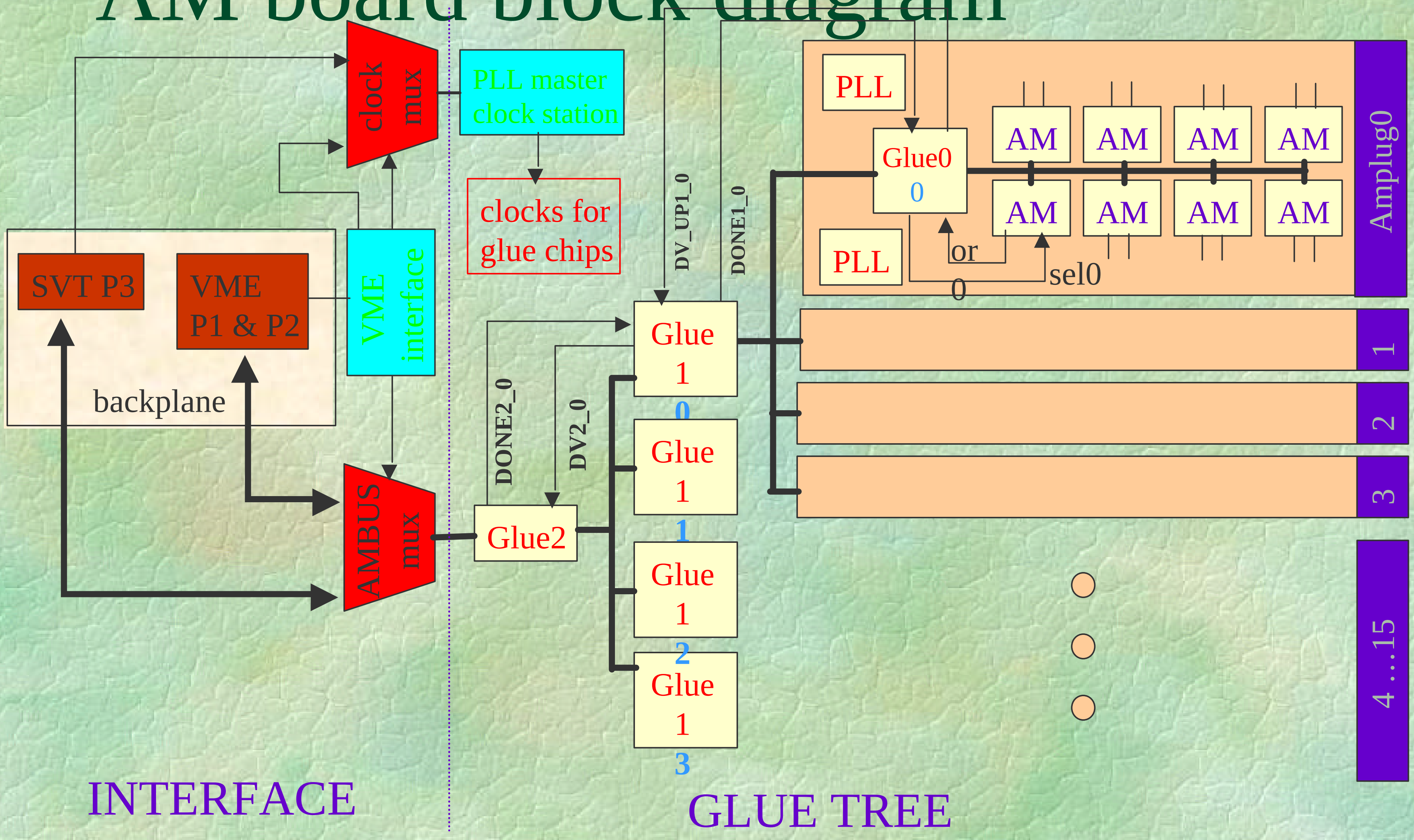


VME

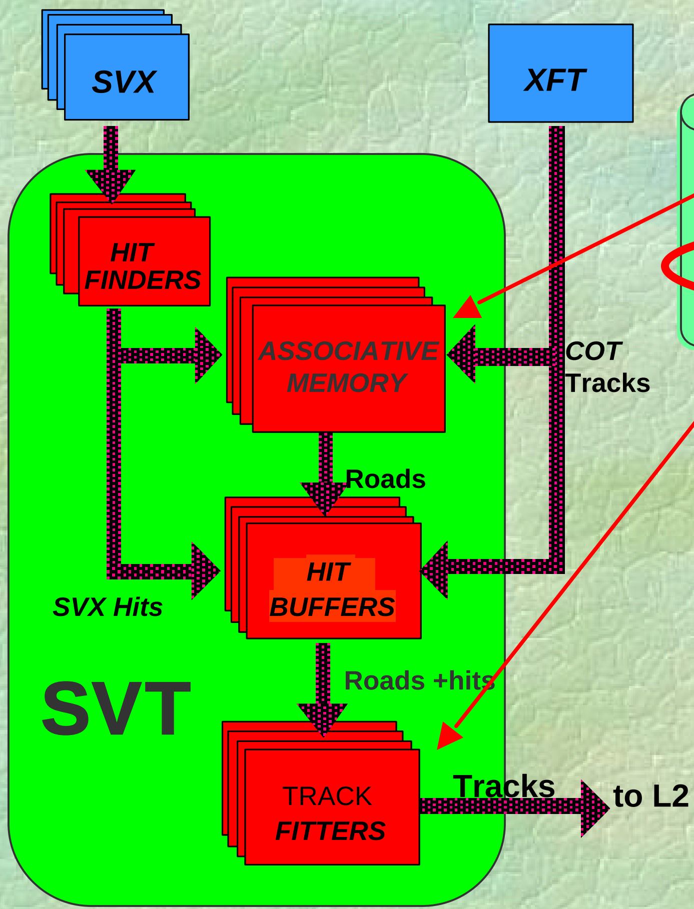
AMbus

128 Amchips
x 128 patterns each
= 16K pattern board

AM board block diagram



SVT: Silicon Vertex Trigger



x 12 phi sectors

The SVT way

1st: find low-res tracks
2nd: fit for best resolution

- **Asynchronous data-driven pipeline**
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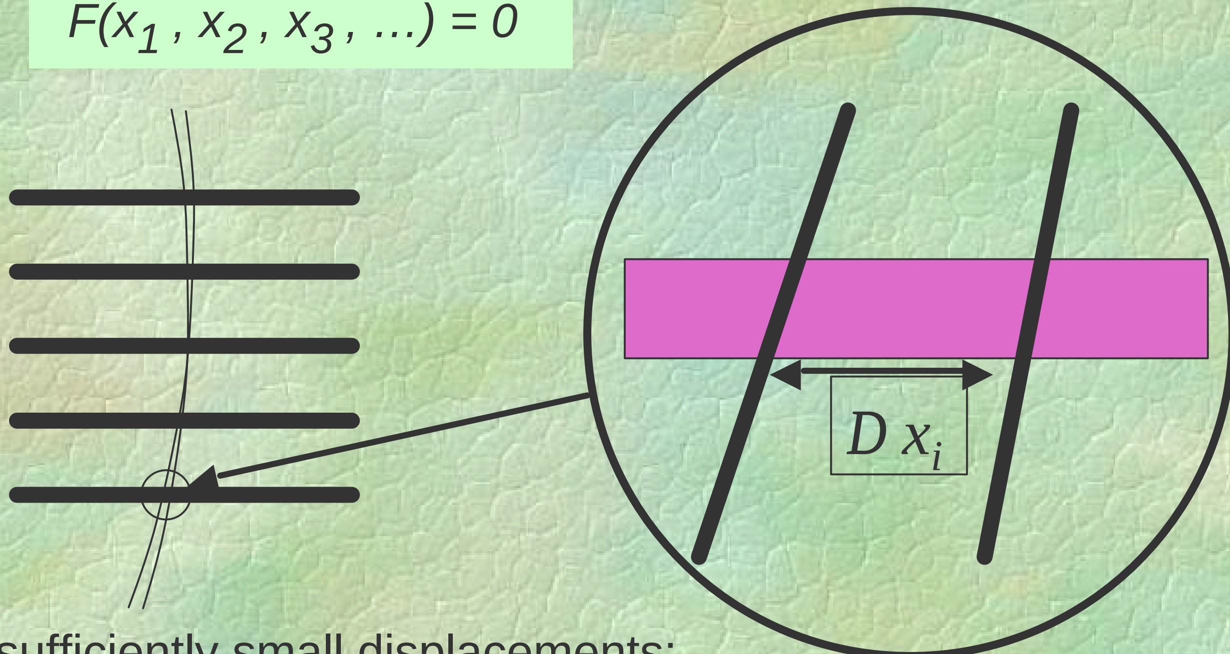
- Associative Memory: real-time pattern recognition at low resolution
- Hit Buffer: associates hits to the roads found by the Associative Memory.
- Track Fitter: full-resolution fit

StepII: use linearized constraints for speed

Non-linear geometrical constraint for a circle:

$$F(x_1 , x_2 , x_3 , \ldots) = 0$$



But for sufficiently small displacements:

$$F(x_1 , x_2 , x_3 , \ldots) \sim a_0 + a_1 Dx_1 + a_2 Dx_2 + a_3 Dx_3 + \ldots = 0$$

with constant a_i (first order expansion of F)

Constraint surface

6 coordinates: x_1, x_2, x_3, x_4, x_5 (P_T), x_6 (ϕ)

3 parameters to fit: P_T , ϕ , d

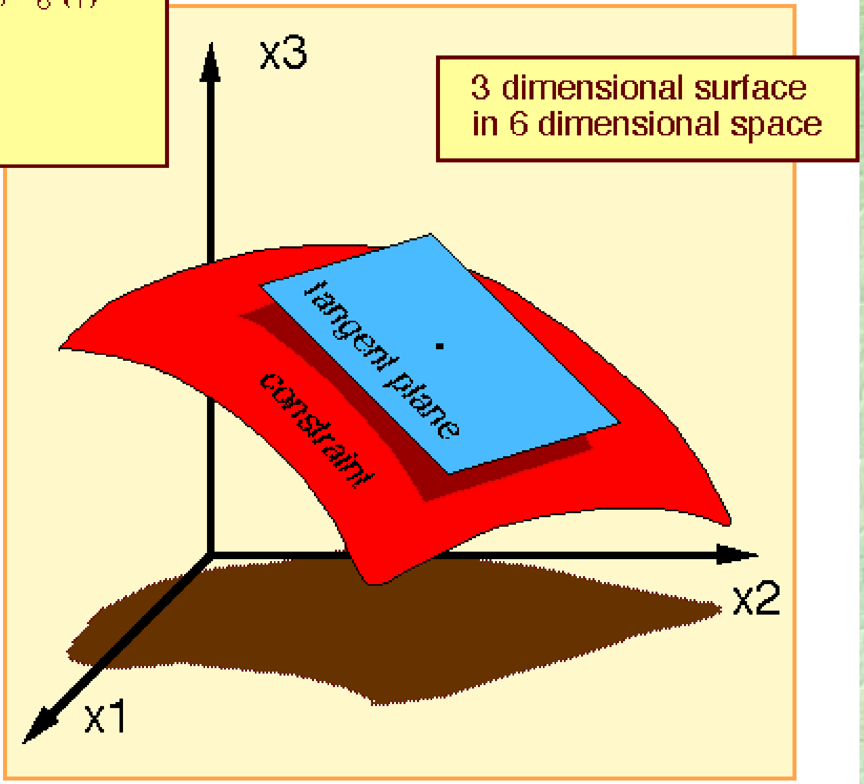
3 constraints

tangent plane:

$$\sum_{1}^{6} a_i x_i = b$$

track parameters:

$$d \approx c_0 + \sum_{1}^{6} c_i x_i$$



Linear approximation is so good that a single set of constants is sufficient for a whole detector wedge (30° in ϕ)

Track Fitter: find track parameters

Track parameters expressed as scalar products:

$P_i = F_i * X + Q_i$ ($P_i = p_t$, f , d , c $_1$, c $_2$, c $_3$, c)

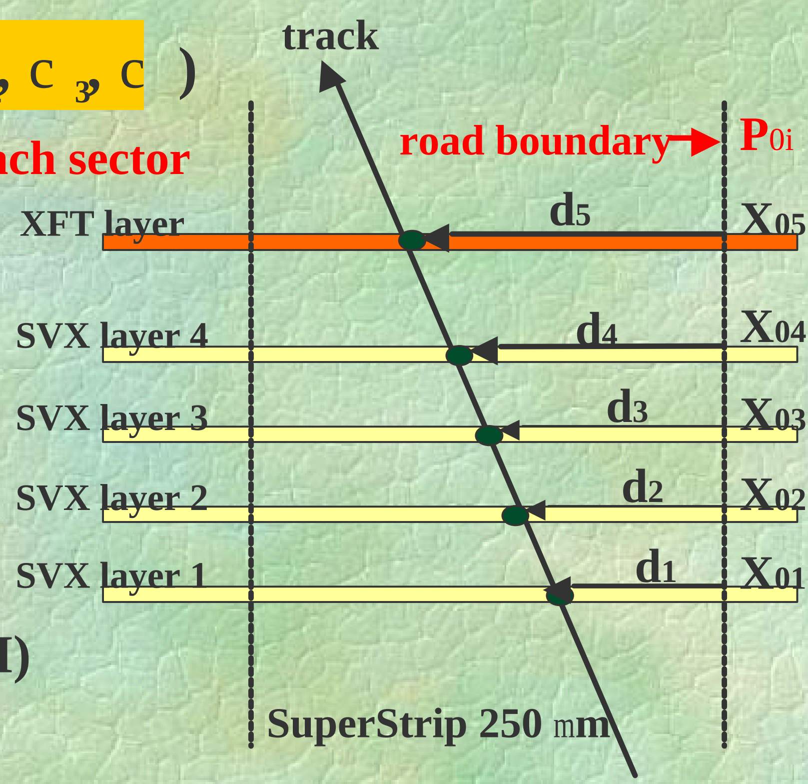
Coefficients fixed in each sector

$P_{0i} + dP_i = F_i * (X_0 + d) + Q_i$

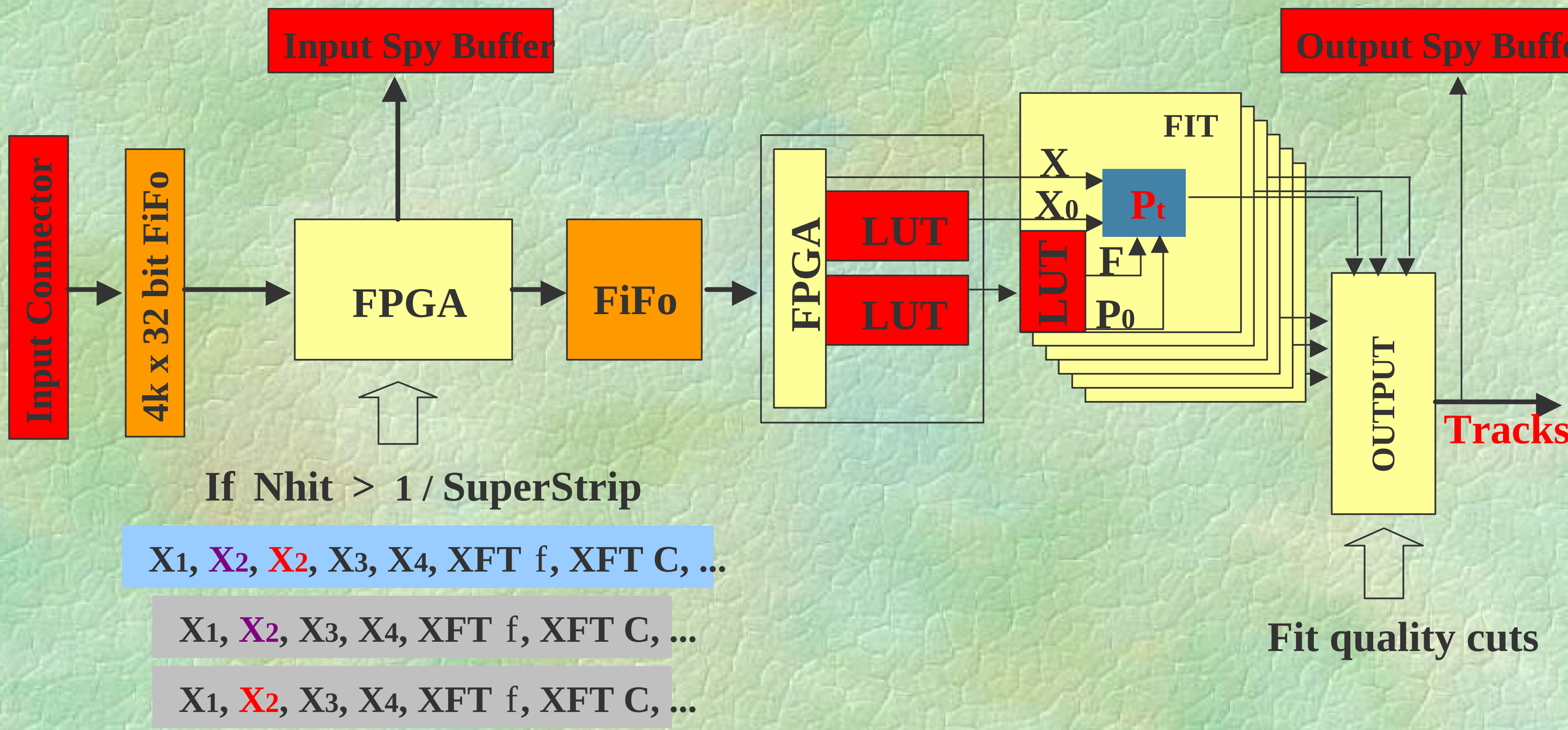
Lower SuperStrip edge

$P_{0i} = F_i * X_0 + Q_i$ (stored in a RAM)

$dP_i = F_i * d$



Track Fitter design

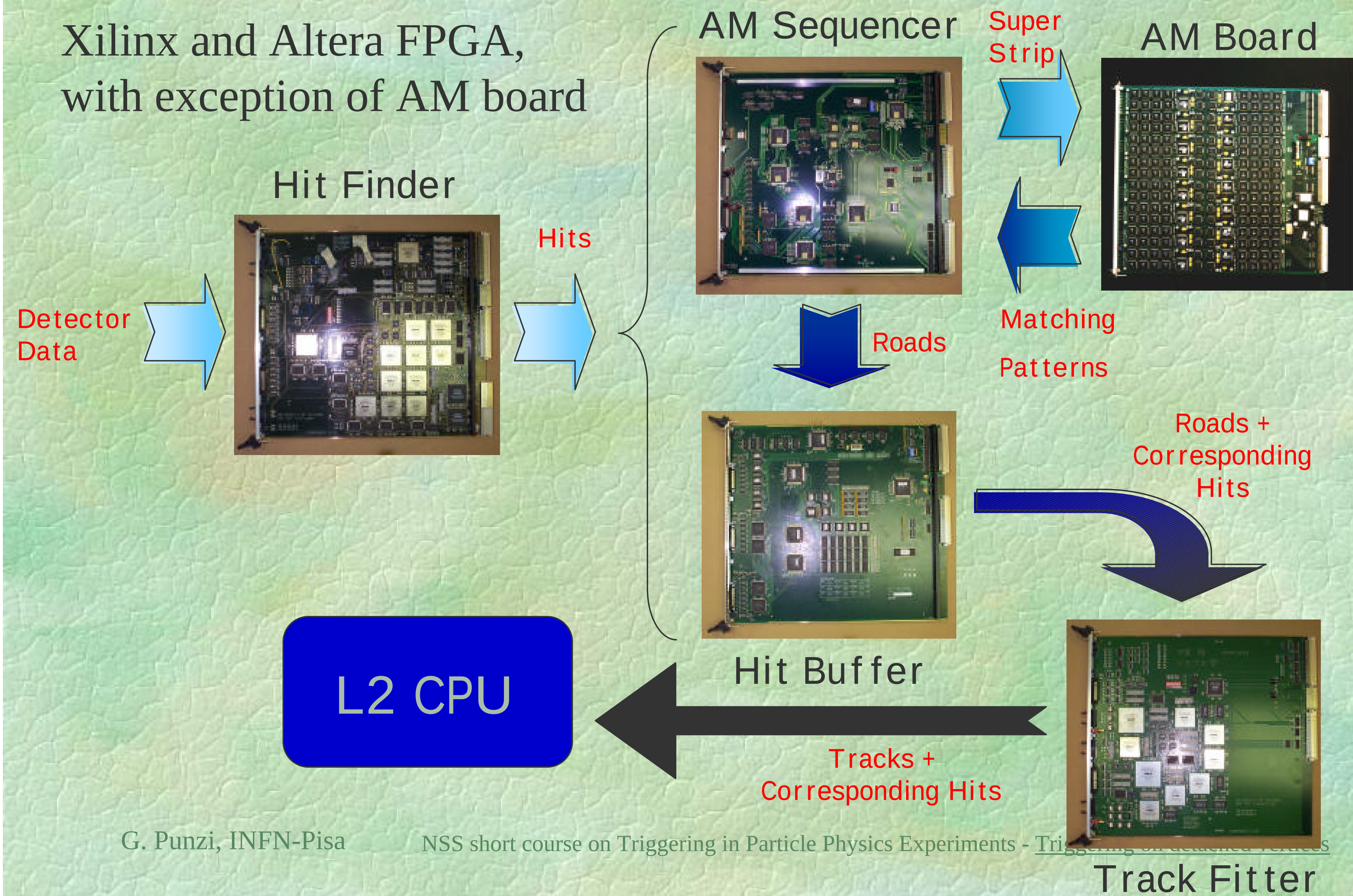


Timing: 1.1 ms (1 road, 1 combination)

All good fits are output - final SVT board (“GhostBuster”) selects only the best one

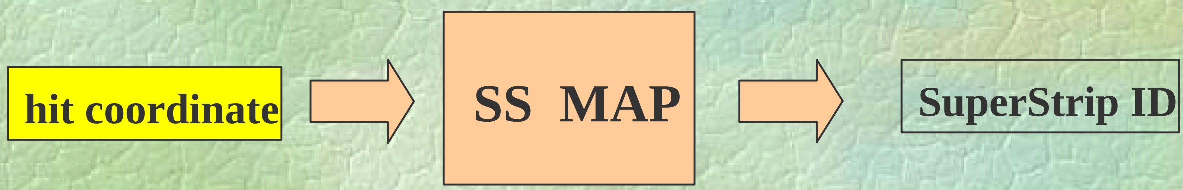
SVT boards

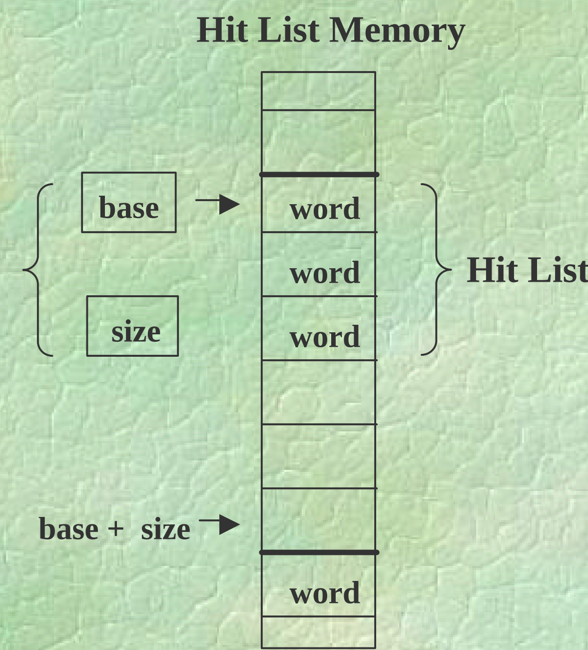
Xilinx and Altera FPGA,
with exception of AM board



Hit Buffer data processing

- **SS MAP: from hits to SuperStrips**

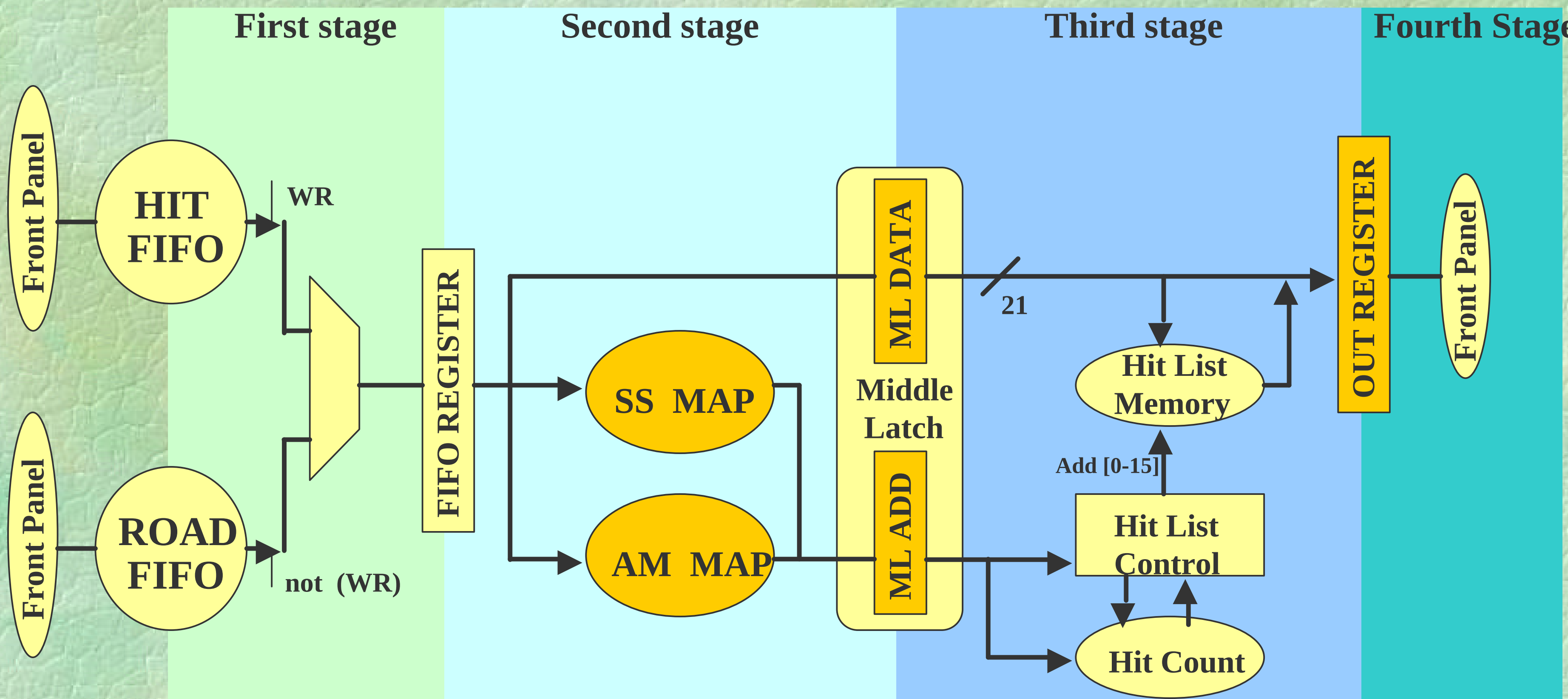




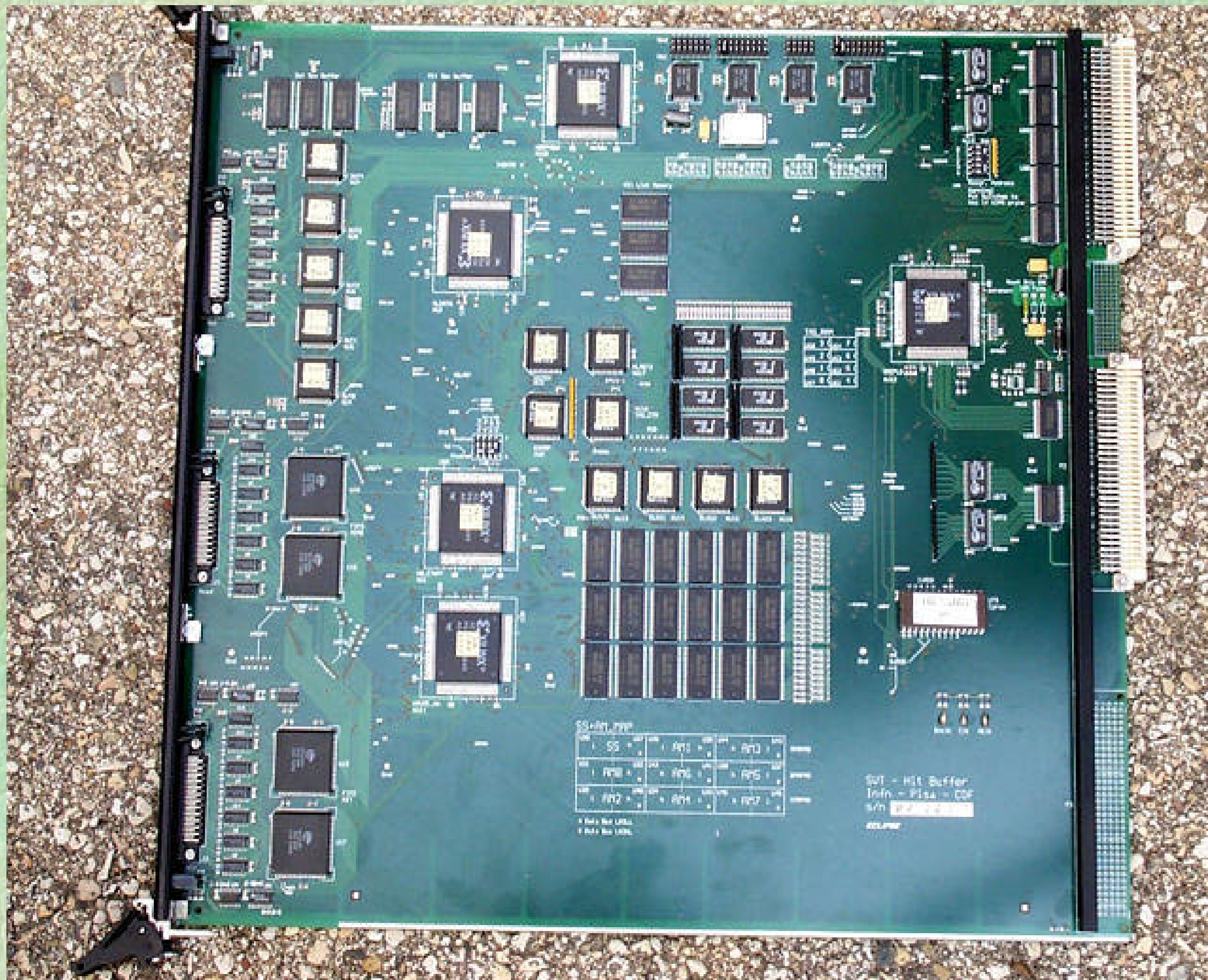
- **AM MAP: from roads to SuperStrips**

SuperStrip ID is used to access the corresponding List and retrieve hits

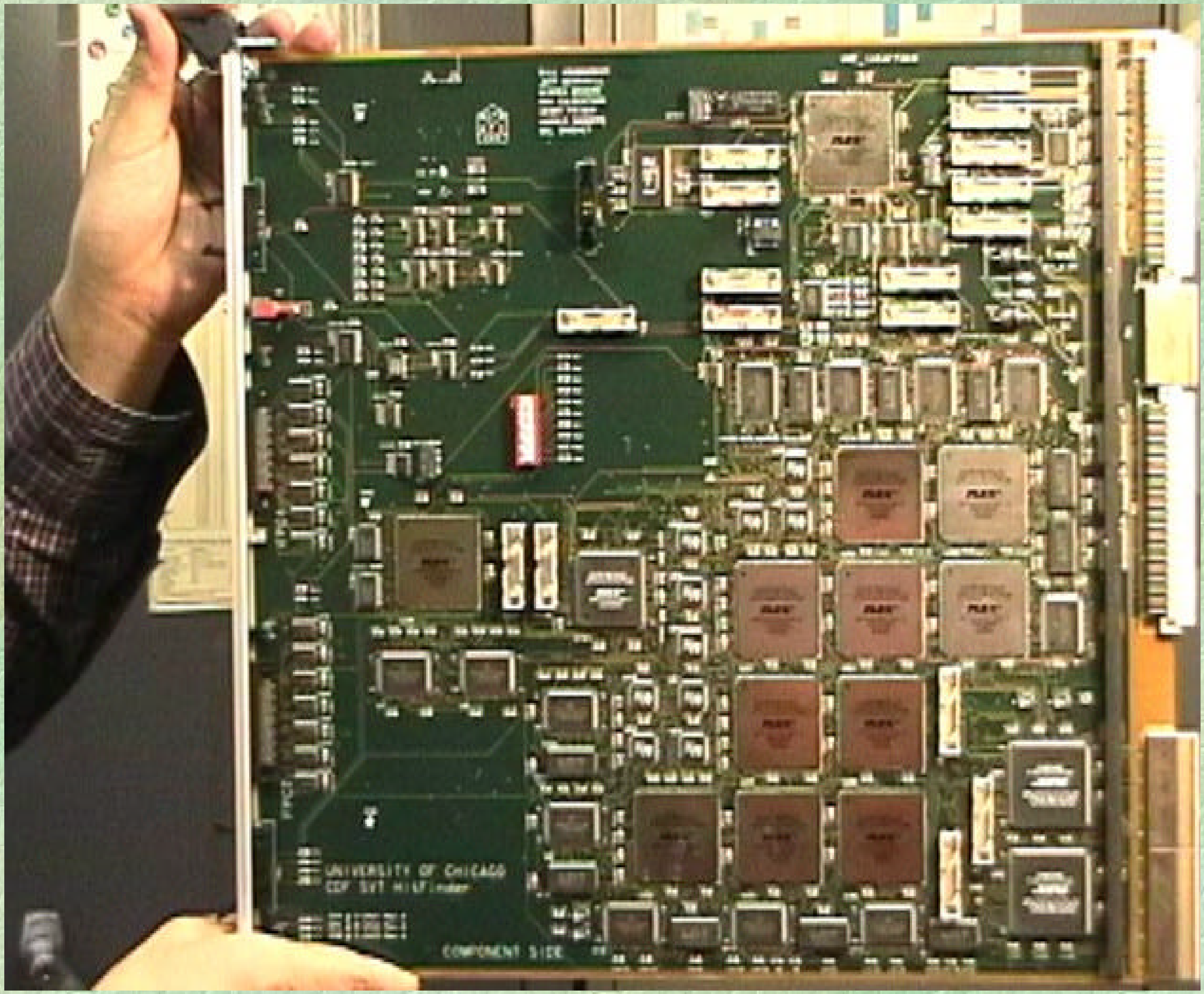
Hit Buffer architecture



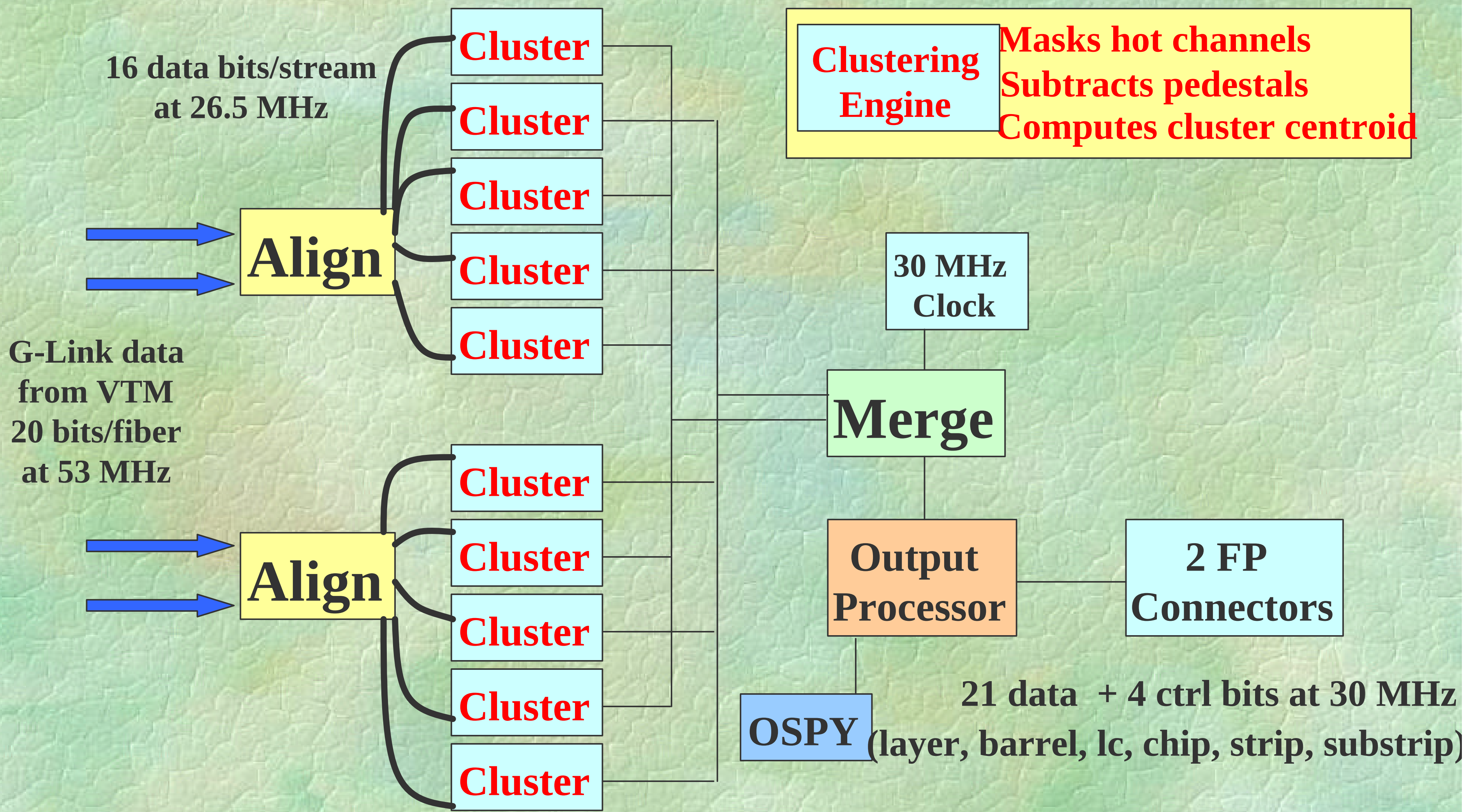
CDF Hit Buffer



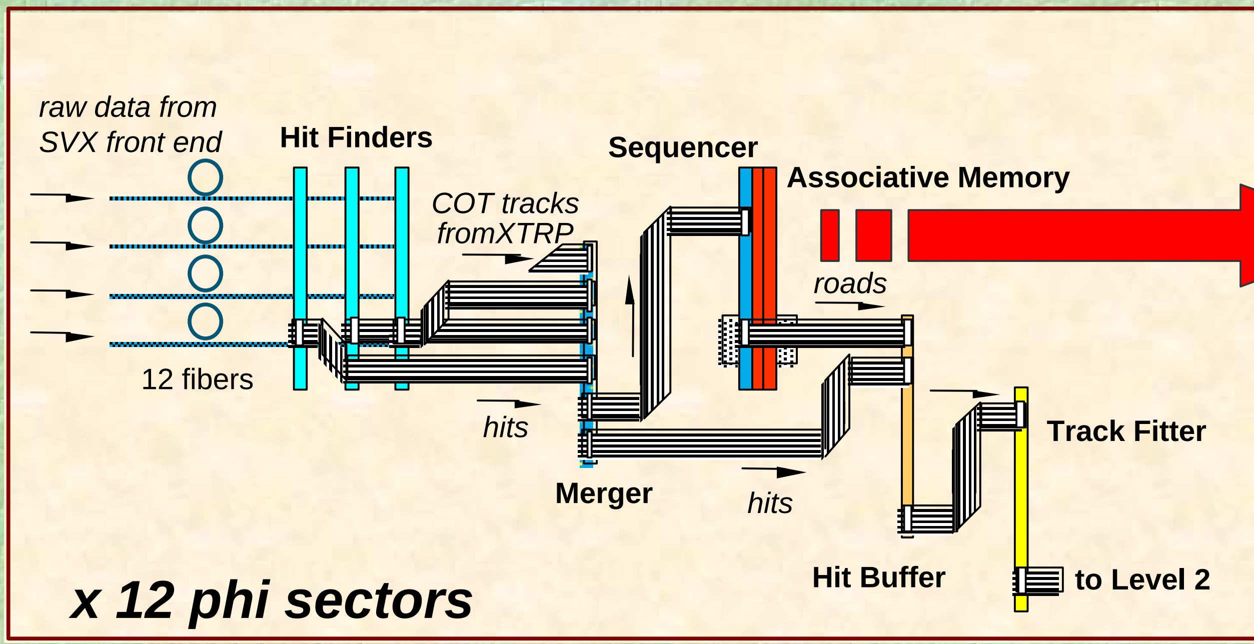
Hit Finder board

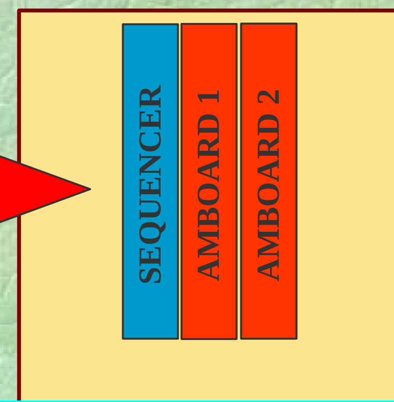


Hit Finder data flow



SVT data flow

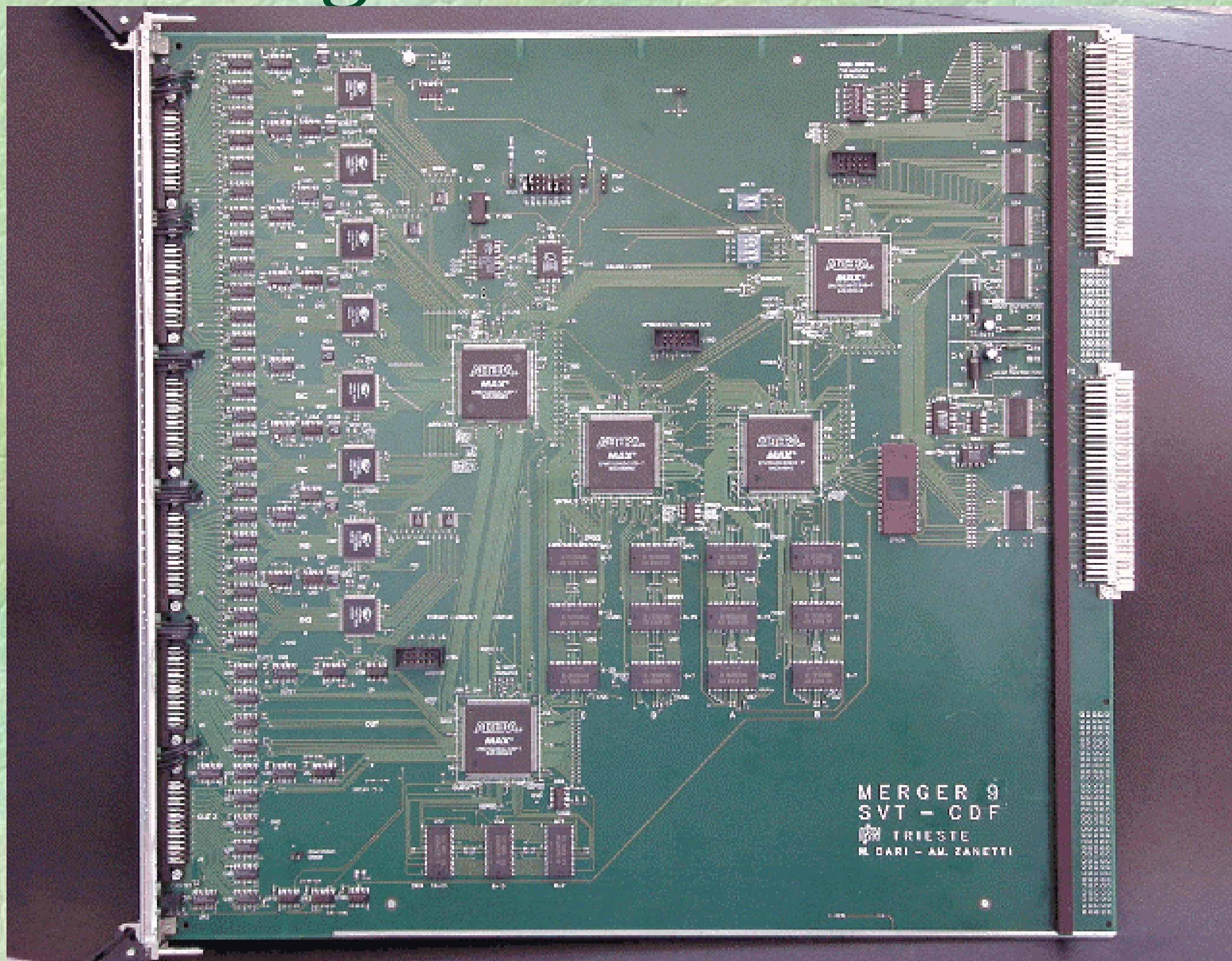




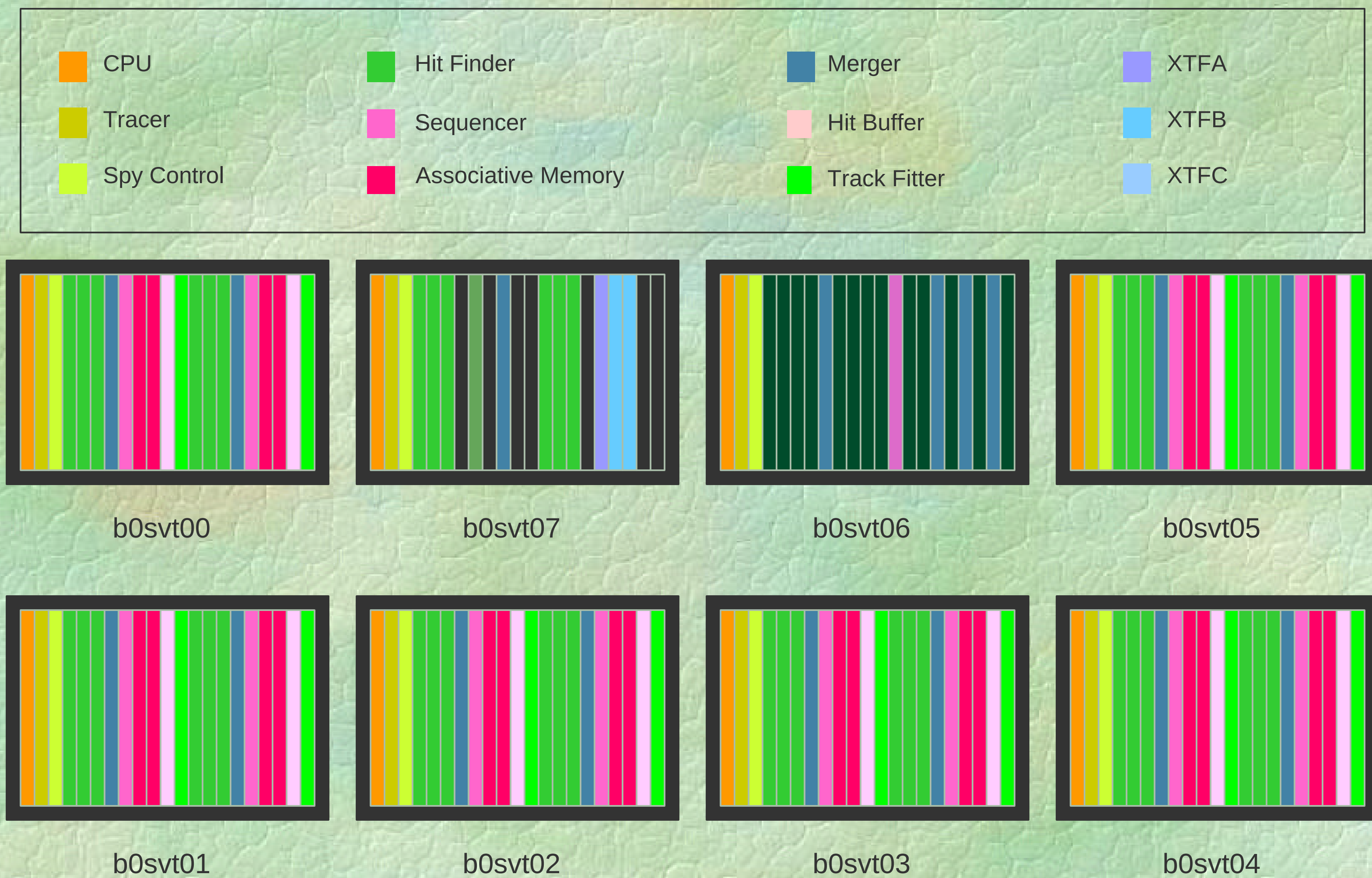
Pattern recognition: 1 AMS + 2 AMBOARD for each phi sector

- **9Ux400mm Eurocard boards**
- **VME used for download/control/diagnostics.**
- **Data flow on dedicated point-to-point cable connections**
- **The sequencer board is the "brain" of the associative memory system**
- **Sequencer and Amboards are connected via a custom P3 backplane**
- **Up to 4 amboards can be driven by one sequencer**

SVT Merger board

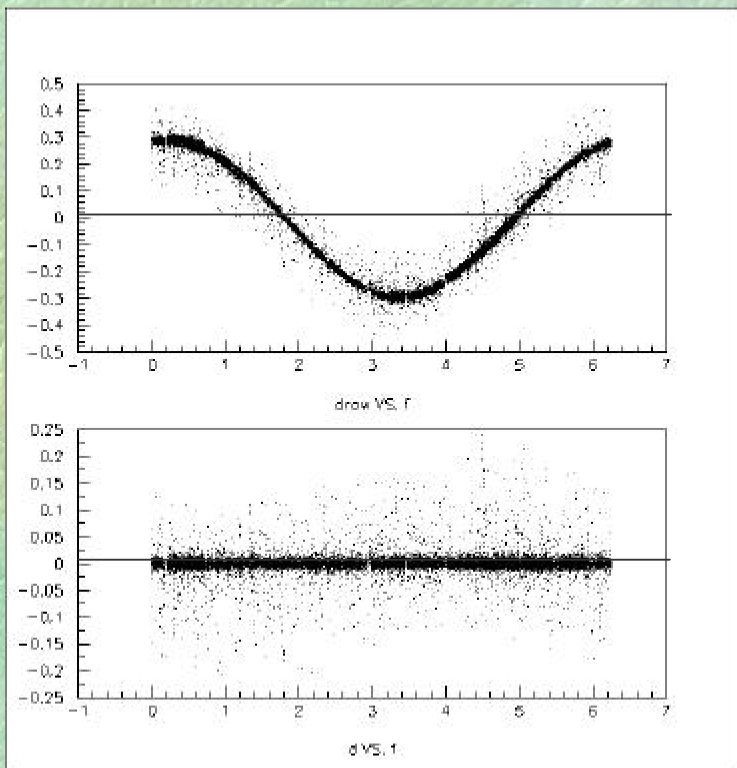


SVT: board and crate layout



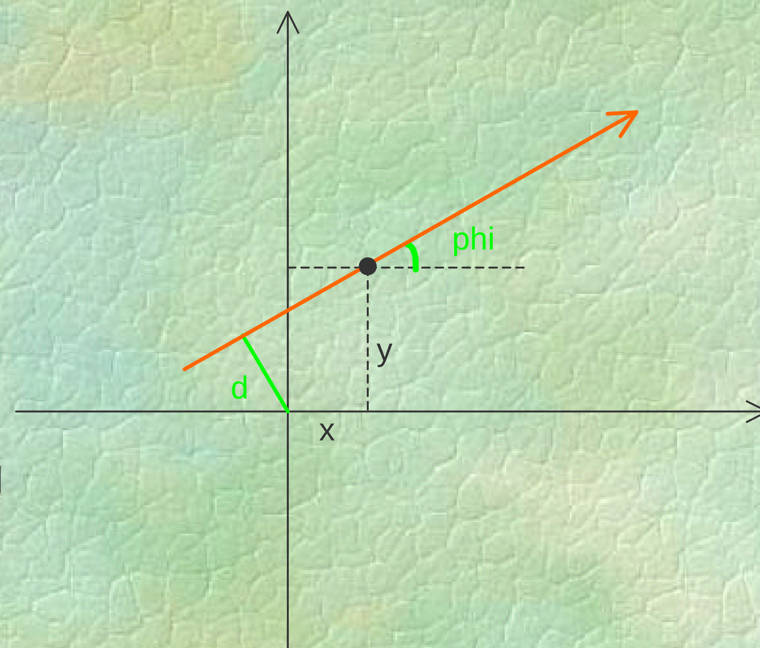

EAST

Beam position effect:
Impact parameter vs. phi



Raw

Subtracted

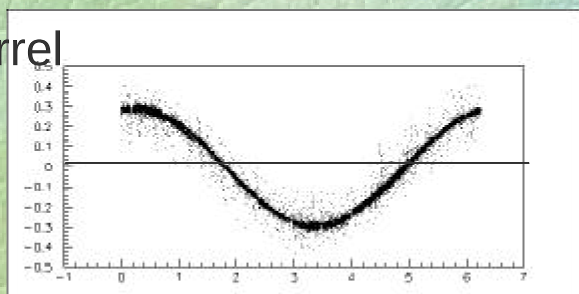


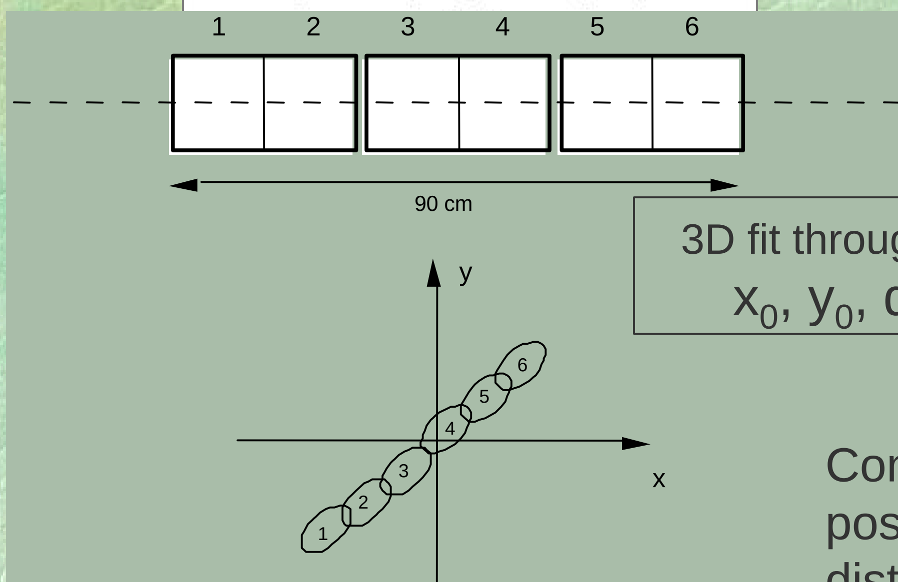
$$d = y \cos(phi) - x \sin(phi)$$

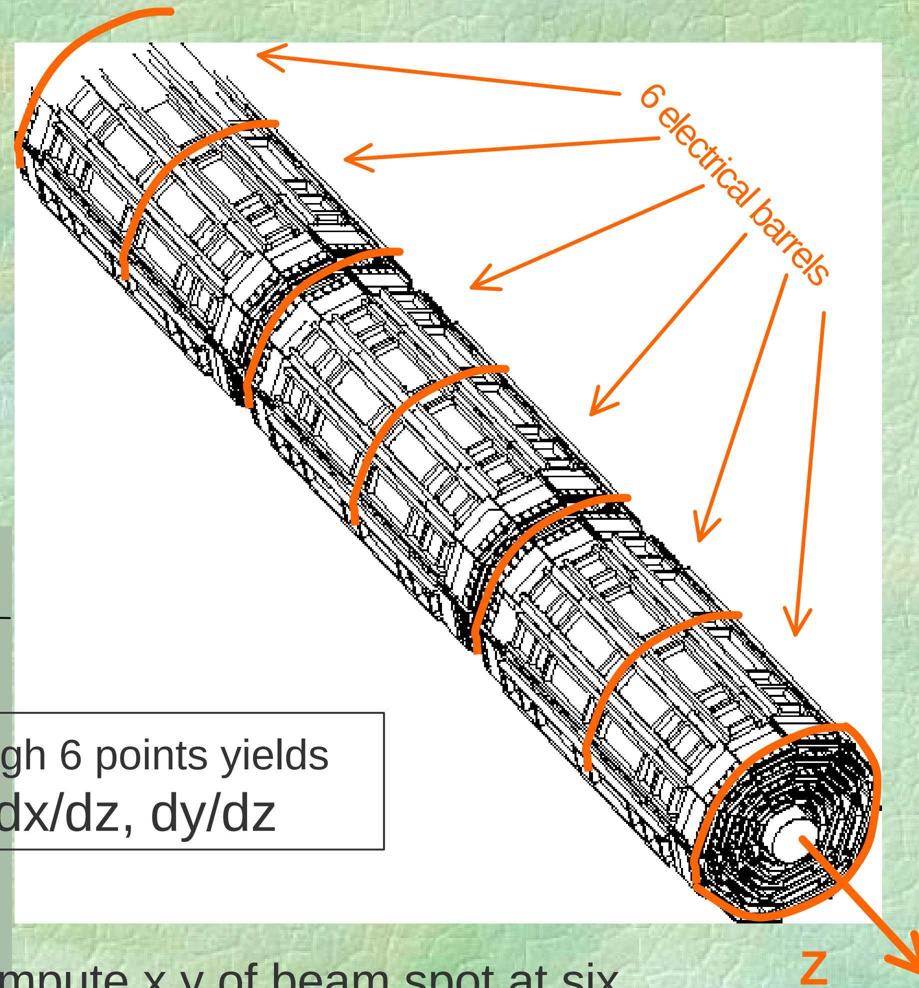
Online 3D beam position

Measuremente delivered to GB for on-line subtraction and to Accelerator Control

In each barrel





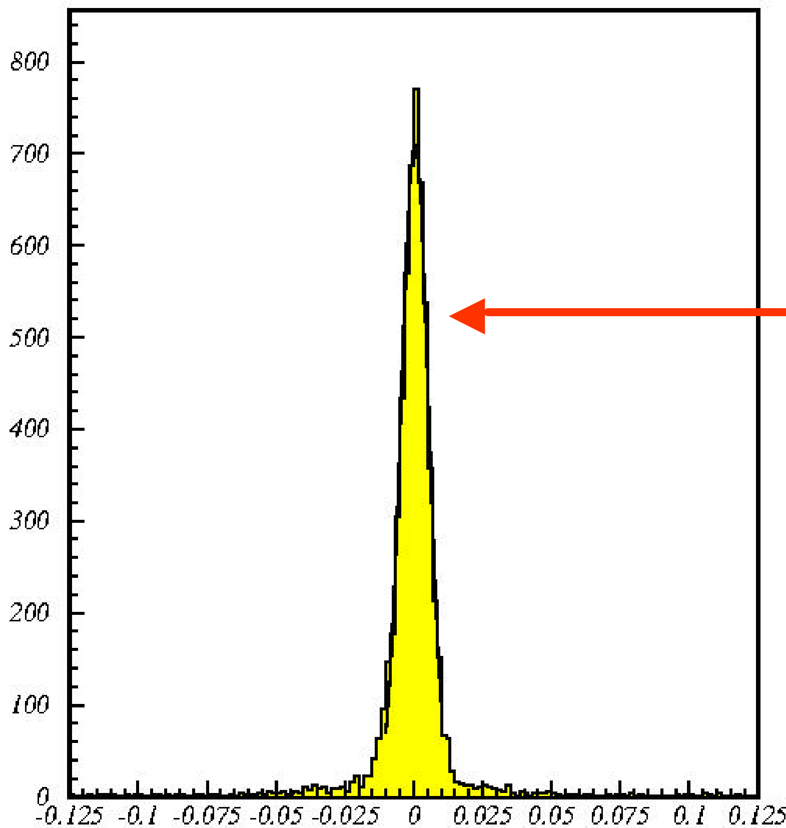


3D fit through 6 points yields
x_0, y_0, dx/dz, dy/dz

Compute x,y of beam spot at six positions in z using tracks from six distinct “electrical barrels”

Beam profile as seen by the trigger

Impact parameter distribution



This distribution is interpreted as the convolution of the actual transverse size of the beam spot with the impact parameter resolution of the SVT

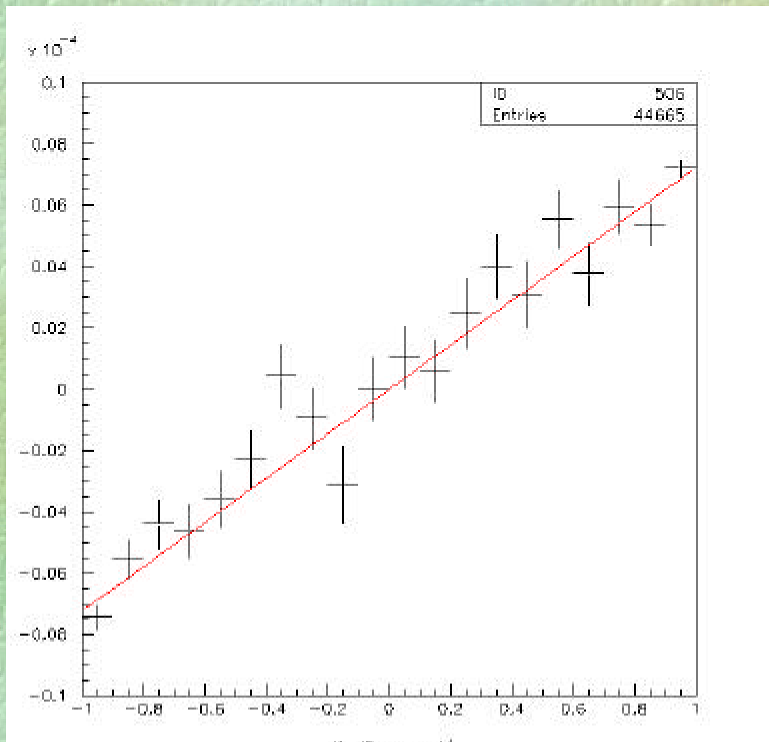
sigma ~ 48 um ~ 42 um $\oplus$ 23 um

SVT resolution   beam spot size

	beam	SVT	Total
sigma	23	42	48
rms	23	51	56

Two-track d correlation

See CDF note 4189



Cos(phi)

CDF/MEMO/TRACKING/CDFR/4189

Measuring beam width and SVX impact parameter resolution

S. Donati, L. Ristori

Introduction

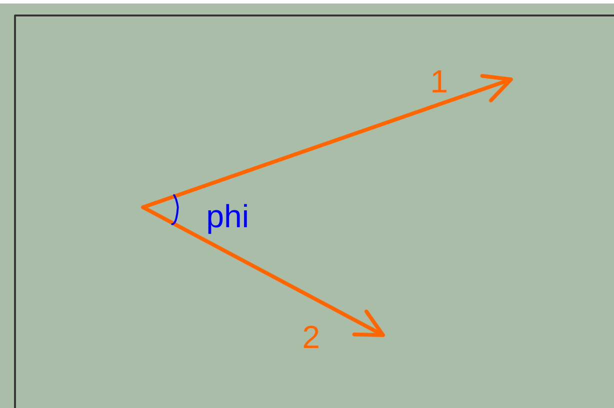
The observed impact parameter distribution of SVX tracks is the convolution of the primary vertex distribution with the impact parameter resolution and its width ($\sigma_d \sim 46\ \mu m$) is given by:

$$\sigma_d^2 = \sigma_{b'}^2 + \sigma_r^2 \qquad (1)$$

where $\sigma_{b'}$ is the actual beam width and σ_r is the impact parameter resolution. We propose a method to measure $\sigma_{b'}$ and σ_r separately from data.

The idea is to extract $\sigma_{b'}$ from the measurement of the correlation between impact parameters of track pairs exiting from the same primary vertex. Since σ_d is easily measured, impact parameter resolution (σ_r) is then determined by subtraction (Eq. (1)).

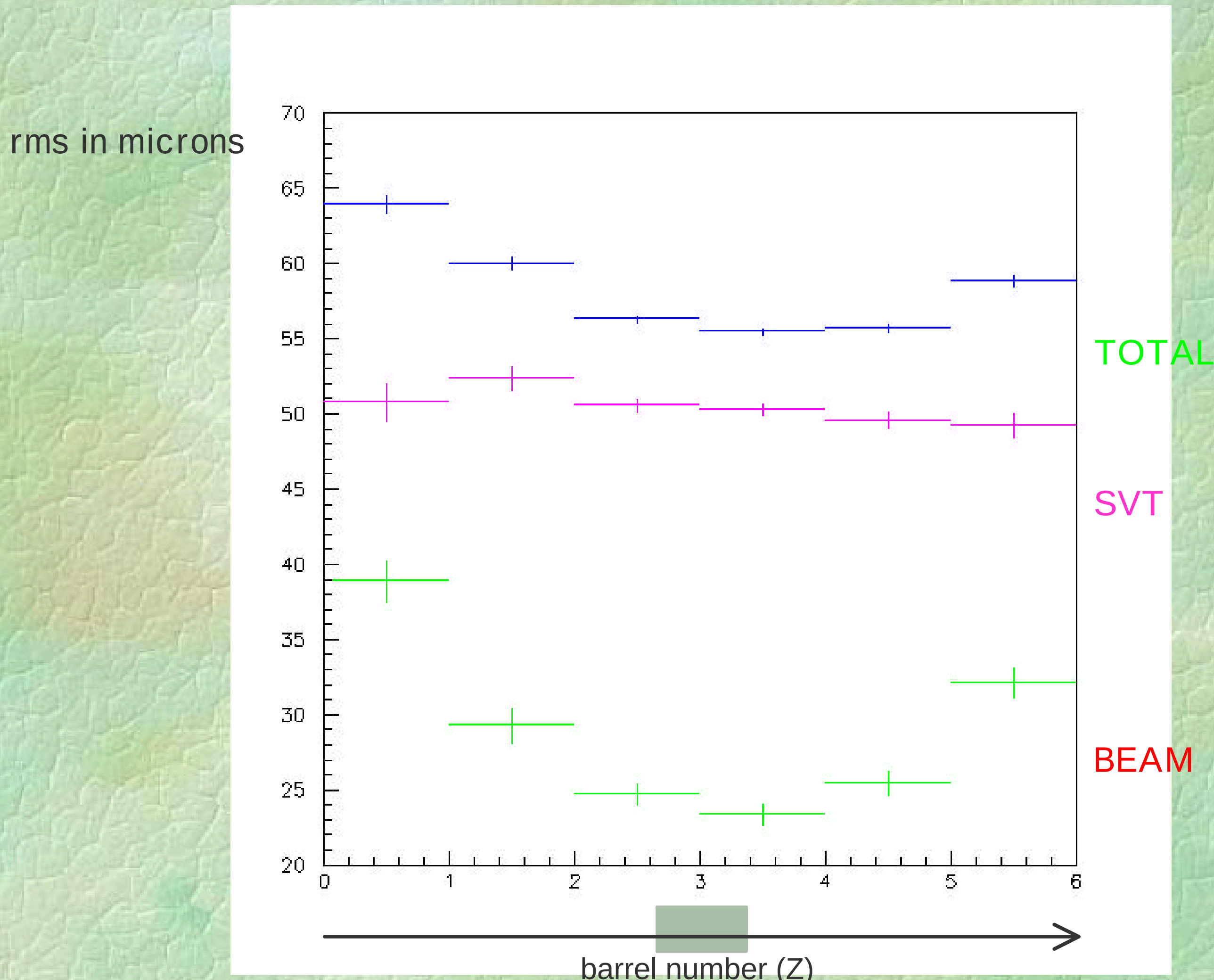
This method can also be used to determine $\sigma_{b'}$ and σ_r dependence on z and p_t.



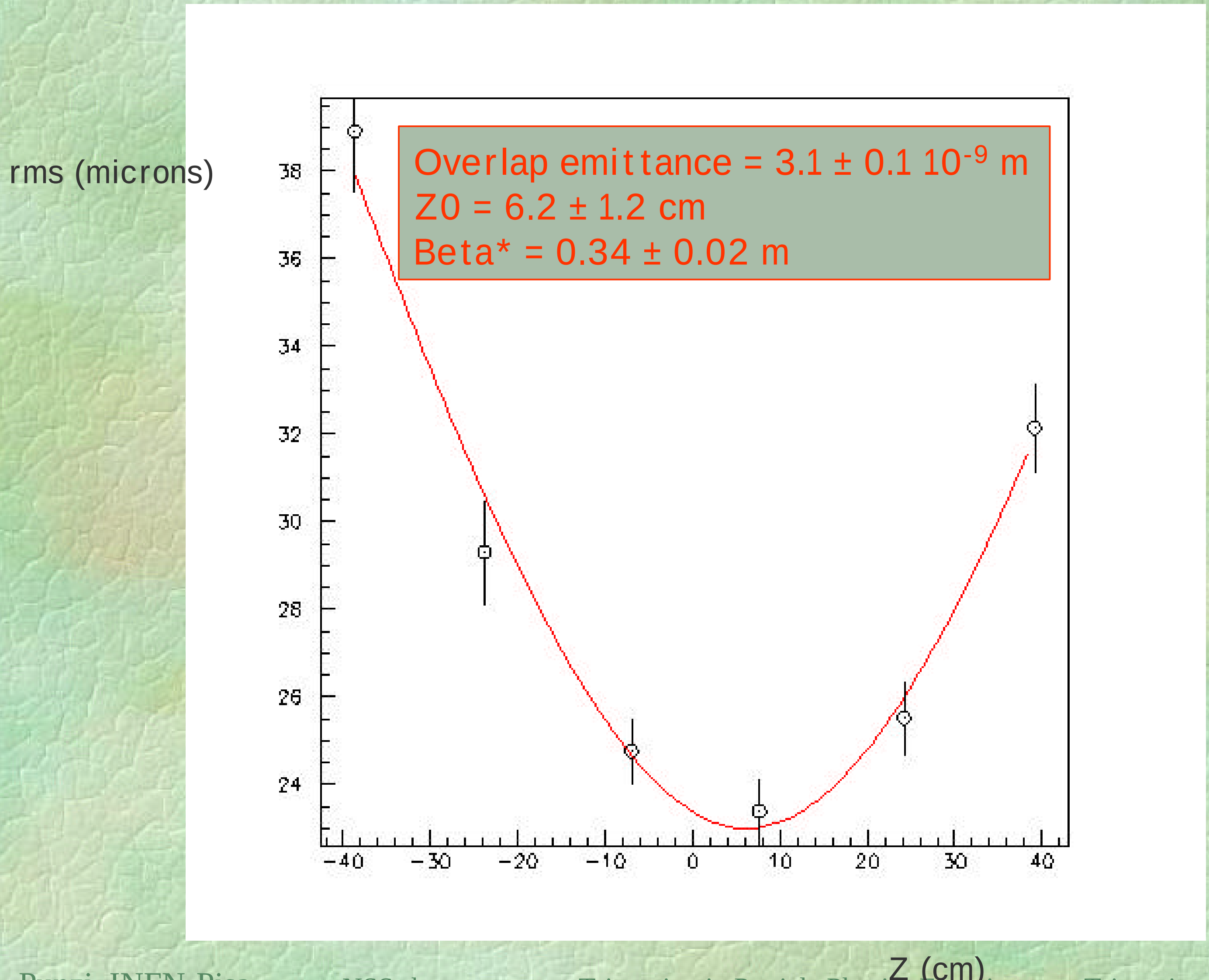
$<d_1 * d_2> - <d_1><d_2> = s^2 \cos(\text{phi})$

Intrinsic beam width

SVT + BEAM = TOTAL

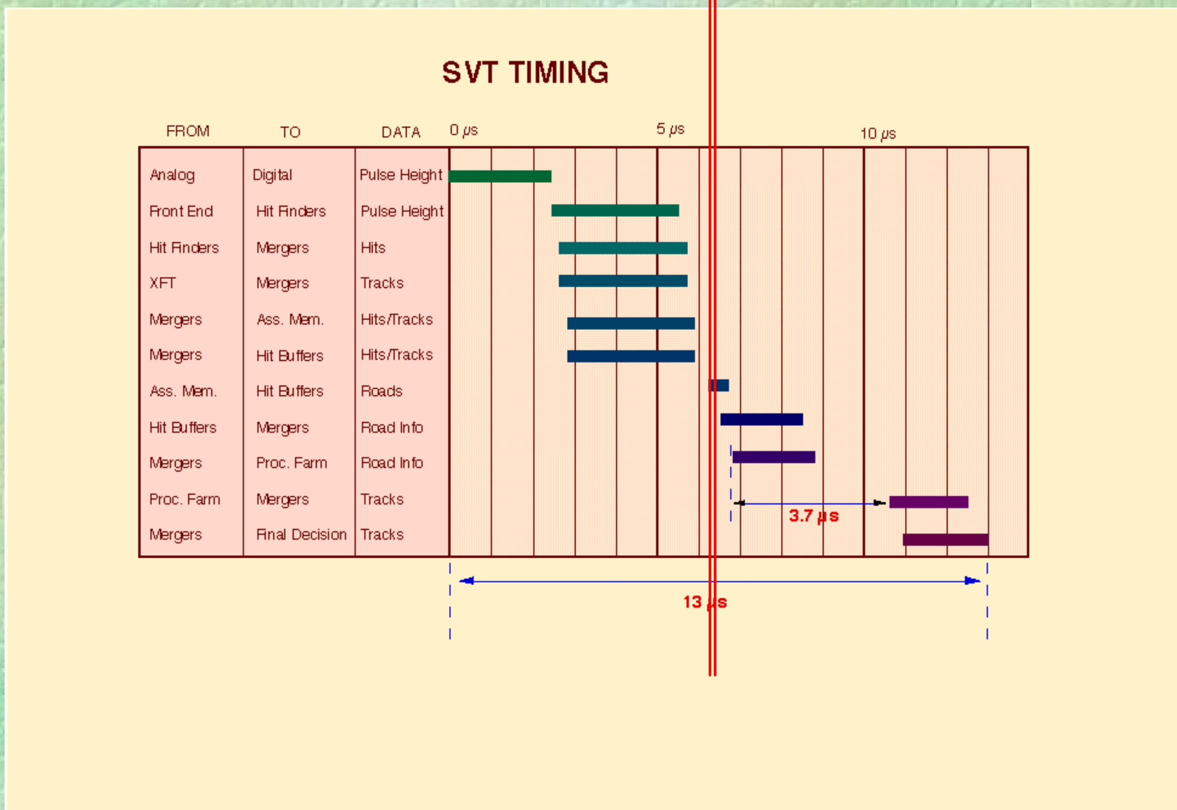


Intrinsic beam width



Timing

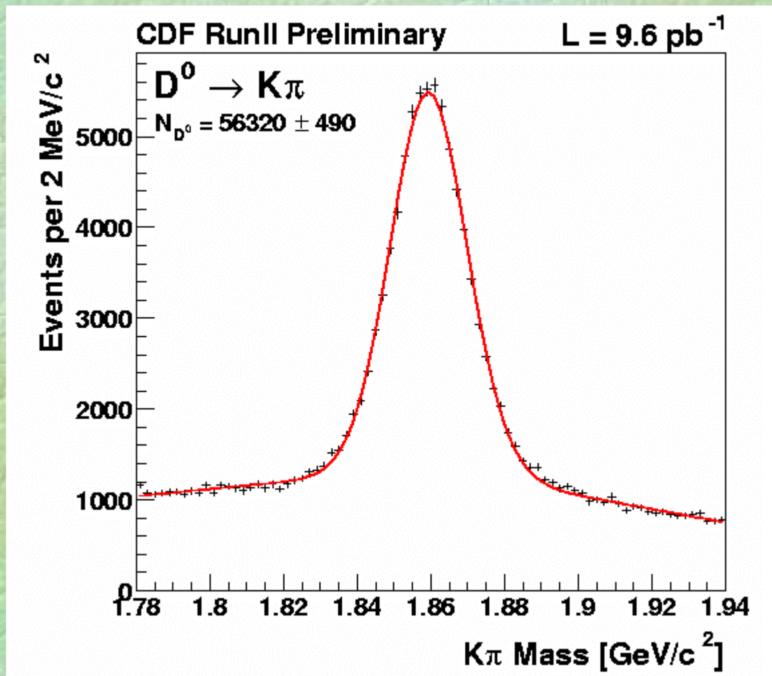
StepI StepII

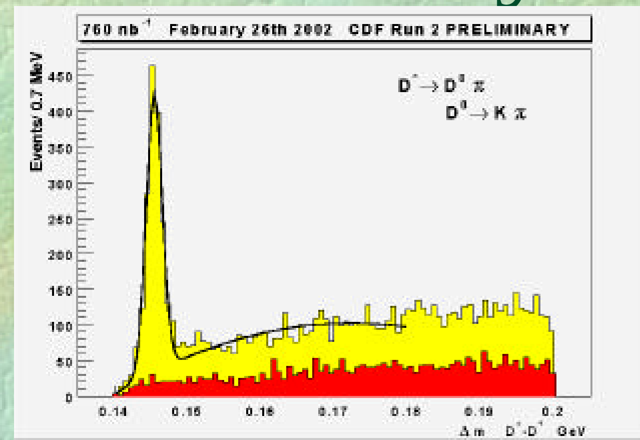


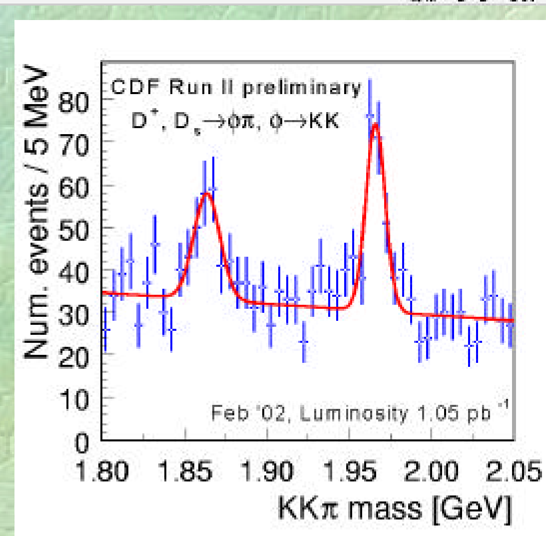
Prediction of SVT execution time from design document CDF3108 – Nov 1994

SVX readout	SVT proc.	Total (us)	
2.5	10.5	13	predicted
9	13	22	actual

Results: Hadronic Charm decays!



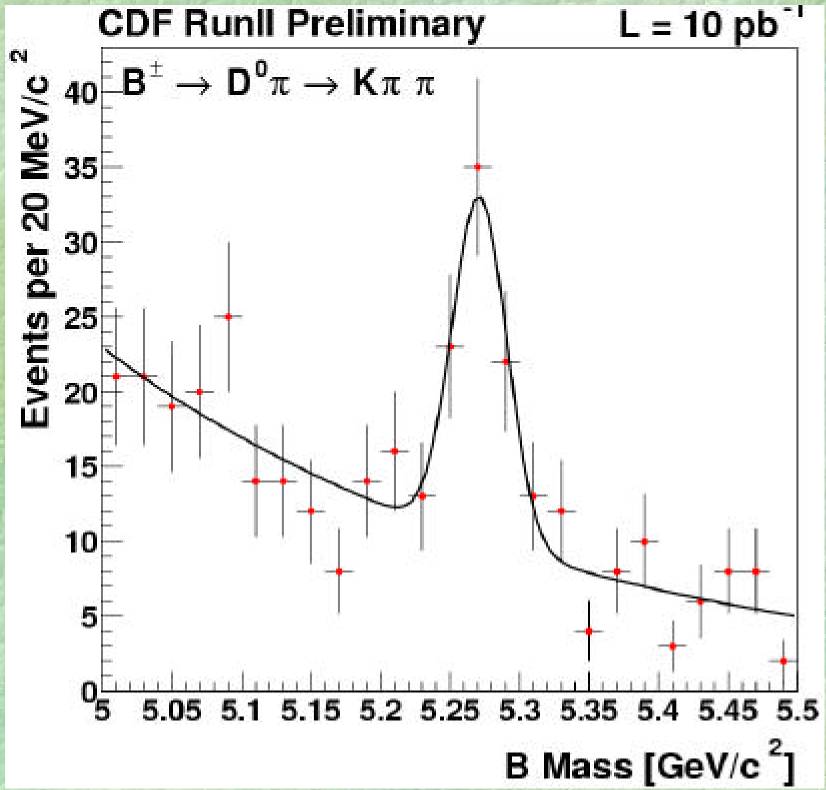


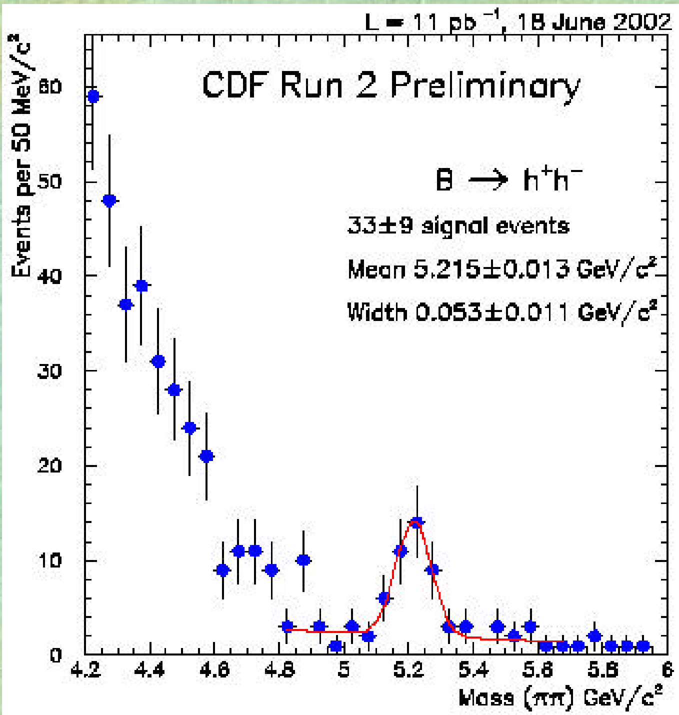


No lepton requirements !

Get as many B from hadronic D sample
than from J/ψ - a whole new window to B physics thanks to V-trigger

Hadronic B decays !

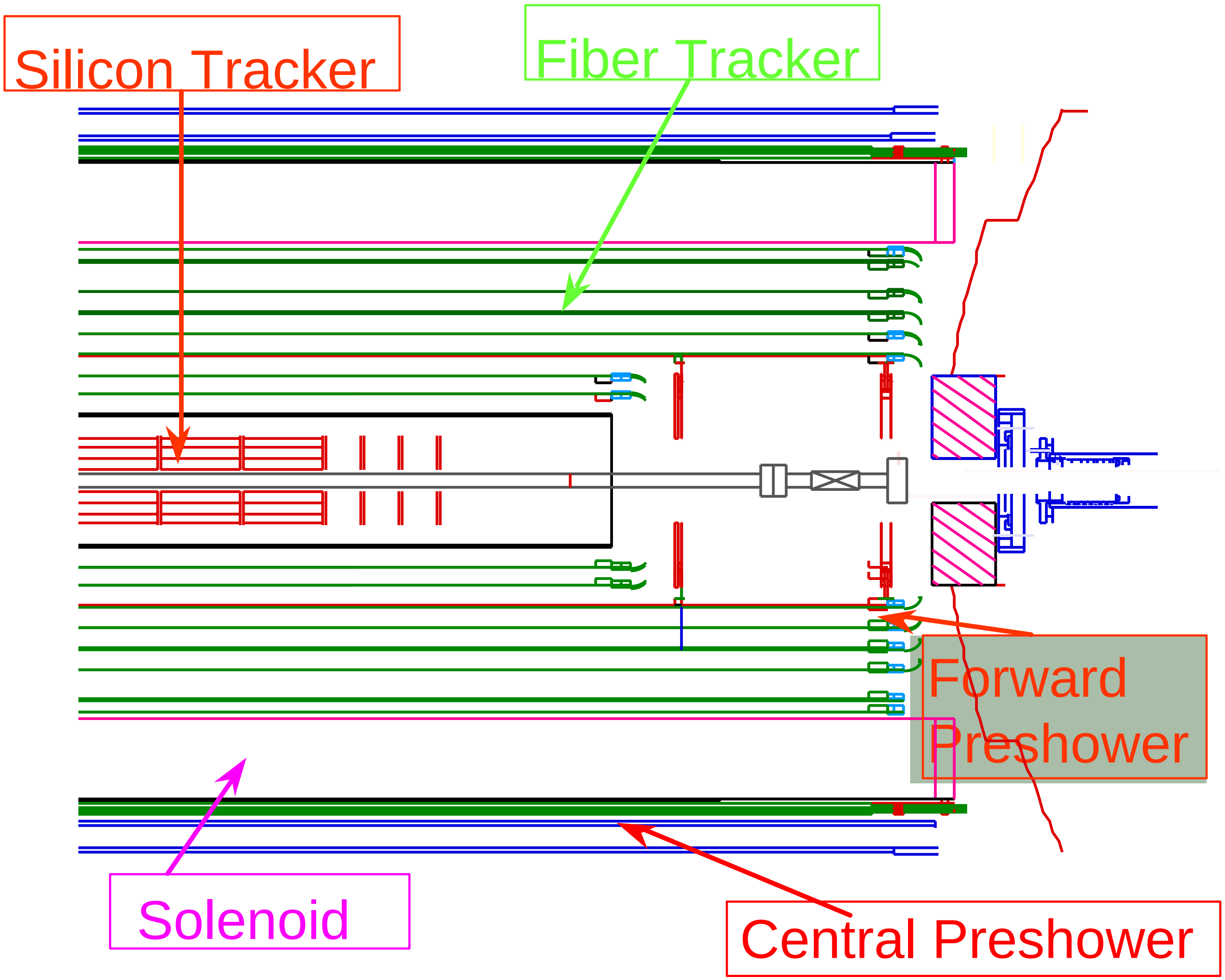




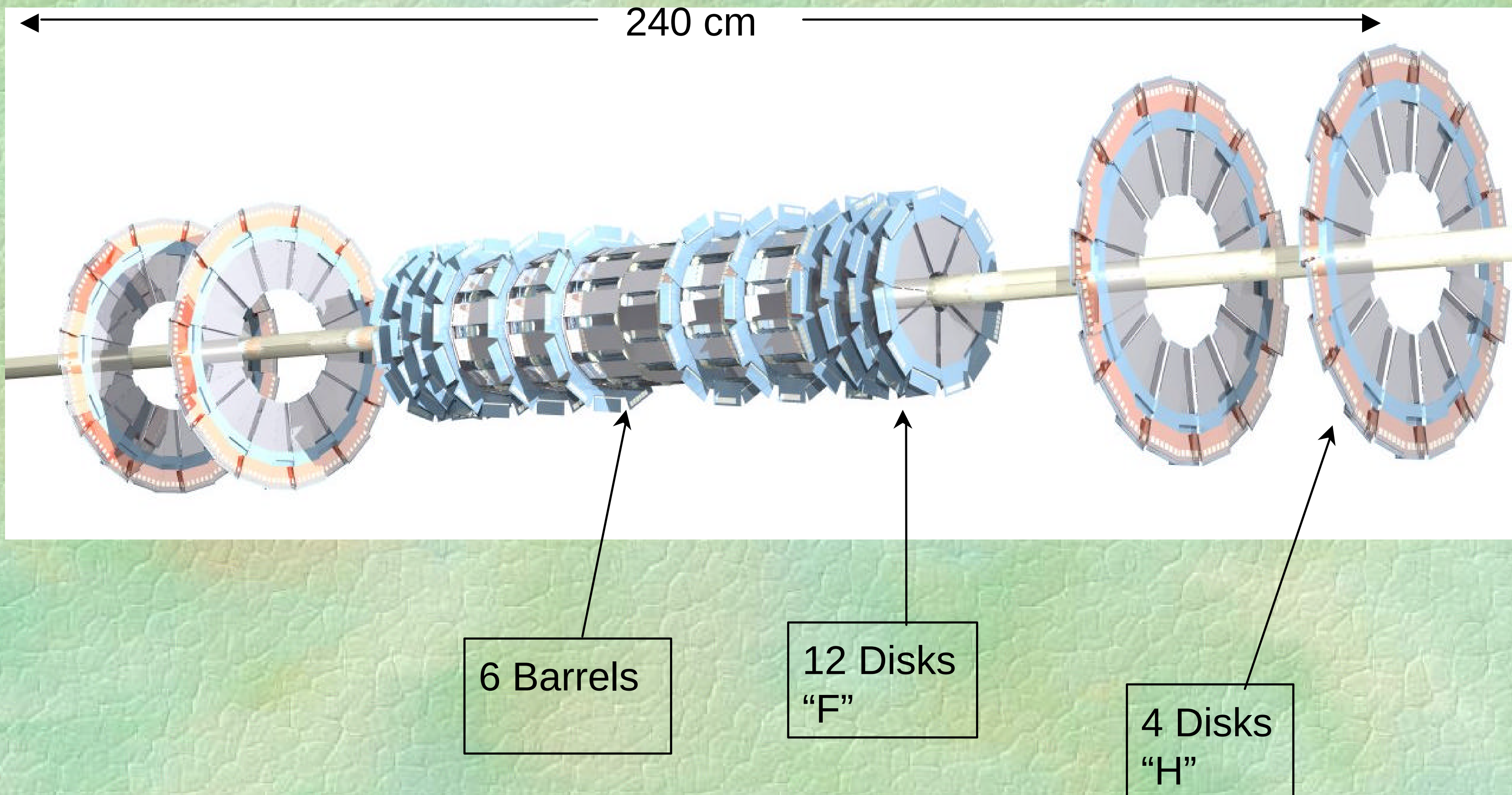
Impact parameter trigger at DØ

- Tevatron experiment, similar goals and boundary conditions as CDF
- Similar trigger design, but younger project: technological differences
- Massive use of powerful FPGA - makes headlines of Xilinx Xcell journal

D0 Central Tracker



Silicon Microstrip Tracker SMT

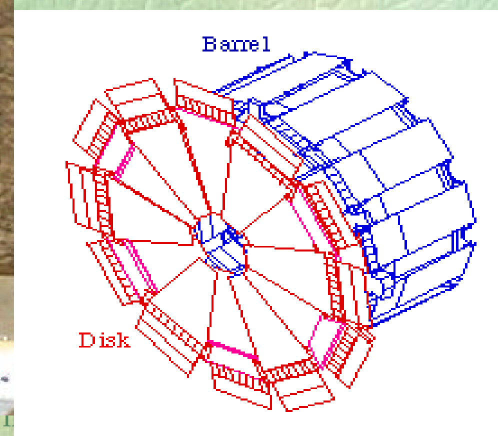


Read-out: SVX-II chips 800.000 channels

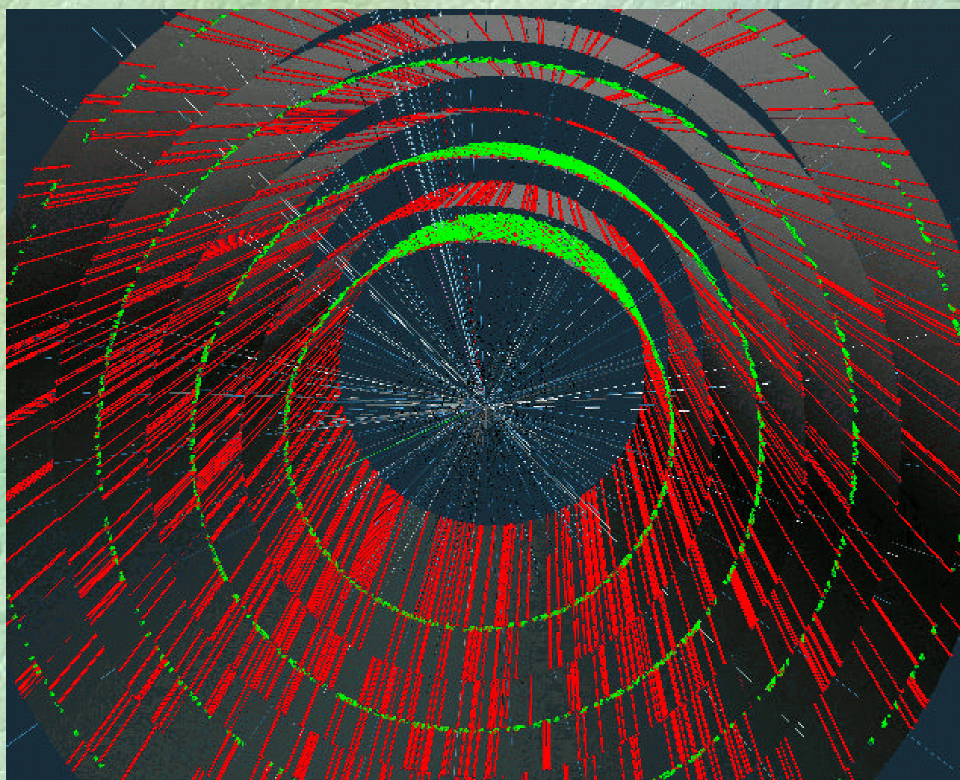
Hit resol. 10um, secondary vertex resol. 35um (r,phi) ; 80um(r,z)

ring on detached vertices

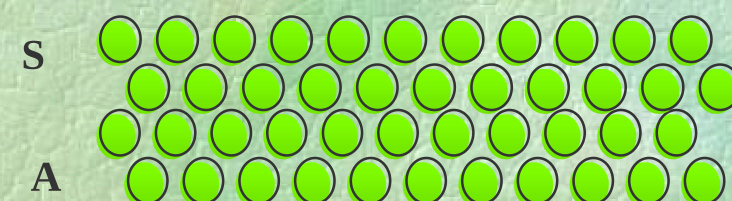
SMT Barrel



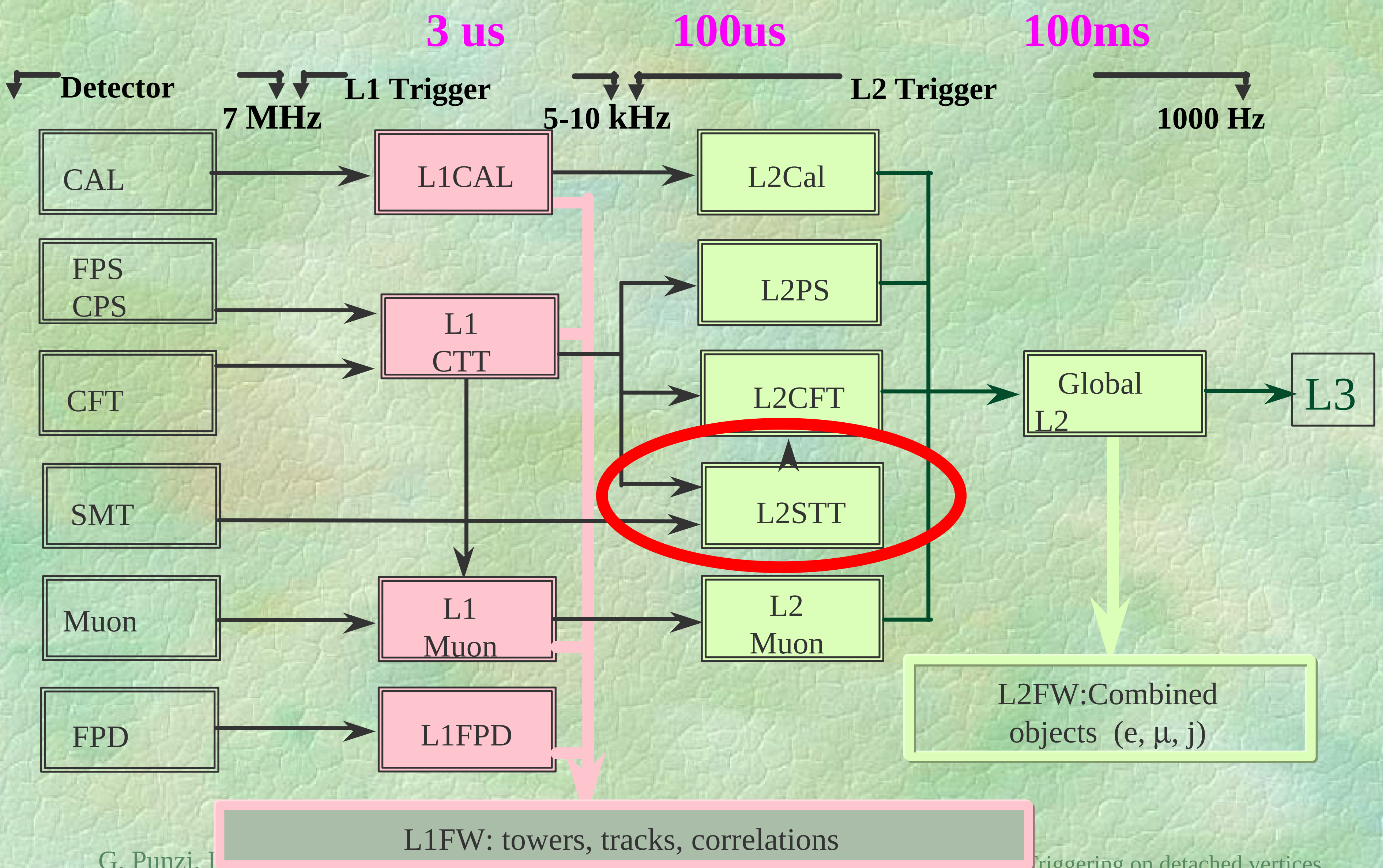
Central Fiber Tracker



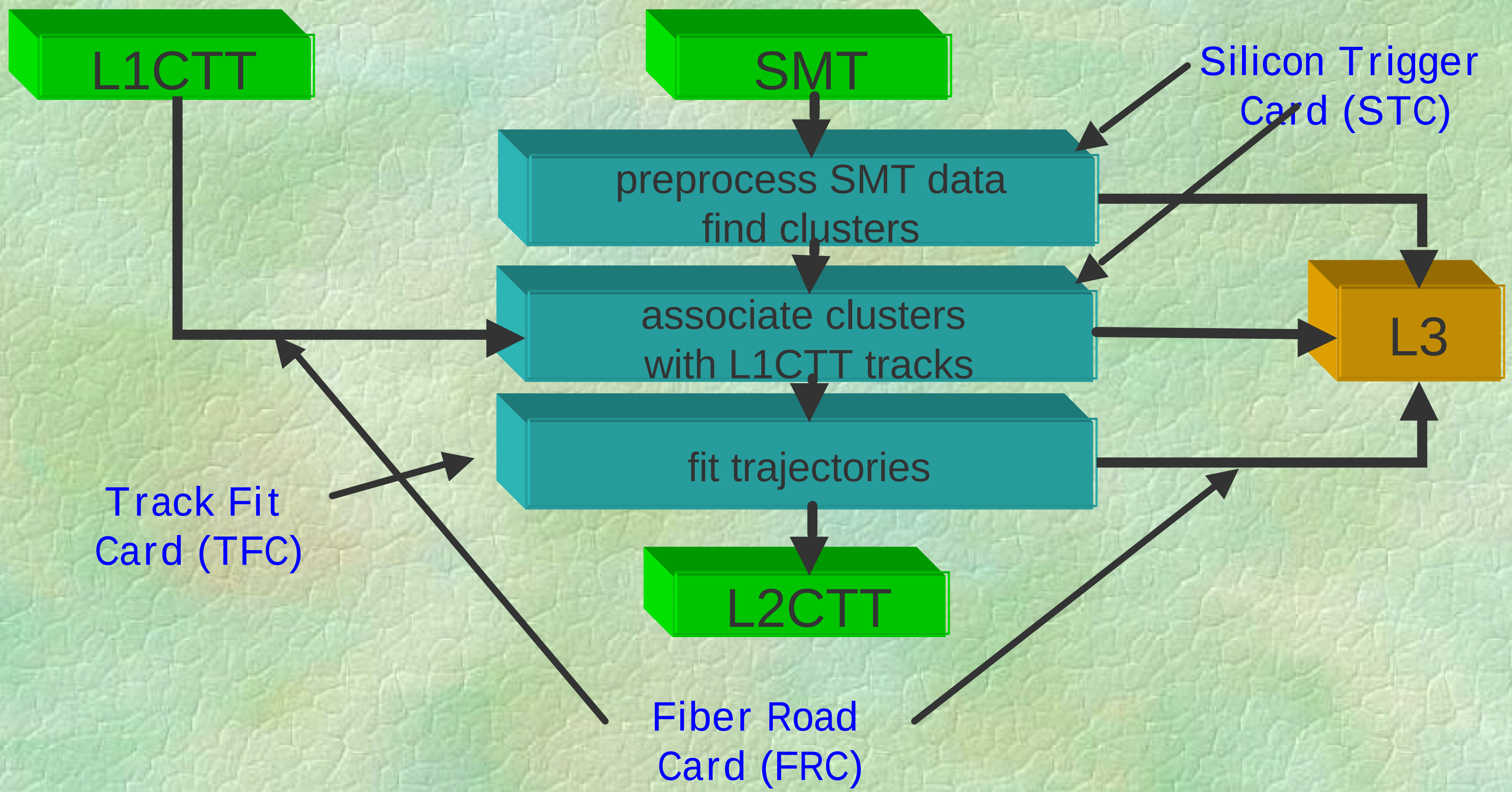
- 16.000 channels
- Read-out: SVX-II chips
- Fast enough for L1
- 2.6 m scintillation fibers, VLPC readout + 10m waveguides
- Mounted on 8 cylinders 20<r<50 cm
- 8 alternating axial and stereo doublets (2deg pitch)



D0 Trigger System



Overview of STT



3 custom VME boards mounted on common custom motherboard

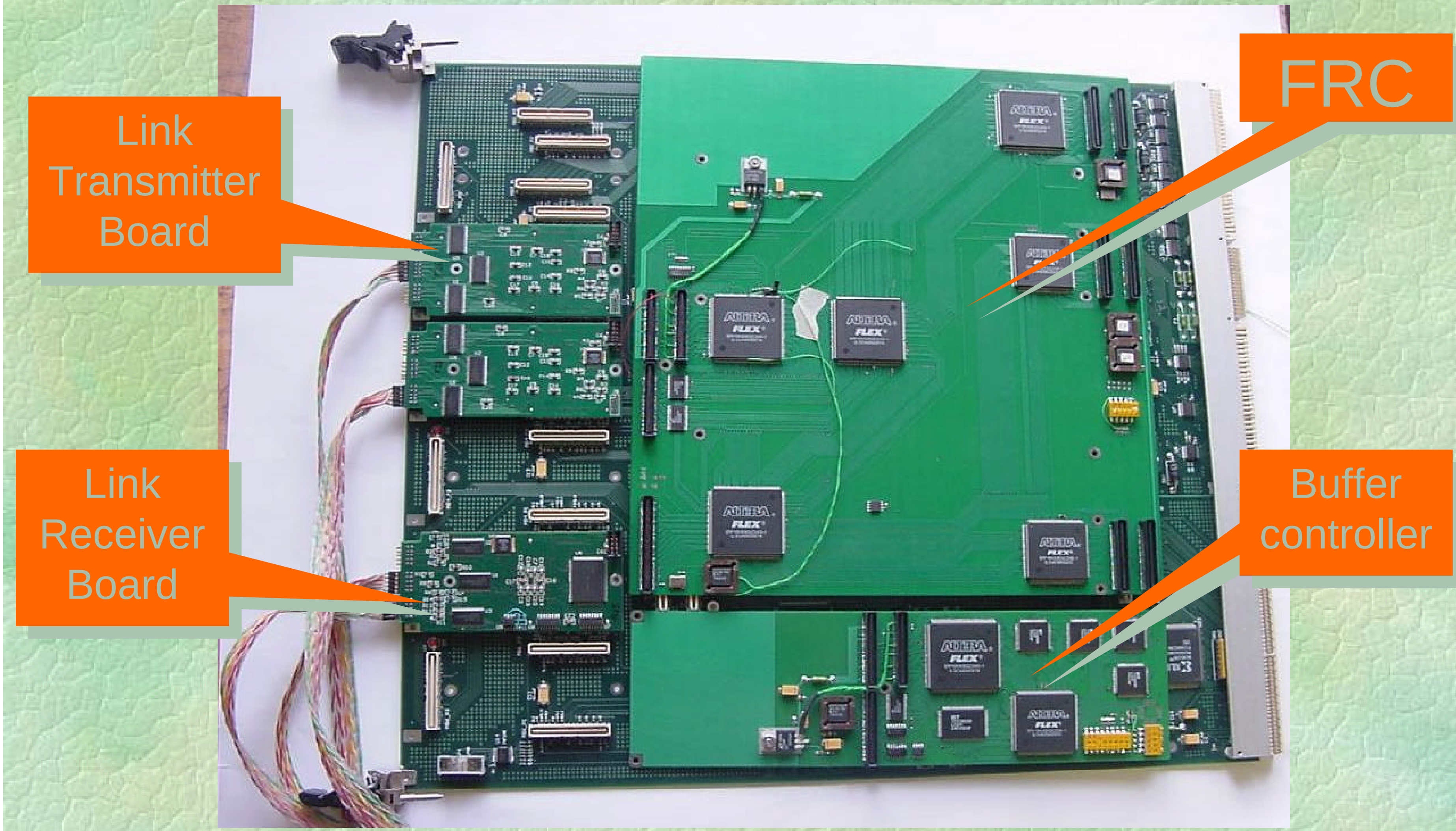
L2STT Card Flavors

- fiber road card
  - receive SCL
  - fan out L1CTT data
  - manage L3 buffers
  - arbitrate VME bus
- silicon trigger card
  - preprocess SMT data
  - associate hits with CFT tracks
- track fit card
  - fit trajectory to hits
- CPU
  - initialization
  - downloading
  - monitoring
  - resets
- VBD

Fiber Road Card

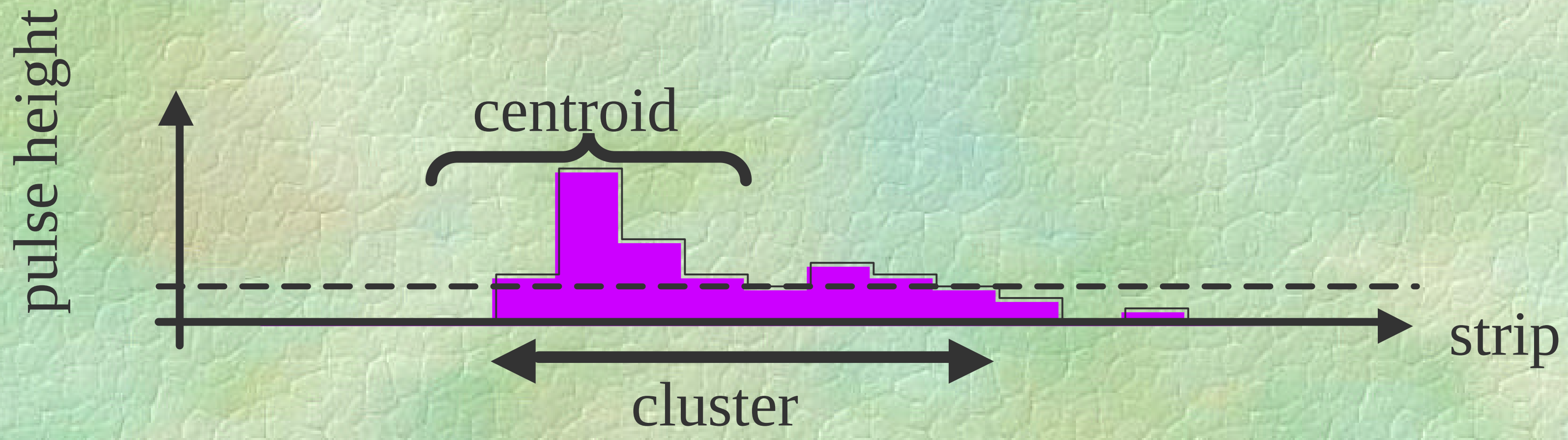
- Trigger receiver communicates with the trigger framework (SCL receiver card on motherboard) and broadcasts any control signals to the other cards (J3)
- Road receiver receives tracks from the Level 1 CFT trigger
- Trigger/road data formatter constructs the trigger/road data blocks and transmits this information to the other cards
- Buffer manager handles buffering and readout to Level 3
- Implemented in 3 FPGAs

Fiber Road Card (FRC)



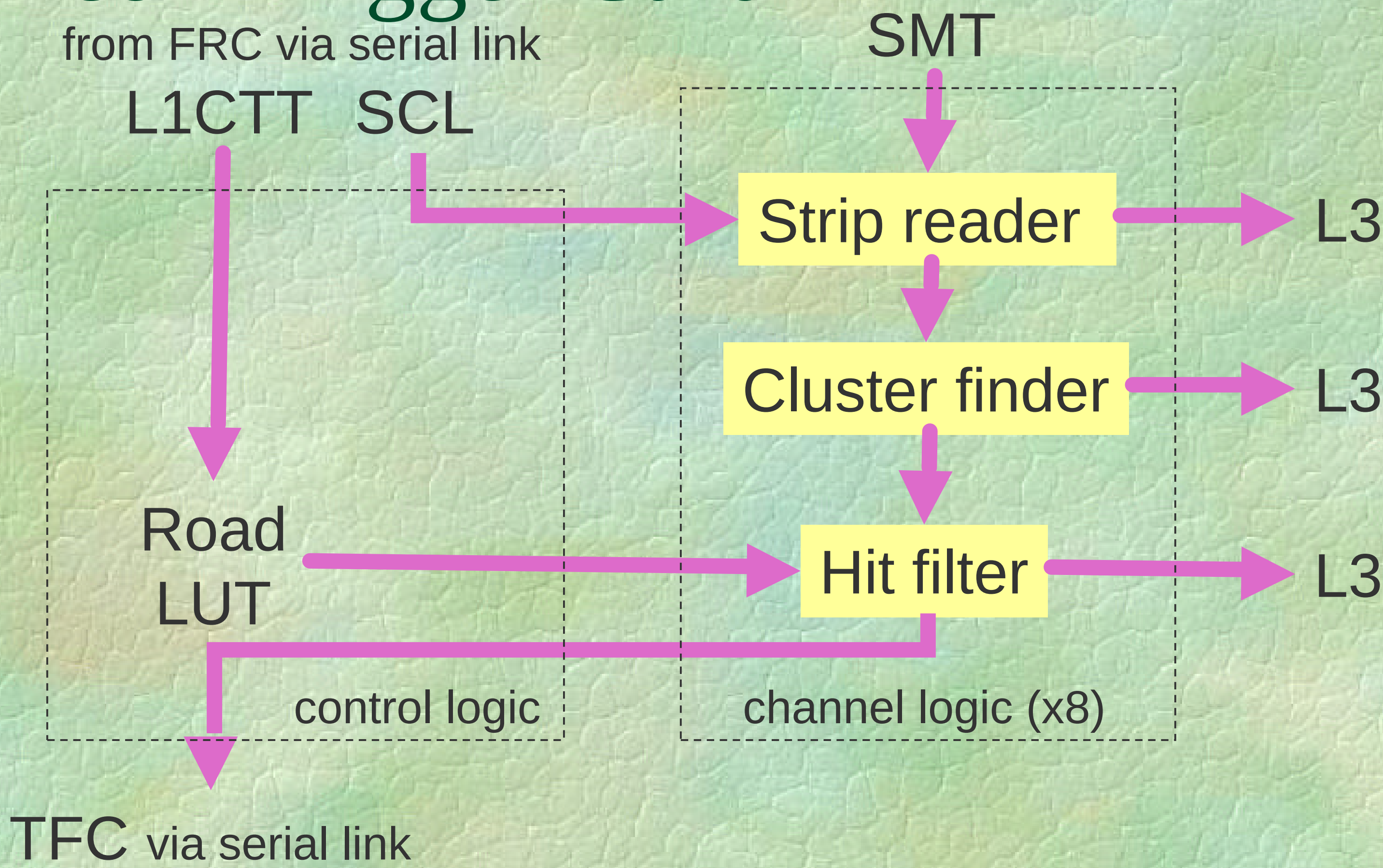
Silicon Trigger Card

- Bad strips are masked (LUT)
- Pedestals/gains are calibrated (LUT)
- Neighbouring SMT hits (axial or stereo) are clustered using FPGAs programmed in VHDL



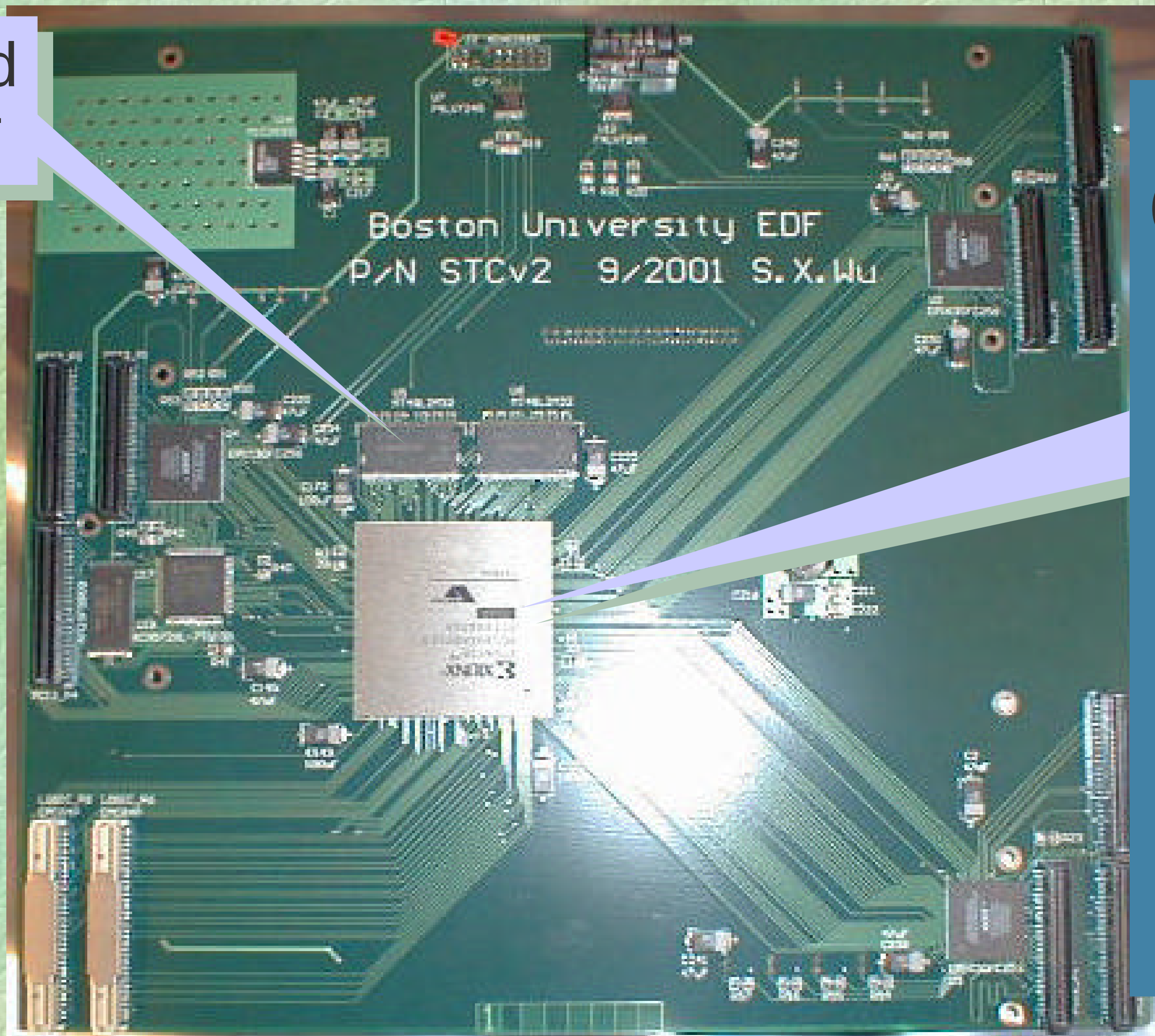
- Axial clusters are matched to ±1mm-wide roads around each CFT track via precomputed LUT

Silicon Trigger Card



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
track						$\frac{dE}{dx}$			sequencer							HDI			chip				centroid								

STC Prototype board



Road LUT

control logic
(8x) channel logic
(Xilinx Virtex E)
800k gates
1.1 Mbits RAM
560 pin BGA
$1200

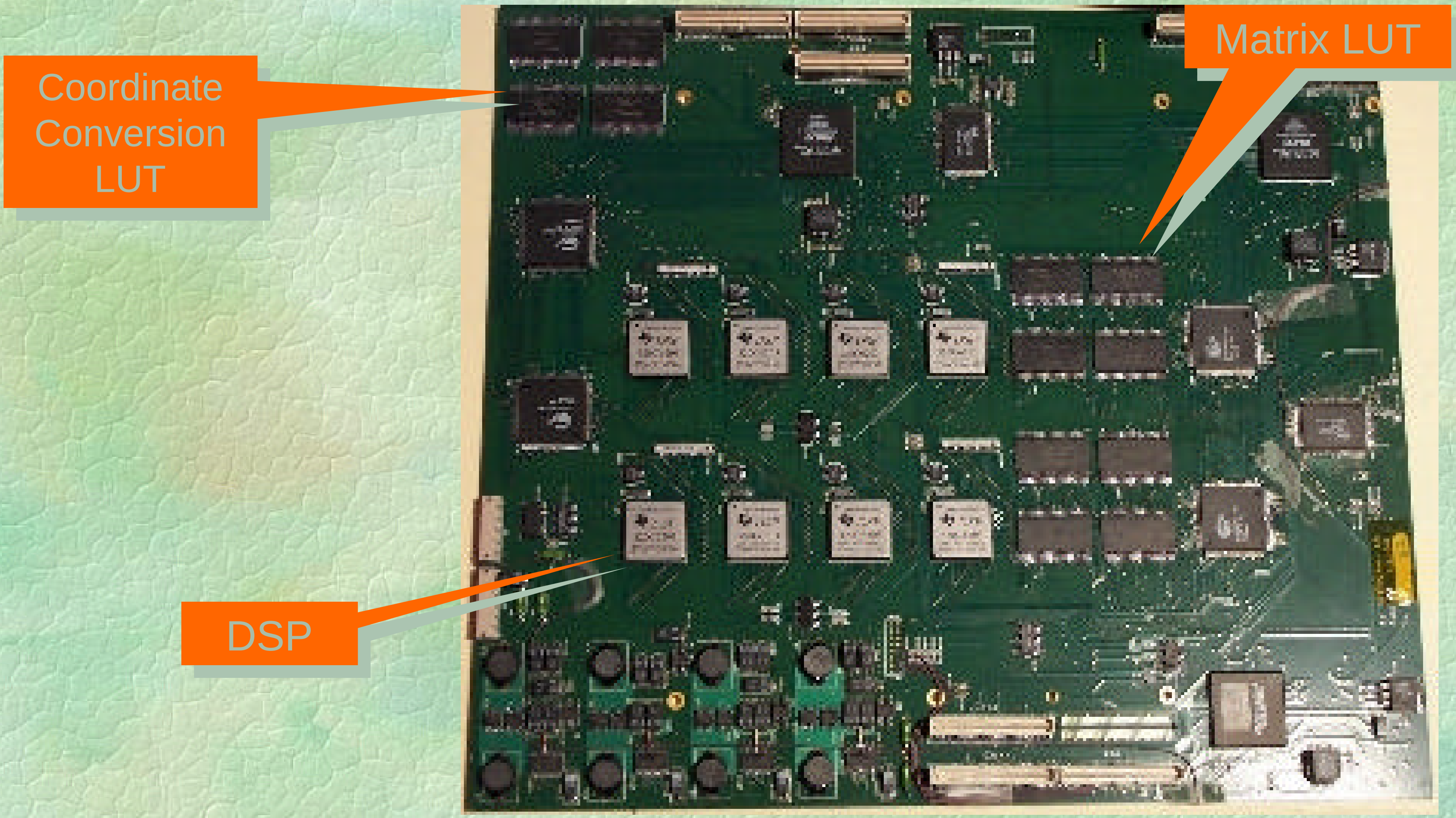
accommodates
all 8 channels
→need 1/STC

Track Fit Card

- Control logic (Altera FPGAs) maps each road to one of eight processors and handles I/O buffer management
- Processor (TI DSP) receives 2 CFT hits and r-φ SMT clusters in road defined by CFT track
- Lookup table used to convert hardware to physical coordinates
- C program on DSP selects clusters closest to road center at each of 4 layers and performs a linearized track fit:

$$f(r) = \frac{b}{r} + kr + f_0$$

Track Fit Card (TFC)



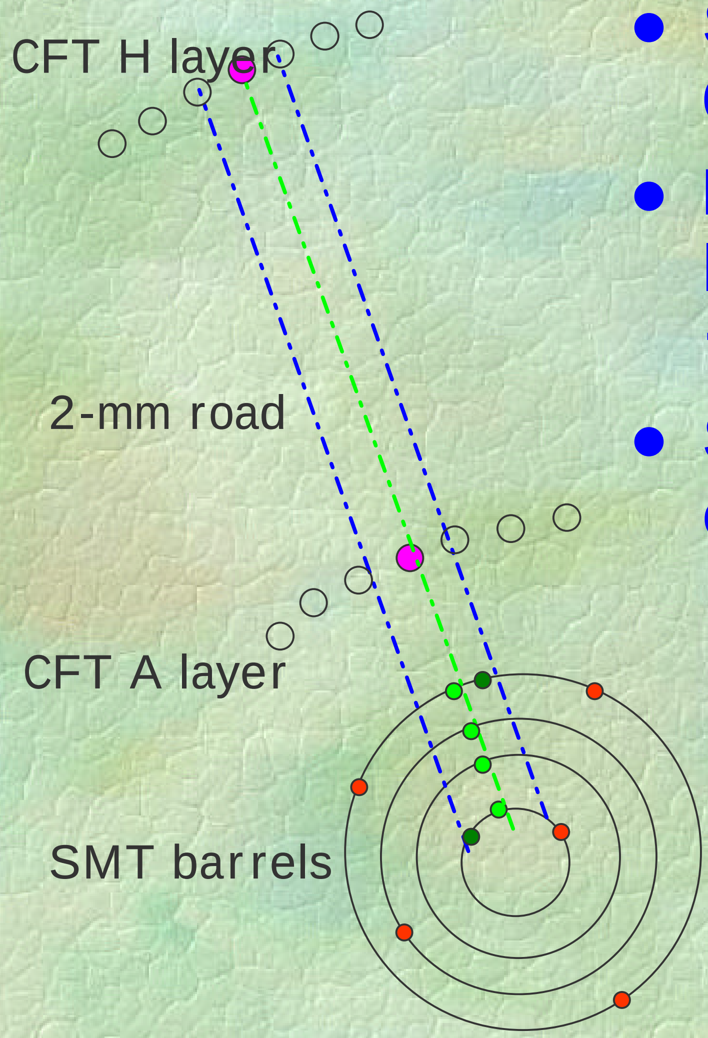
Track Reconstruction

- Formulate track equation in terms of hits (3 or 4 SMT + 2 CFT hits)
- With ϕ_1 as reference, use ϕ residuals in computation
- near-zero ϕ residuals allow use of integer arithmetic
- Matrix is precomputed and stored in a lookup table

☞ Expect 35 µm I.P. sigma (15µm res.+30µm beam)

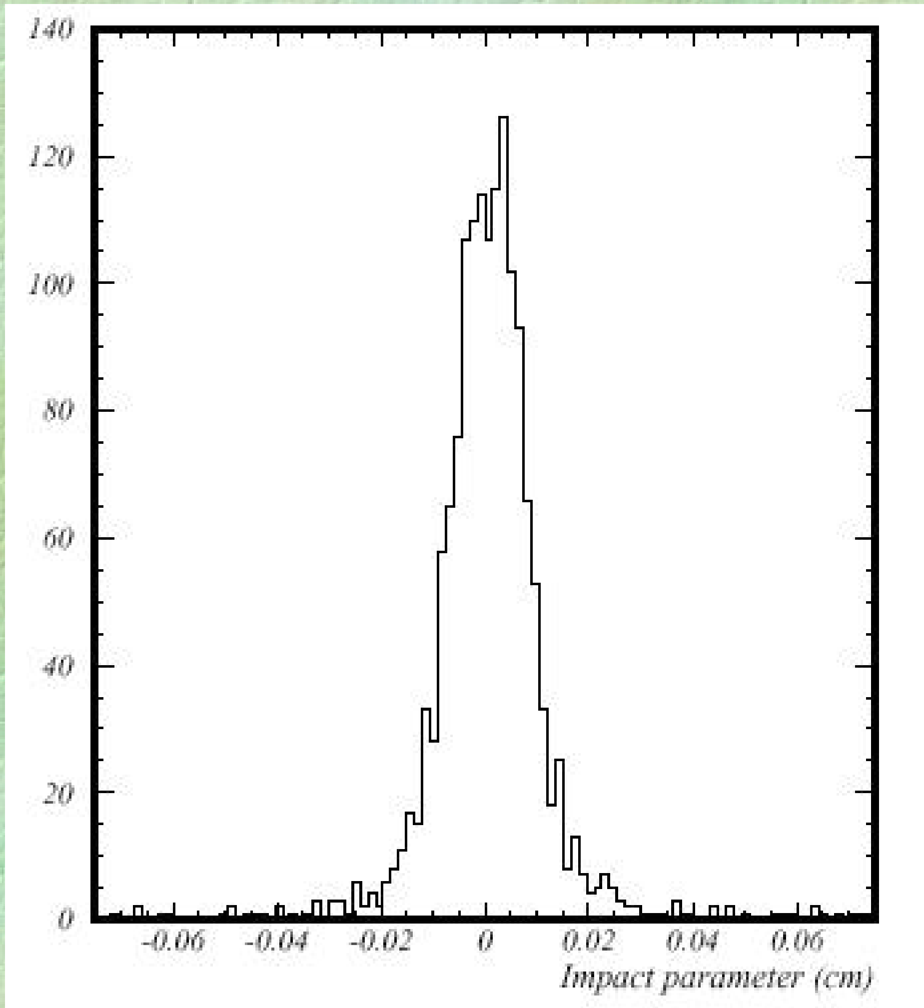
☞ Simulation predicts 25 µs average total execution time, adequate for D0 L2

Hit Filtering Algorithm



- Start from road defined by CFT track
- Look for hits in all four layers but allow hits in only three out of four layers
- Simpler than AM algorithm, easier to implement in FPGA

CDF I.P. trigger with just 4 Si layers



AM-based tracking does not need an external track as seed

I.P. resolution = ~60μm

Beam Spot Correction

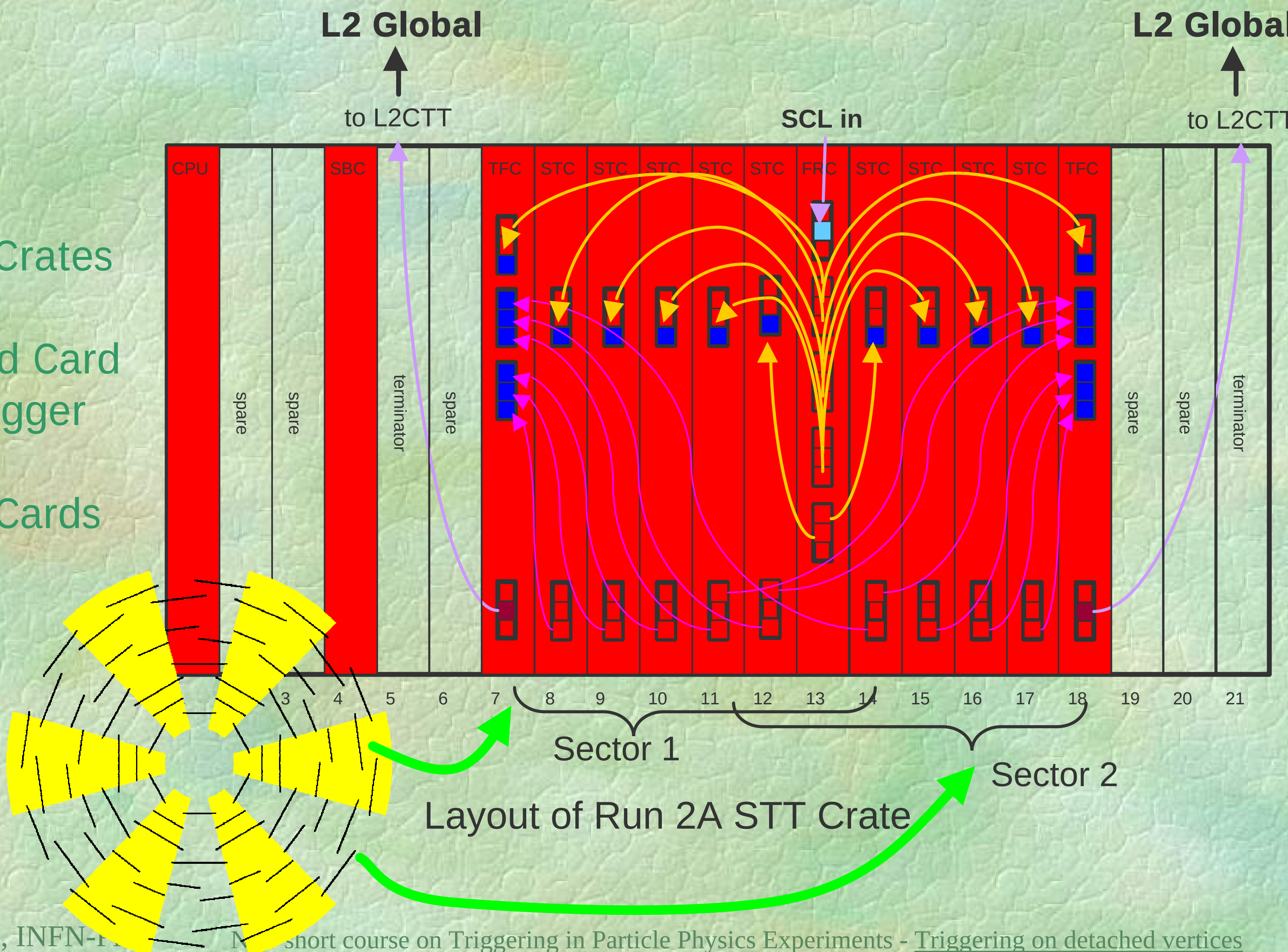
- Track parameters computed wrt detector origin (0,0)
- Impact parameter relevant to physics measured wrt collision (i.e., beam spot)
- Beam spot position downloaded to STT on a run-by-run basis
- Impact parameter correction performed in DSP

$$b_{corr} = b + sign(k)\, r_B \sin(f_B - f_0)$$

  where (r_B, f_B) is beam position
- Beam spot offset tolerance is 1 mm, within Tevatron specs

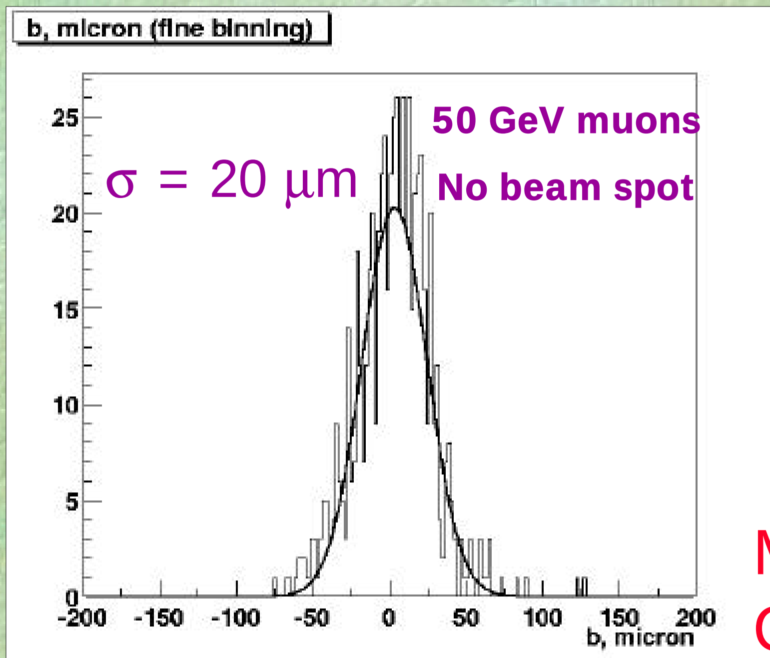
STT Crate

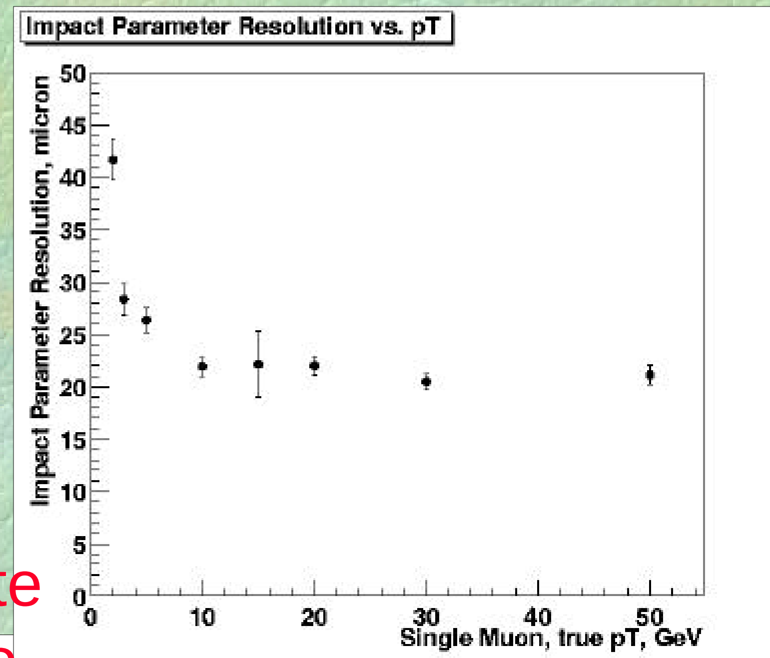
6 Identical Crates with
1 Fiber Road Card
9 Silicon Trigger Cards
2 Track Fit Cards



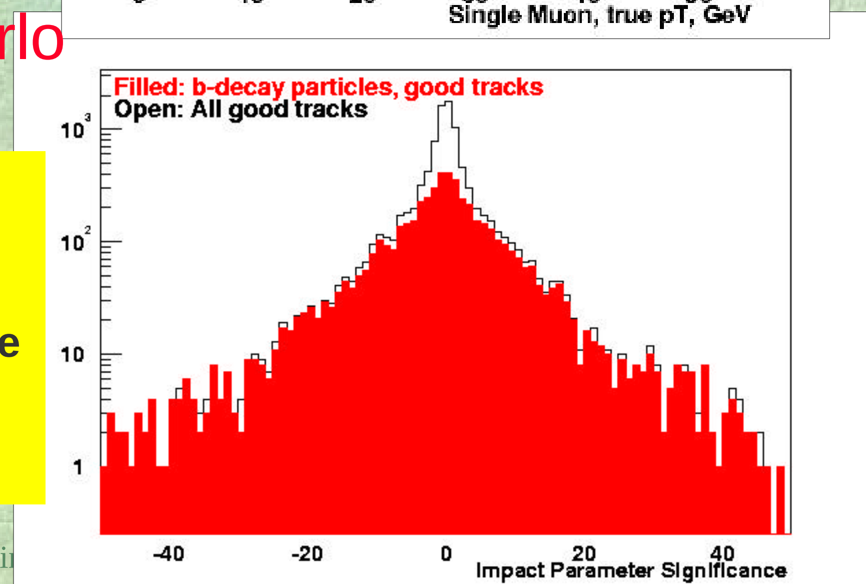
Layout of Run 2A STT Crate

STT Performance





Monte Carlo



- **Plots from STT Trigger Simulator**
- **Exact DSP fitting code used**
- **Has been instrumental in developing the fitting algorithm**
- **Produces test vectors for all cards**

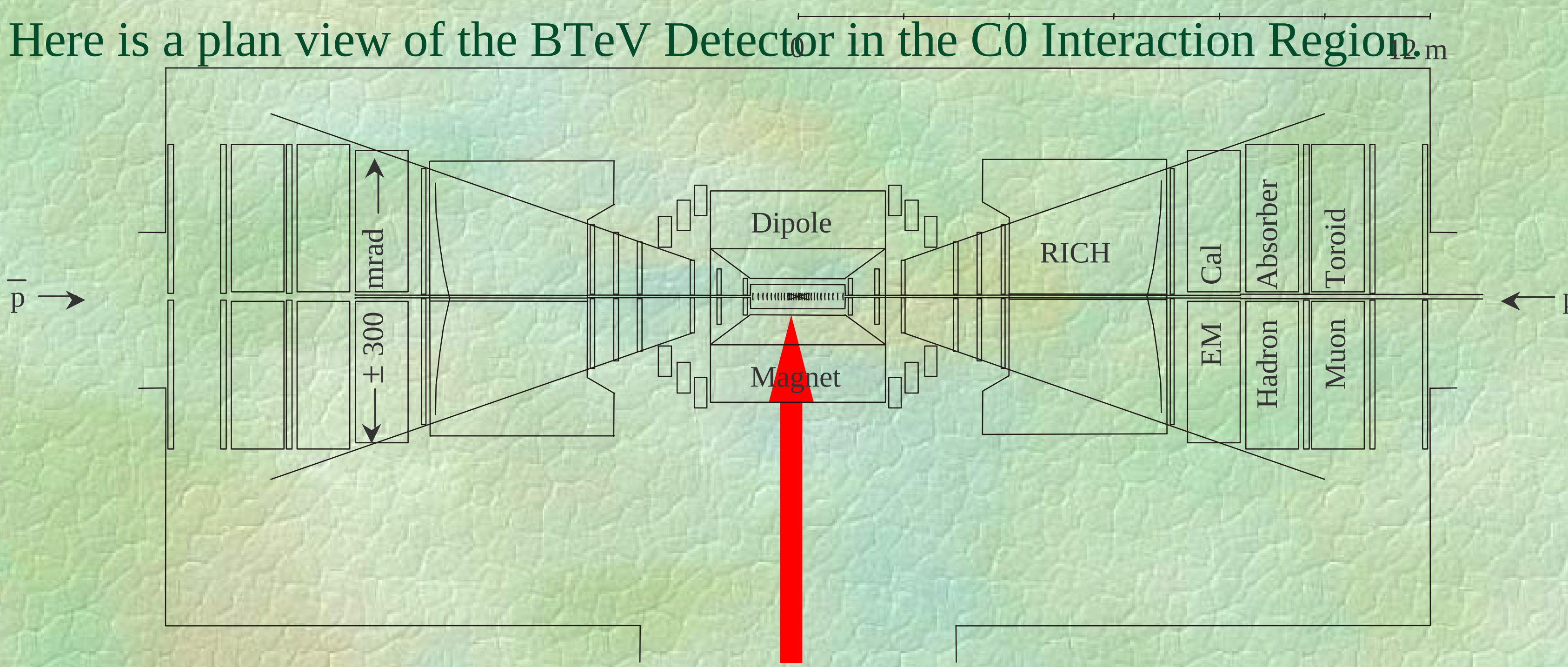
Physics expectations from STT

- Increase inclusive $b\bar{b}$ production yield six-fold with low enough threshold to see $Z \rightarrow b\bar{b}$ signal
  - Control sample for b-jet energy calibration, $b\bar{b}$ mass resolution, b trigger and tagging efficiencies
- Top quark physics
  - Factor of 2 improvement in top mass systematics due to improved jet energy scale calibration
- Heavy $b\bar{b}$ resonances for Higgs searches
  - Double trigger efficiency for $ZH \rightarrow (\nu\nu)(b\bar{b})$ by rejecting QCD gluons and light-quark jets
- b-quark physics
  - Lower p_T threshold on single lepton and dilepton triggers ($B^O \rightarrow \mu\mu$, B_s mixing, etc.)
  - Increase $B_d^o \rightarrow J/\Psi\ K_S$ yield by 50% (CP violation)

New challenge: BTeV L1 trigger

- Tevatron collider experiment, forward-backward geometry
- Strongly oriented to B physics
- Depend on displaced track trigger starting from L1

Here is a plan view of the BTeV Detector in the C0 Interaction Region.



The pixel vertex detector has tracking stations located inside the Tevatron beam vacuum in the dipole field of the BTeV spectrometer magnet:

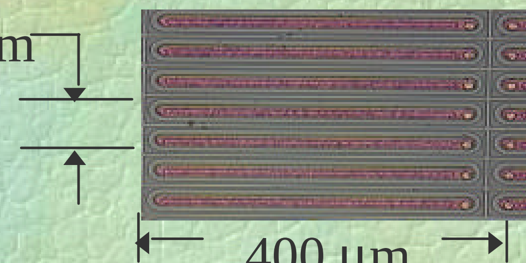
- **31 tracking stations** are evenly distributed over 128 cm
- each tracking station has **2 pixel planes**
- each plane has ~ **500,000 pixels** covering a 10 x 10 cm area
- each pixel is rectangular, with a size of 50 x 400 microns

BTeV Si pixel detector

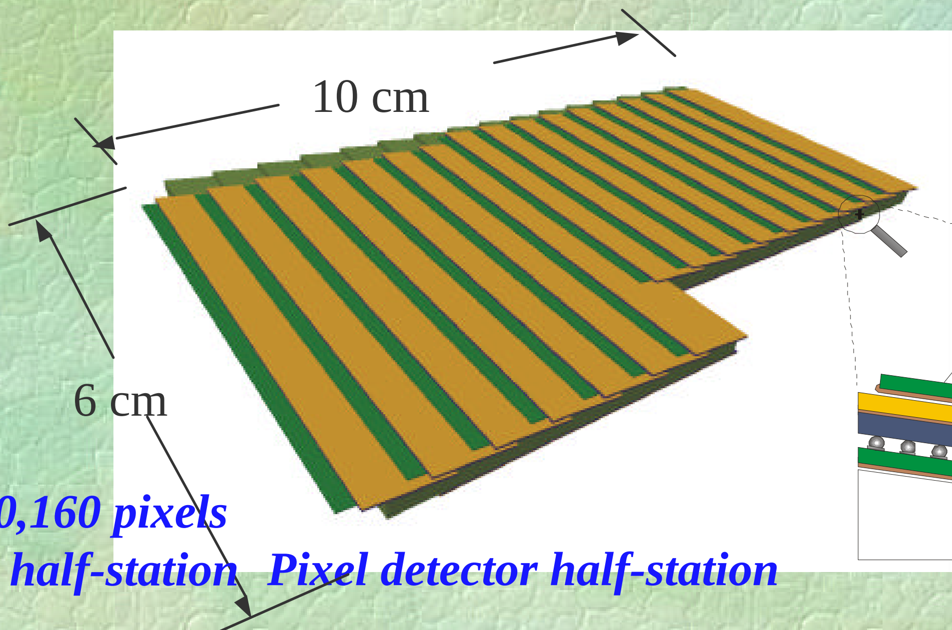
sensor module

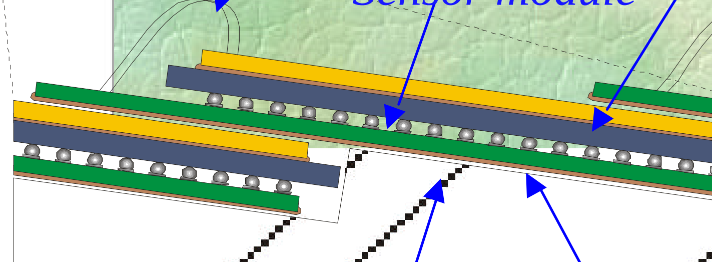
14,080 pixels (128 rows x 110 cols)

total of 23Million pixels in the full pixel detector



Si pixel sensors





380,160 pixels per half-station

Pixel detector half-station

BTeV trigger system

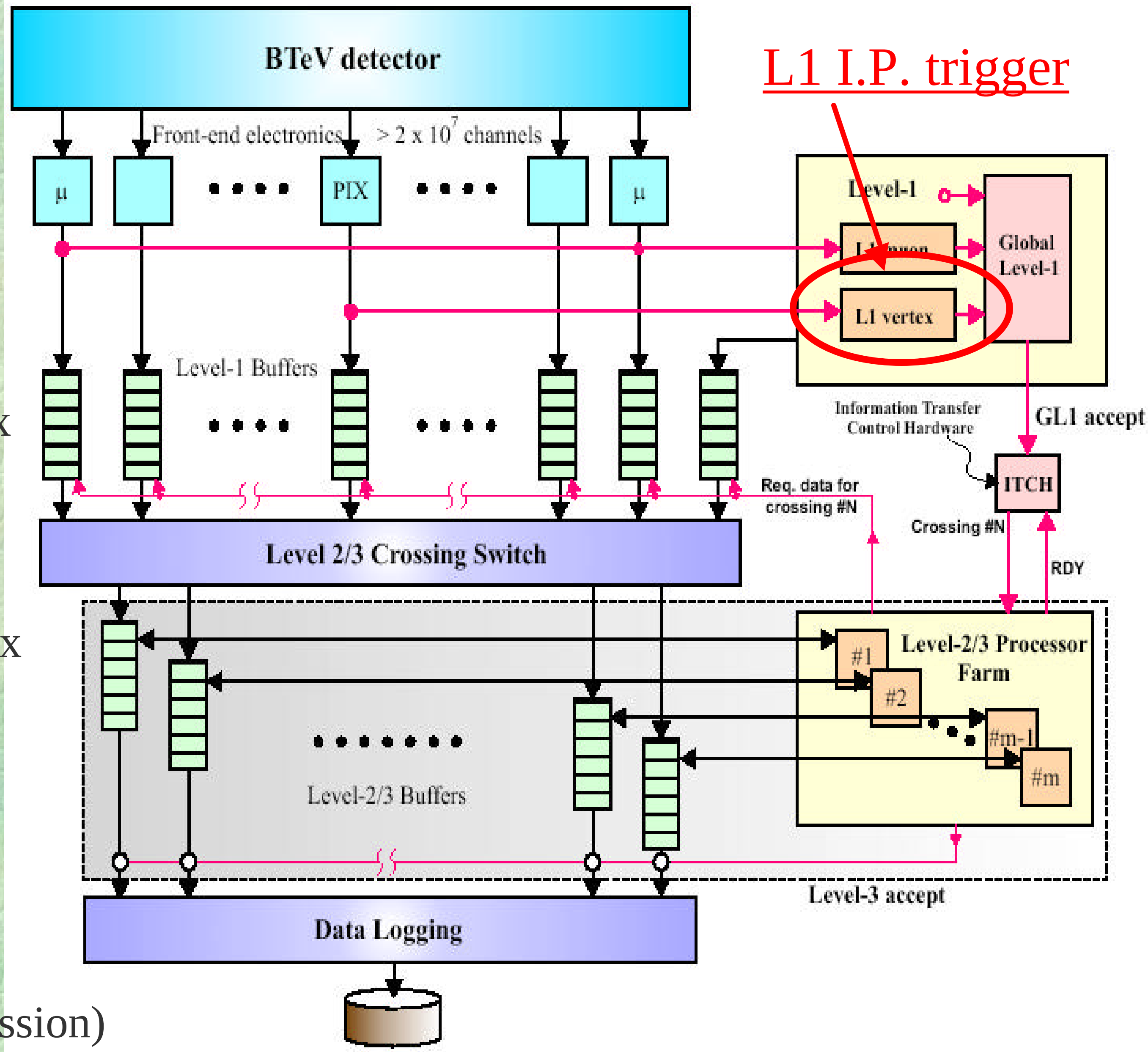
7.6 MHz 1.5 TB/s

L1 rate reduction: ~100x

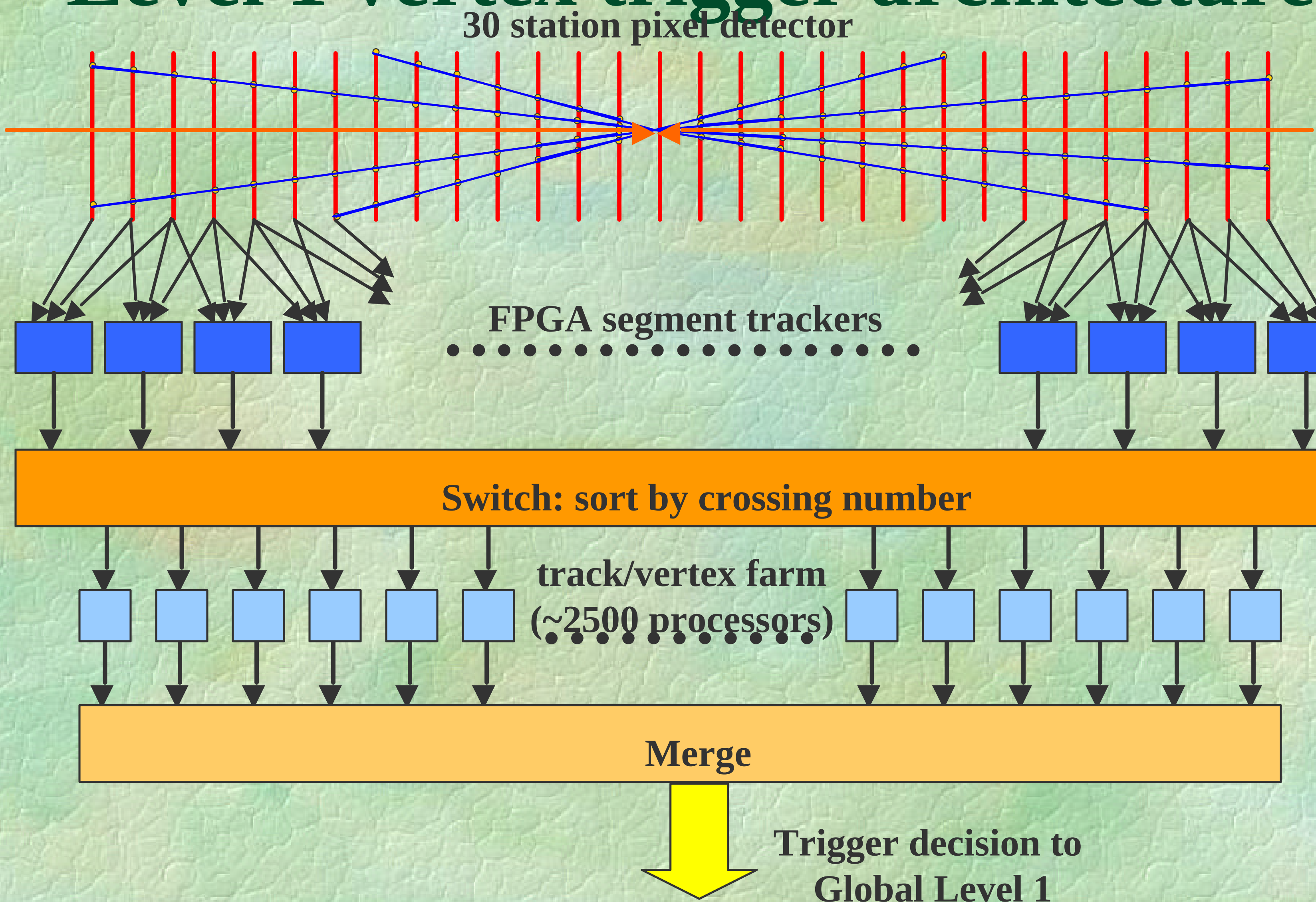
L2/3 rate reduction: ~20x

4 KHz ~800 MB/s

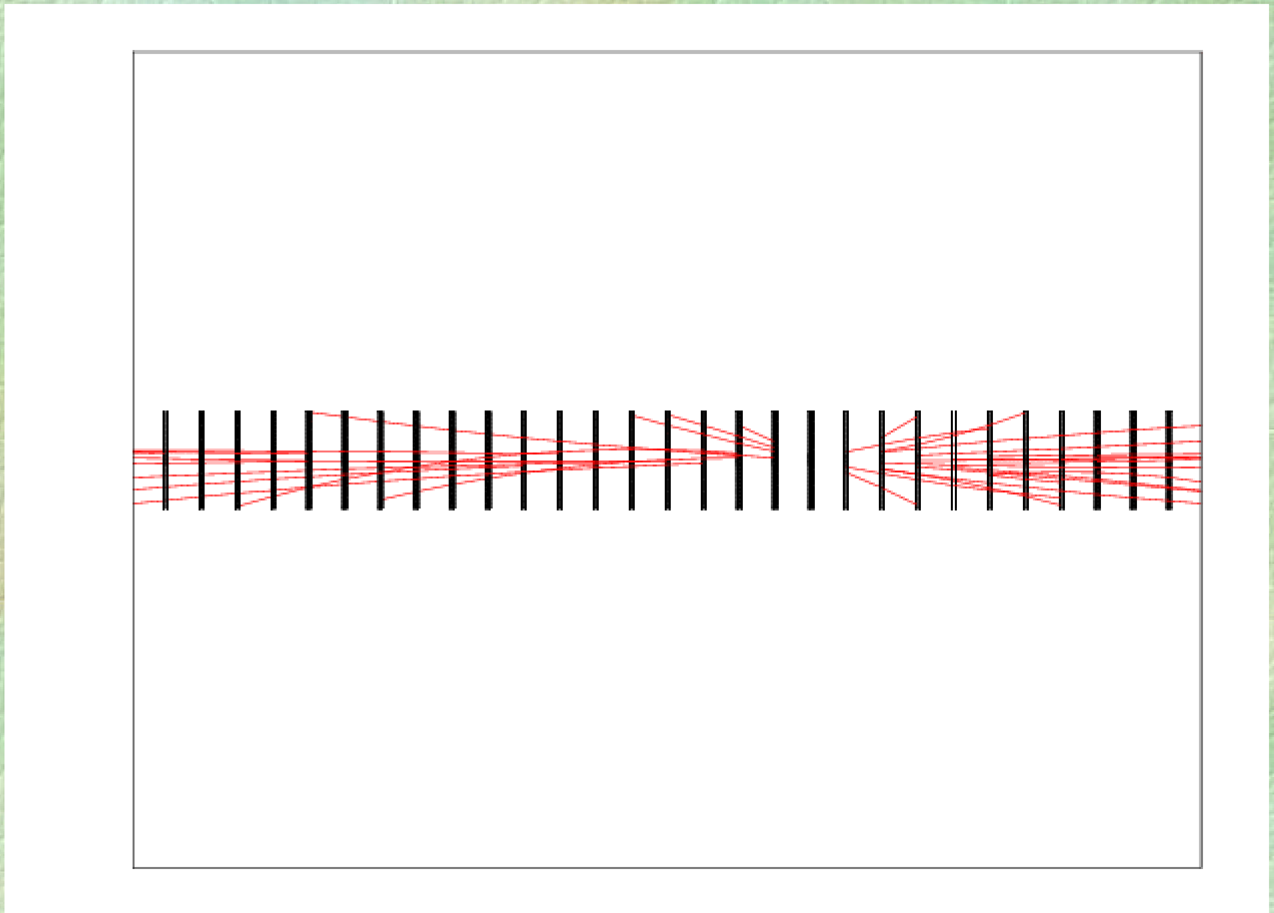
200 MB/s (4x compression)



Level 1 vertex trigger architecture



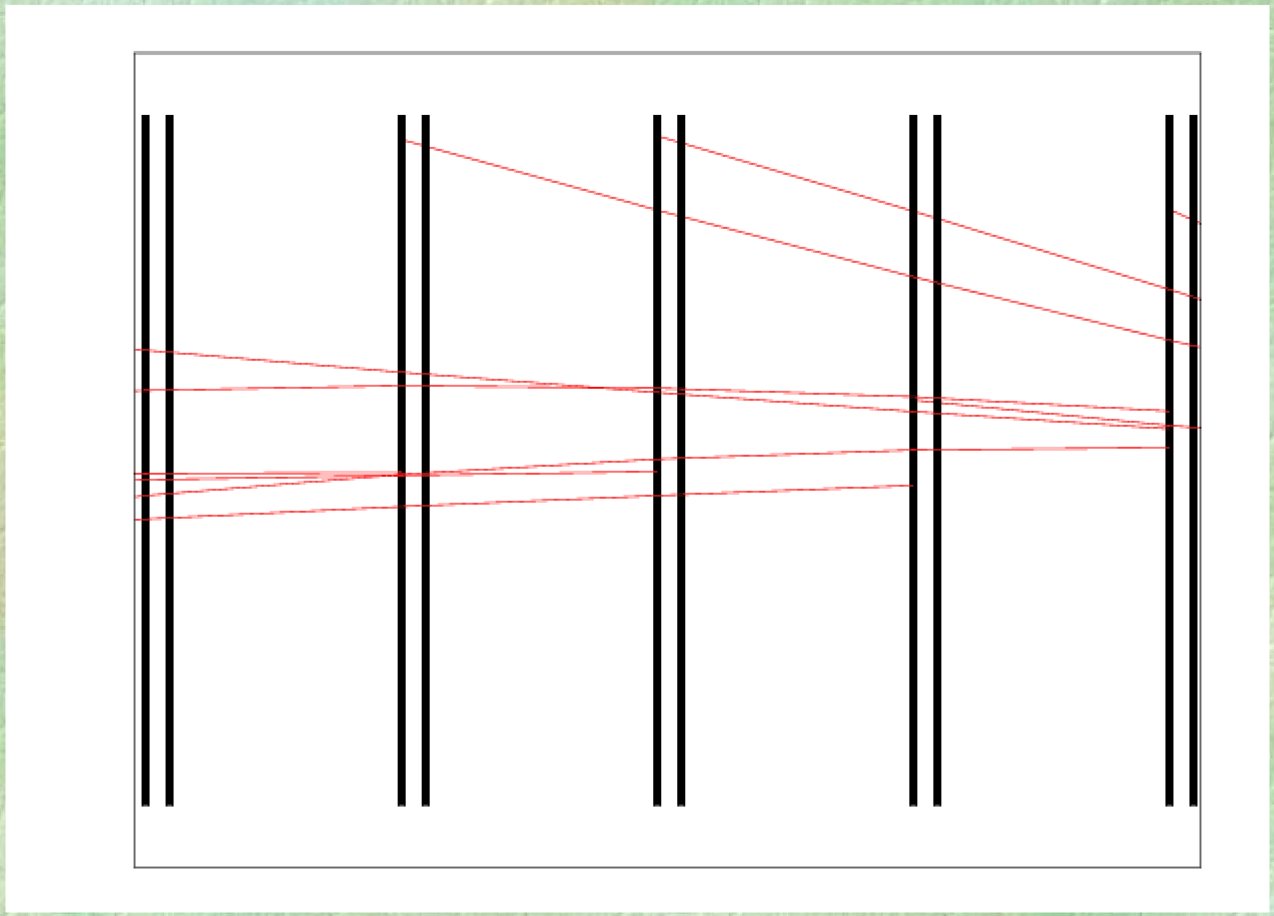
Here is a simulated event in the pixel vertex detector.



A closer look at the vertex detector shows two pixel planes per tracking station.

Per vedere questa immagine
occorre QuickTime™ e un
decompressore Cinepak.

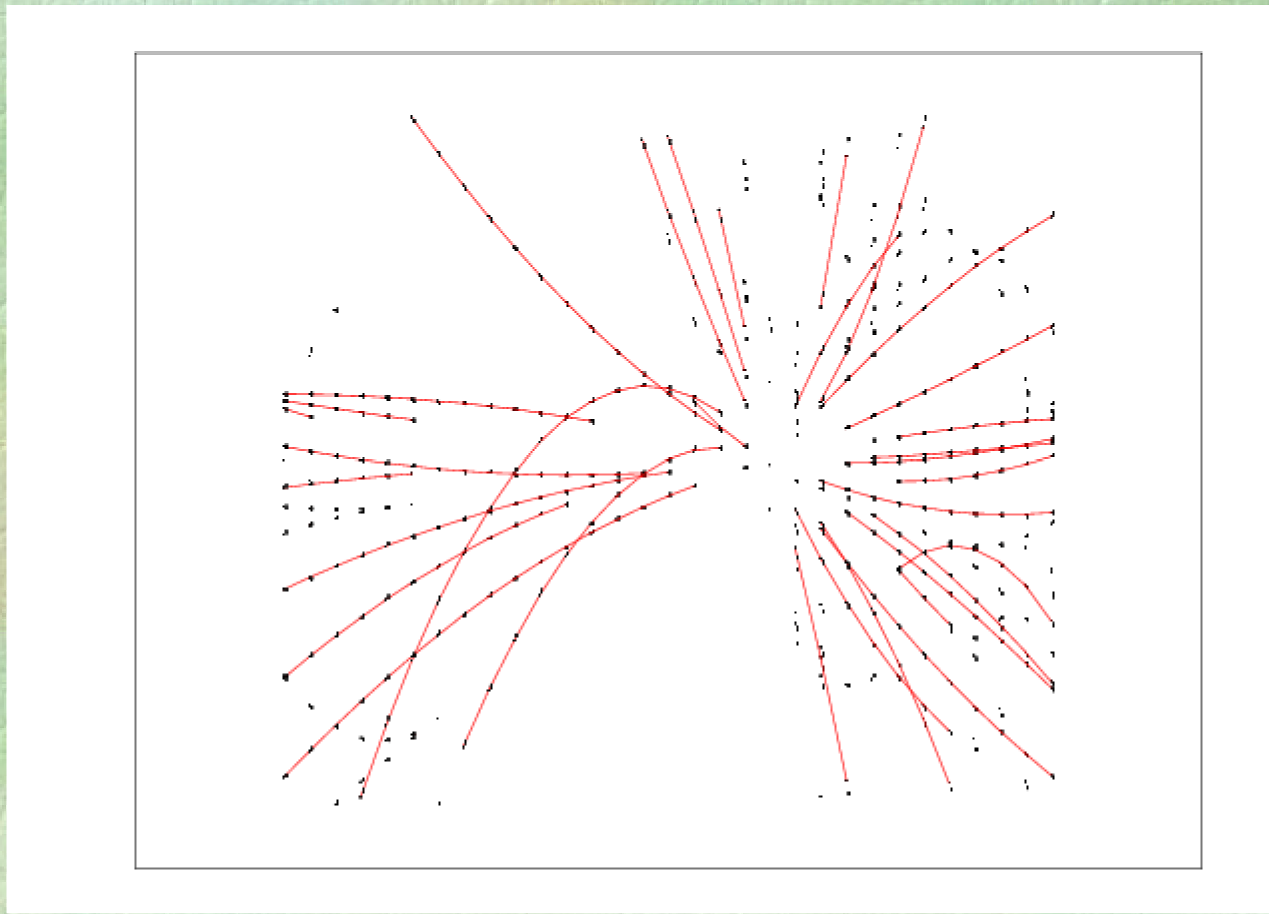
For each station the plane on the right belongs to the collection of planes referred to as the non-bend view and the plane on the left belongs to the bend view.



By compressing everything by a factor of 10 along the beam direction, the curvature of each track in the bend view is more evident.

Per vedere questa immagine
occorre QuickTime™ e un
decompressore Cinepak.

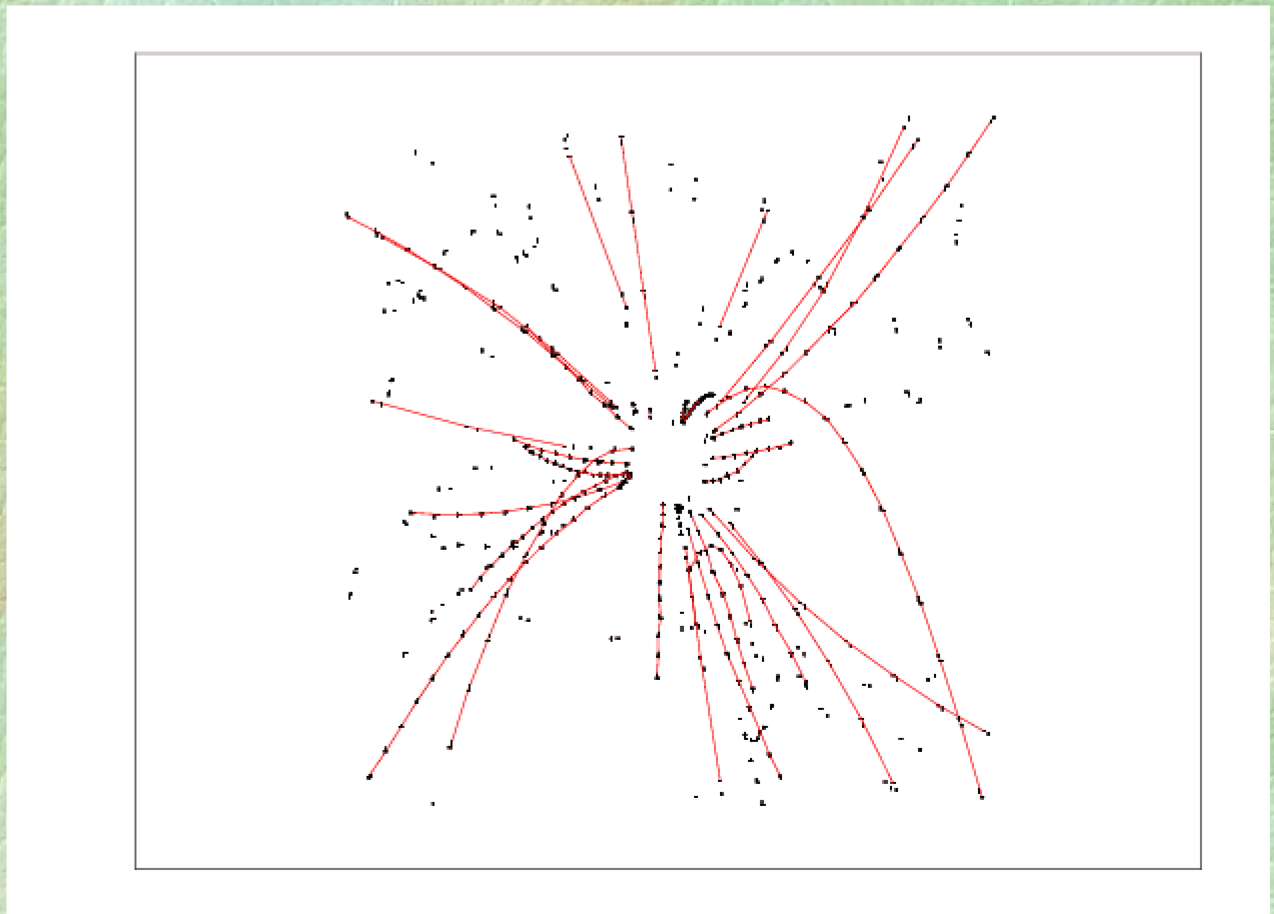
By removing the pixel planes we can see the individual pixel measuremen referred to as “pixel hits.” Hits that are not located on a red track are “noise” hits, or come from tracks not associated with the primary interaction.



Let’s rotate everything by 90 degrees so that we can see the tracks and hitslooking along the beam direction.

Per vedere questa immagine
occorre QuickTime™ e un
decompressore Cinepak.

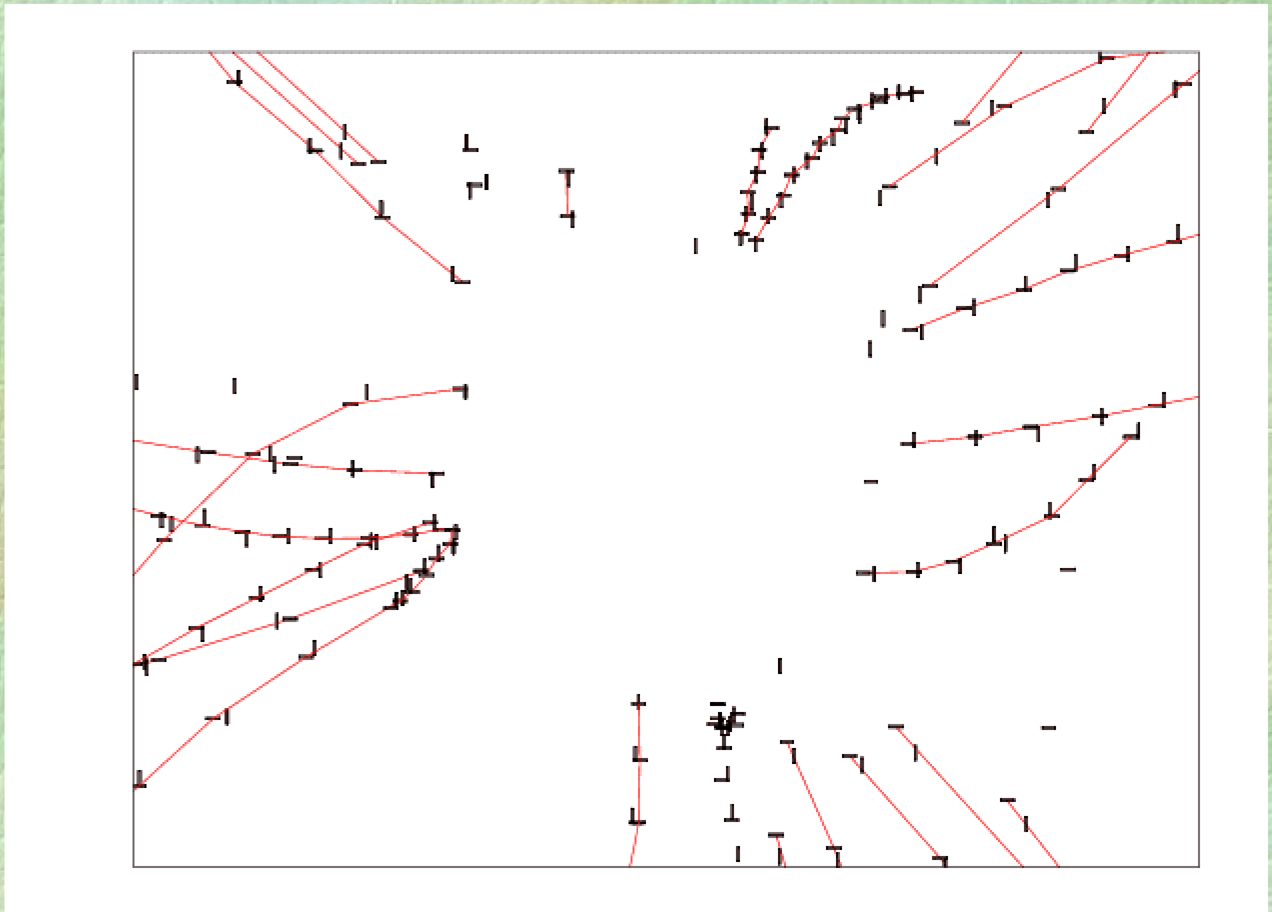
At the center of each pixel plane is a square hole that allows the Tevatron beams to pass through the vertex detector. This explains the absence of hits in the central region, which is referred to as the beam region.



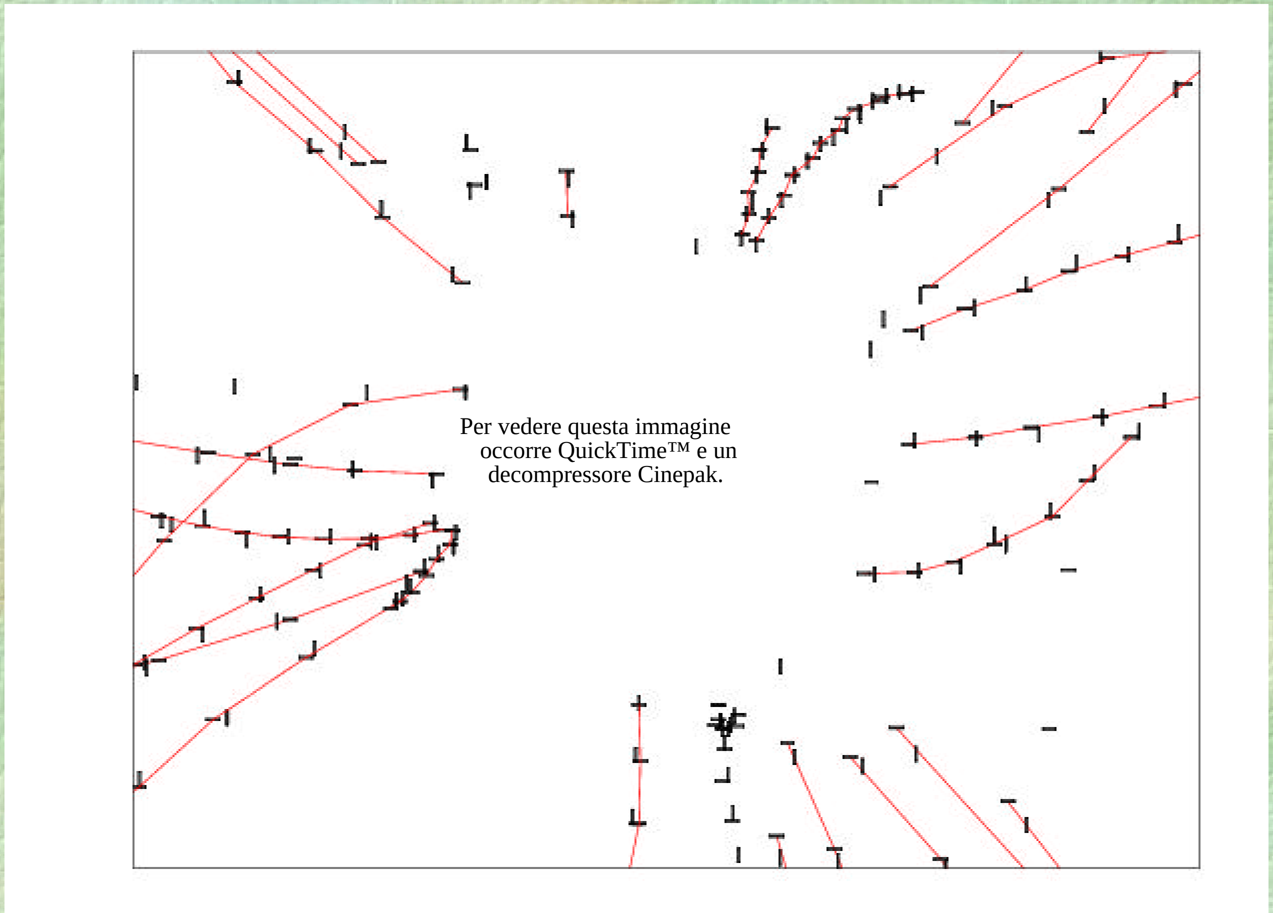
We zoom in a bit more to have a closer look at the pixel hits.

Per vedere questa immagine
occorre QuickTime™ e un
decompressore Cinepak.

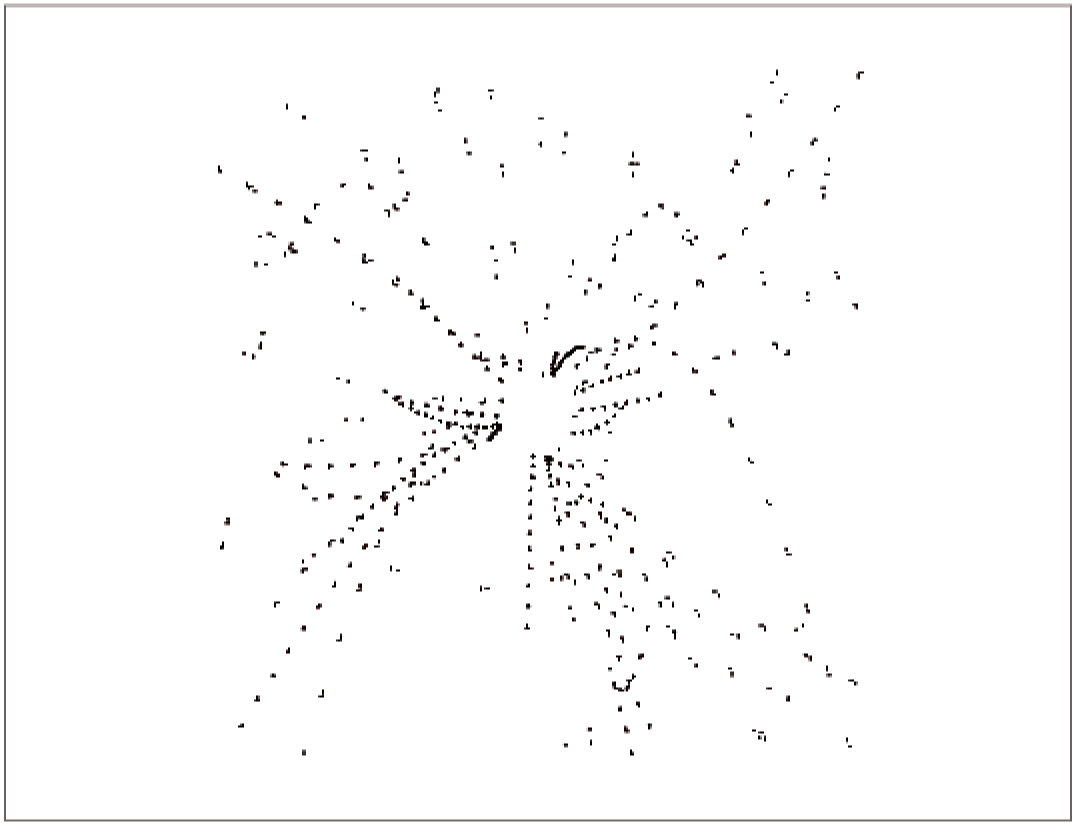
The horizontal rectangles represent hits in the bend view, while vertical hits come from pixel planes belonging to the non-bend view.



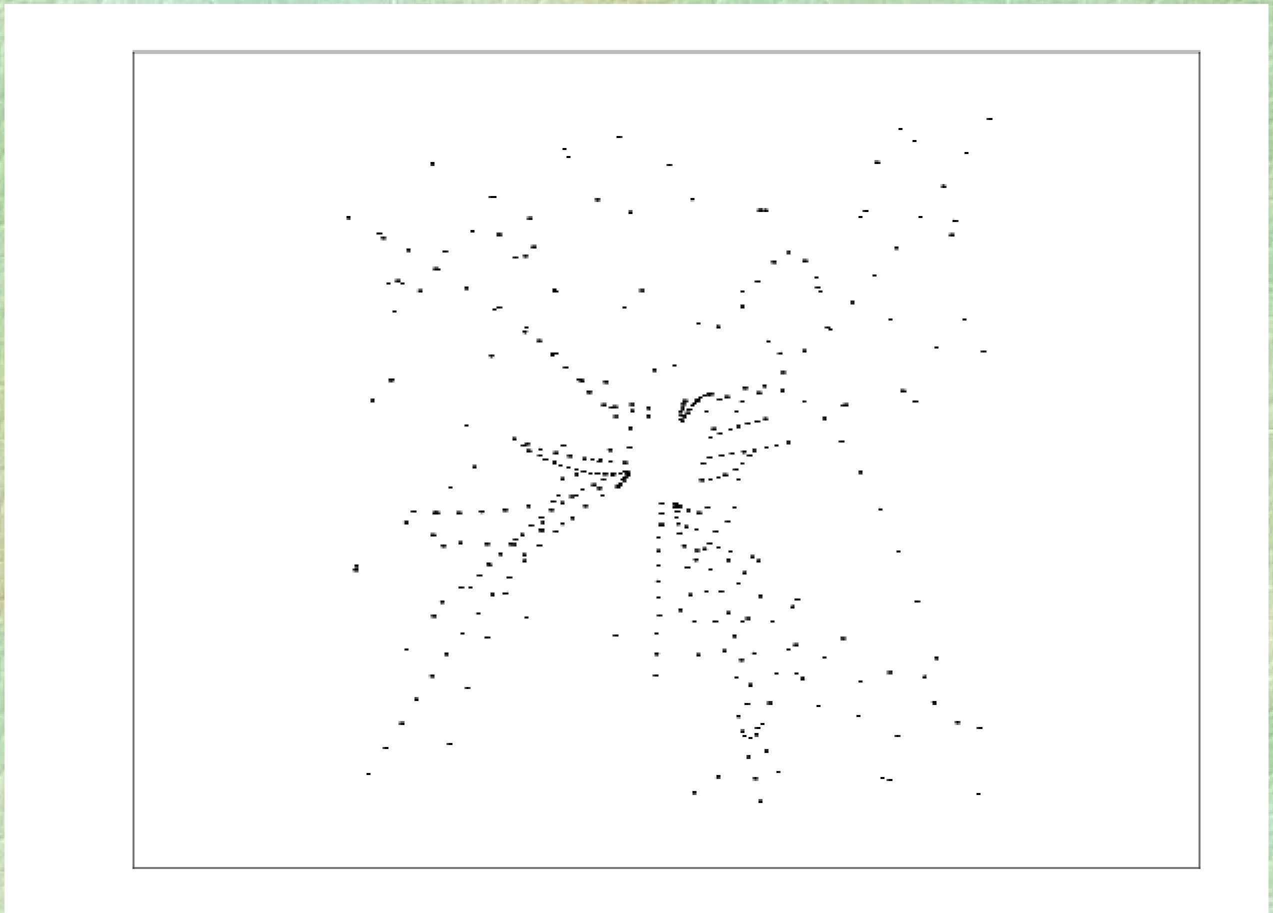
Let’s zoom out and remove the tracks.



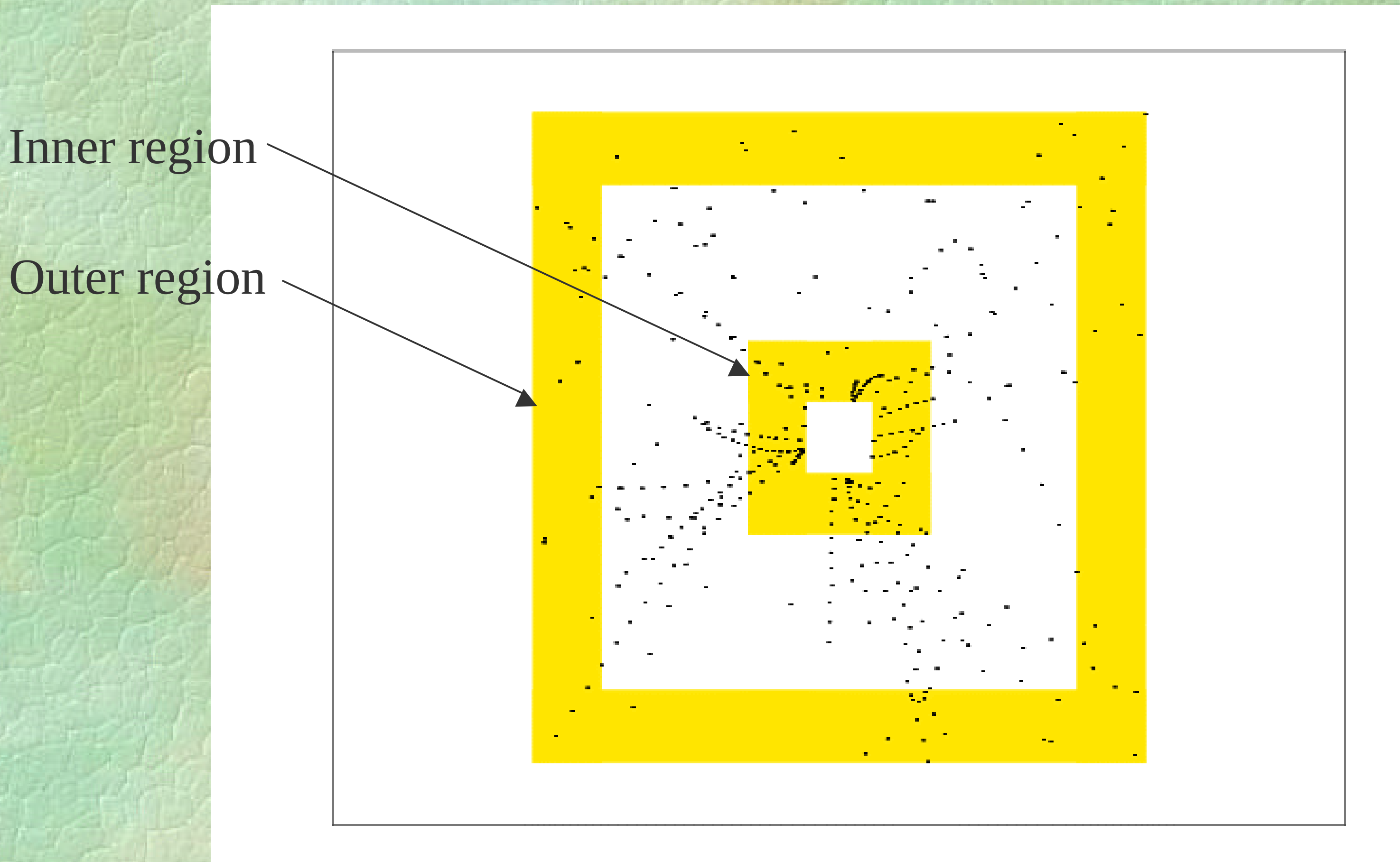
This shows the data that is passed to the vertex trigger, and marks the start of the trigger algorithm.



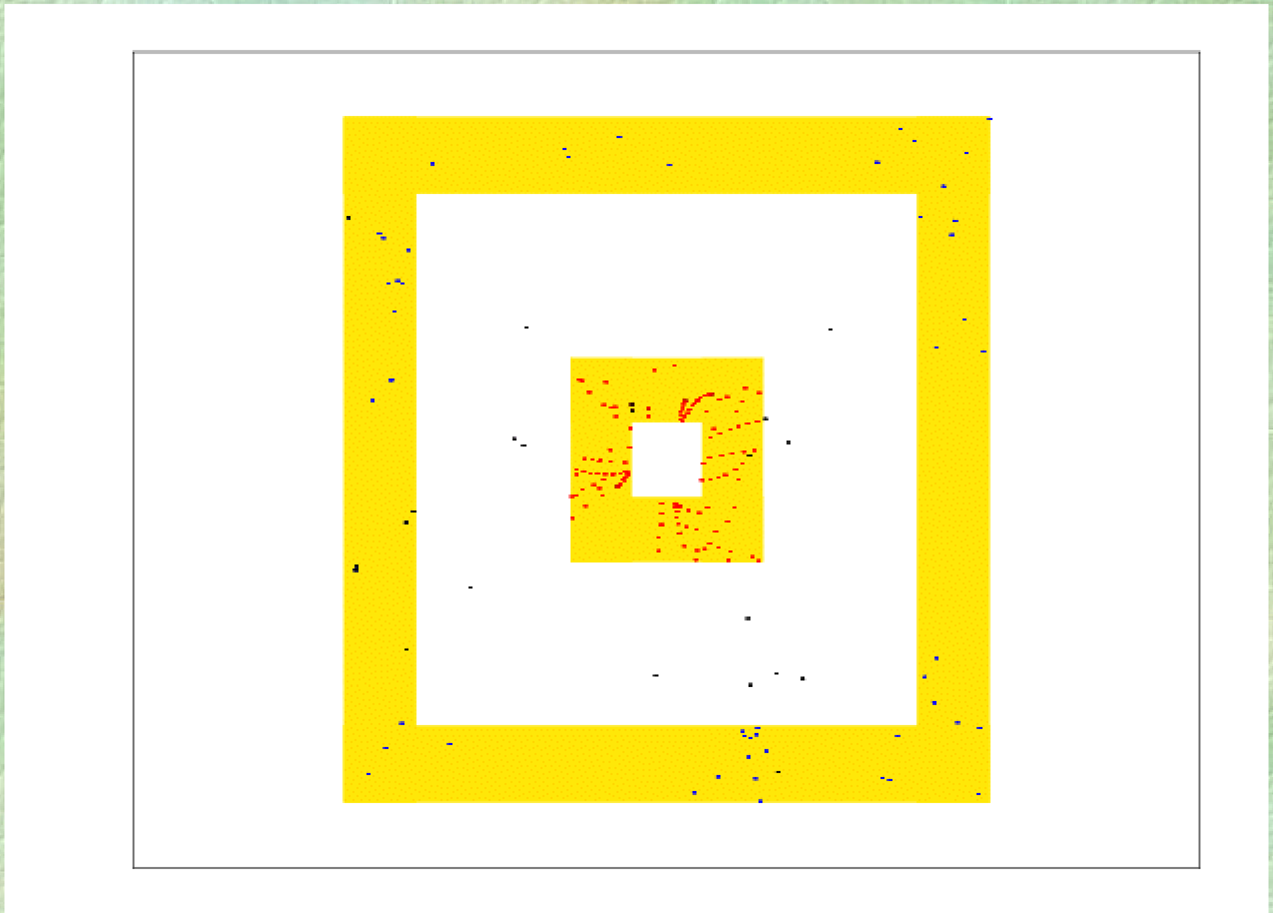
The vertex trigger starts by considering the hits in the bend view. The hits in the non-bend view are ignored for now.



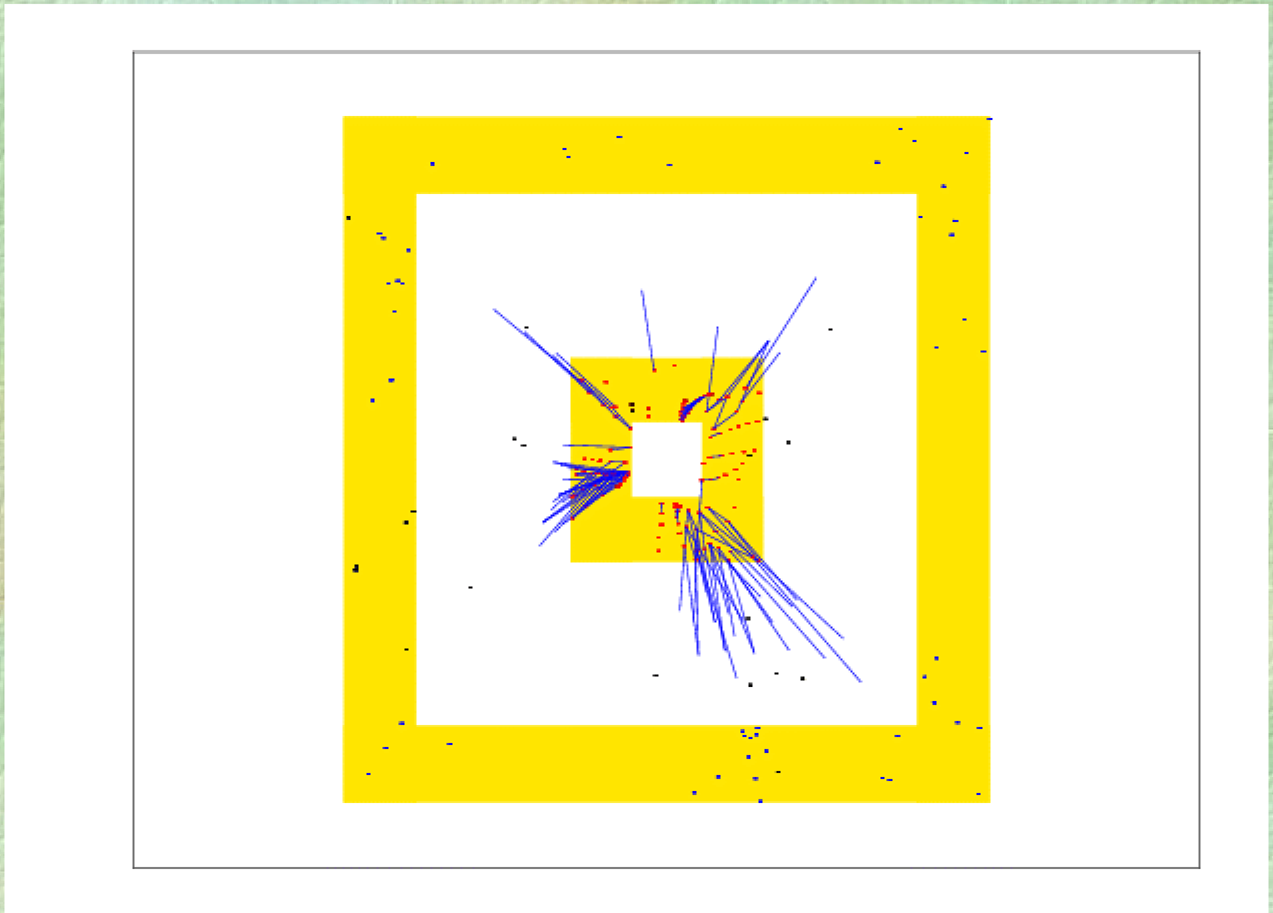
The inner region is used to find the beginning of tracks as they leave the beam region and enter the pixel detector. The outer region is used to find tracks as they exit the pixel detector.



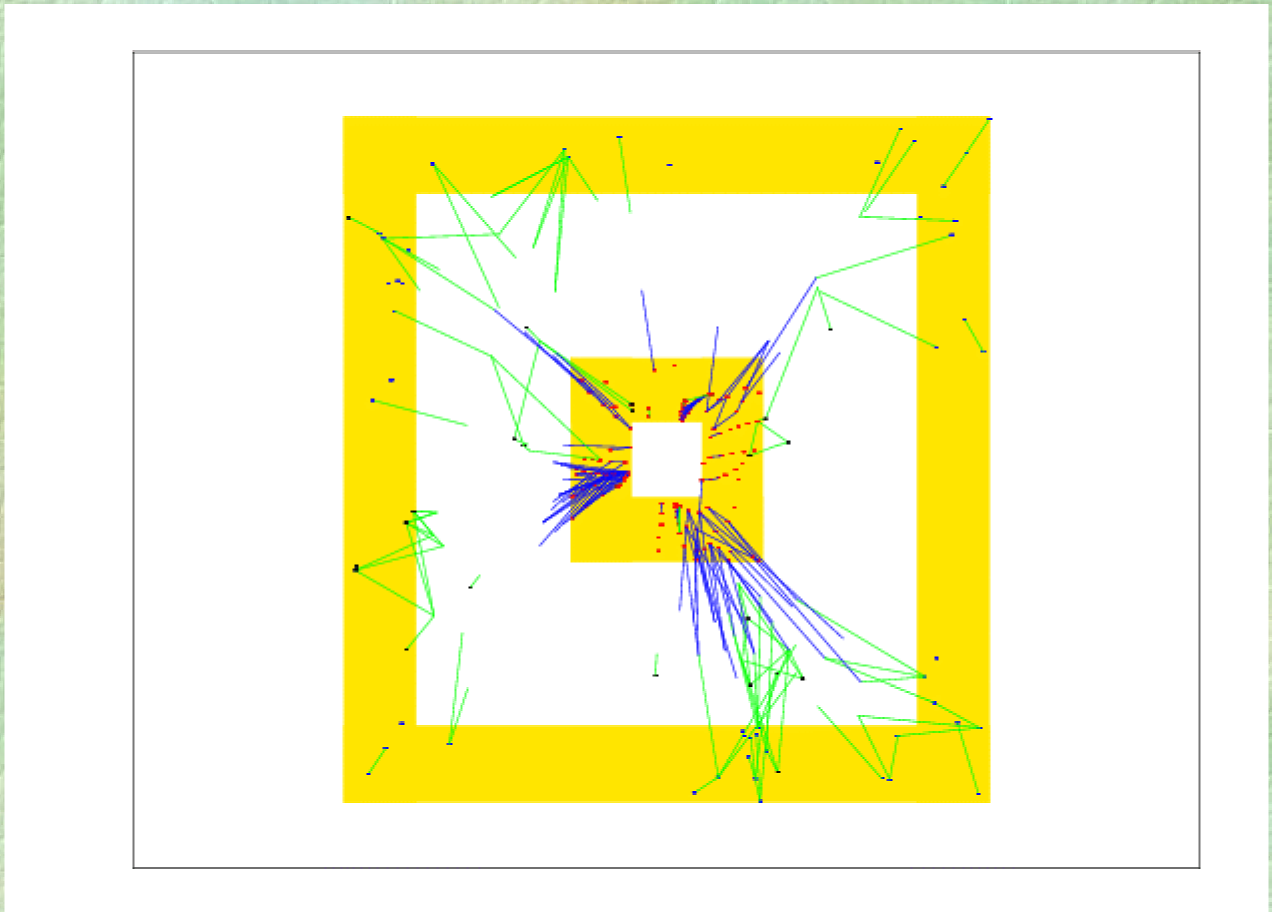
These are the selected hits: red hits in the inner region, and blue hits in the outer region. The **black** hits come from the first and last tracking stations, and are used to find tracks that exit the vertex detector at either end.



Inner hits in one tracking station are matched with pixel hits in an adjacent station. We require that the line connecting a pair of hits projects to the beam region. This step is performed in parallel for hits in all 31 tracking stations.



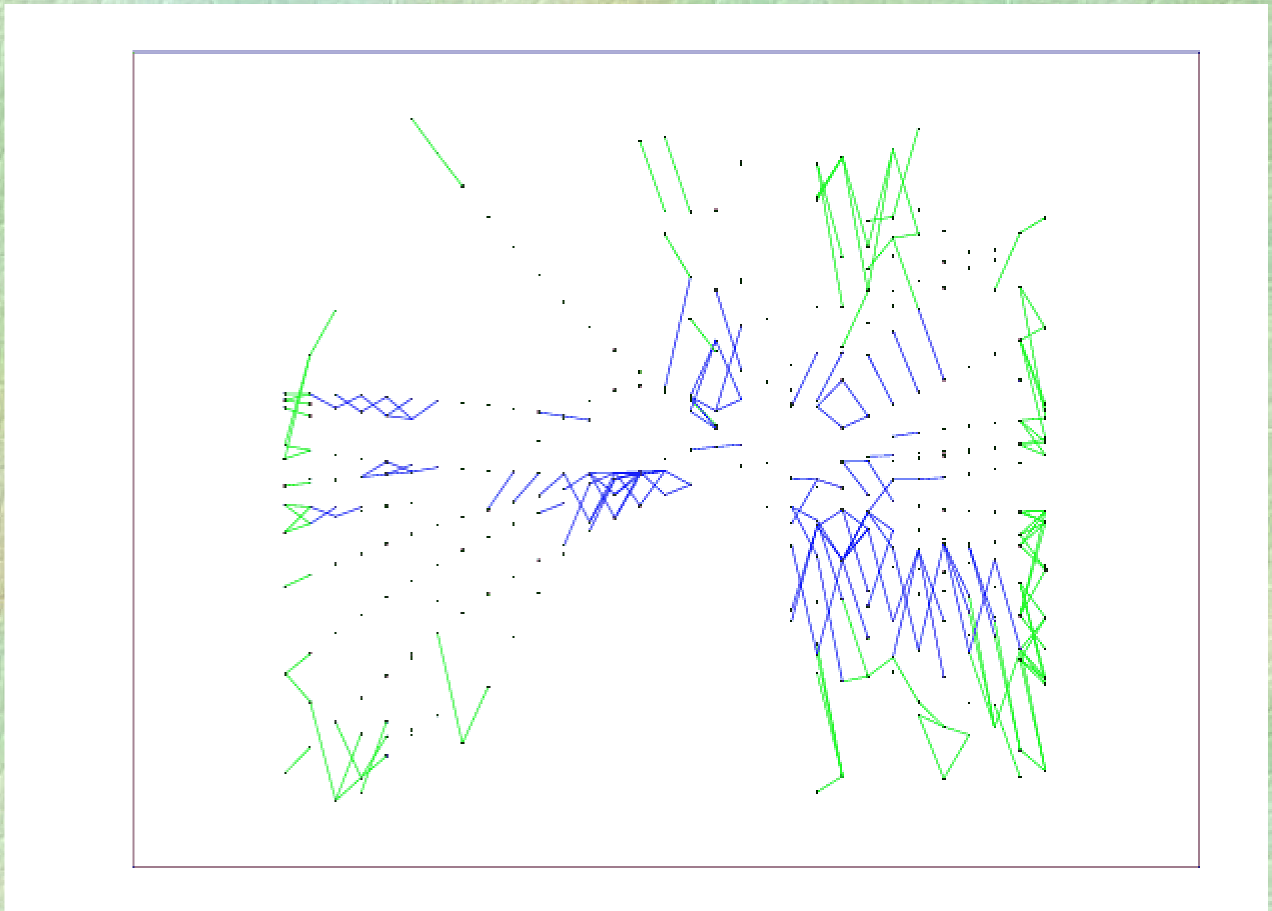
Similarly, the outer hits in each tracking station are matched with pixel hits in adjacent stations. We require that the line connecting a pair of hits projects outside the pixel detector.



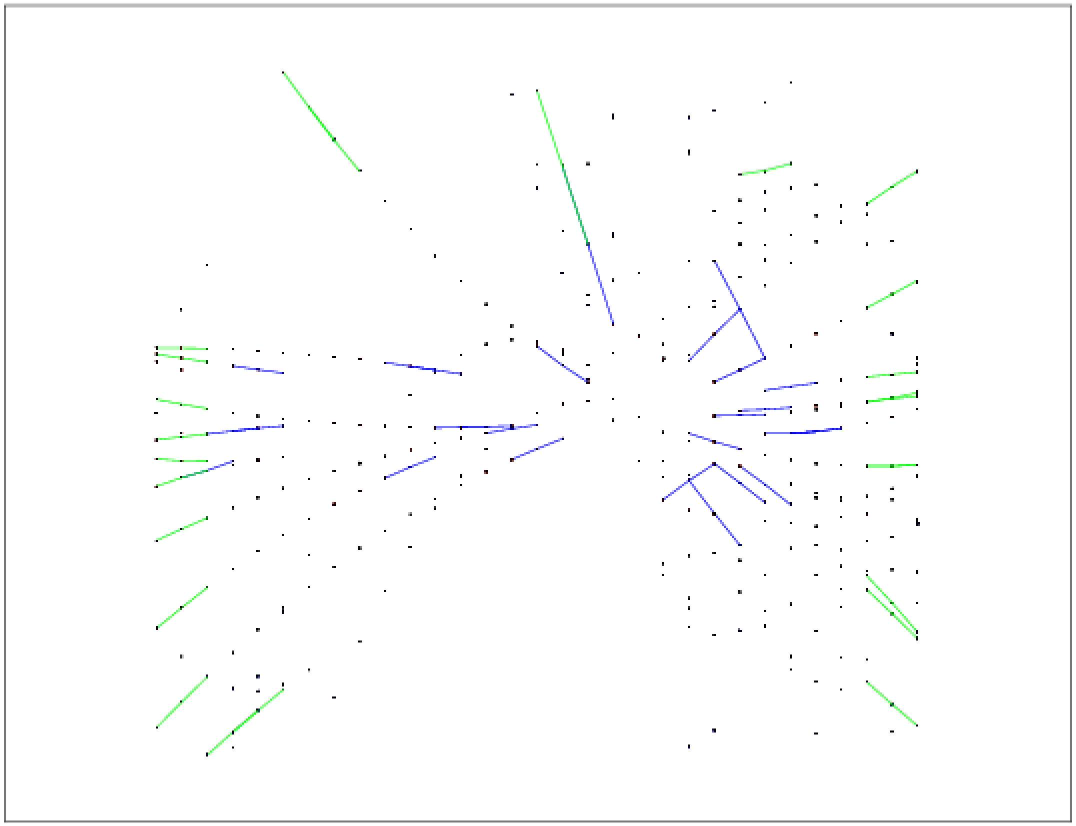
Now we rotate everything back by 90 degrees, and have a look at the track segments that we have found.

Per vedere questa immagine
occorre QuickTime™ e un
decompressore Cinepak.

There are quite a few fake tracks. However, the total number of tracks is less than the number of hits that we started with. So the first step of the trigger is able to reduce the amount of data that must be processed by subsequent steps.



This step does an excellent job, and we are left with the tracks that we need for subsequent track/vertex reconstruction and event selection. A few fake tracks remain, but these are almost all eliminated later on.

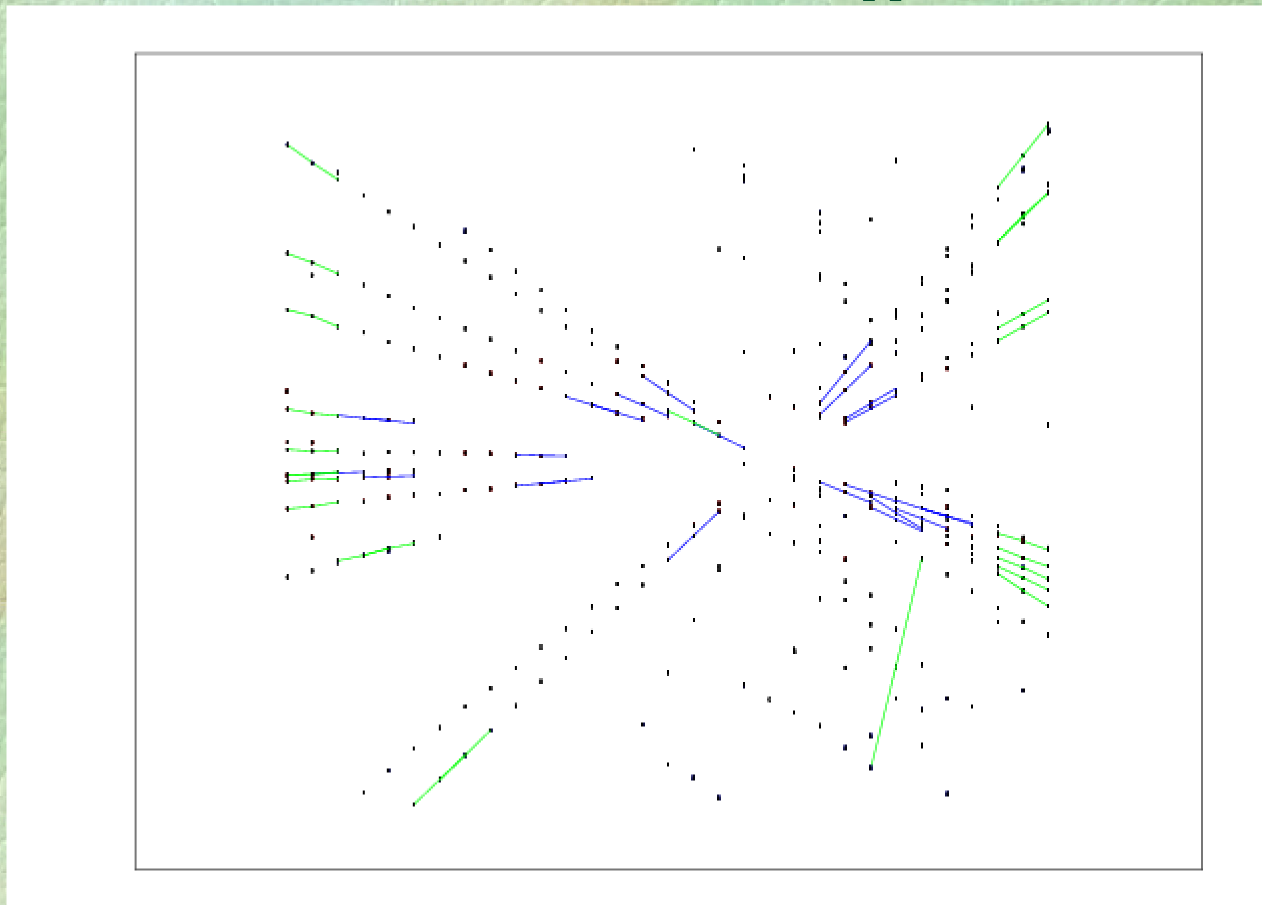


Now we rotate everything by 90 degrees around the beam direction, and have a look at the track segments in the non-bend view.

Per vedere questa immagine
occorre QuickTime™ e un
decompressore Cinepak.

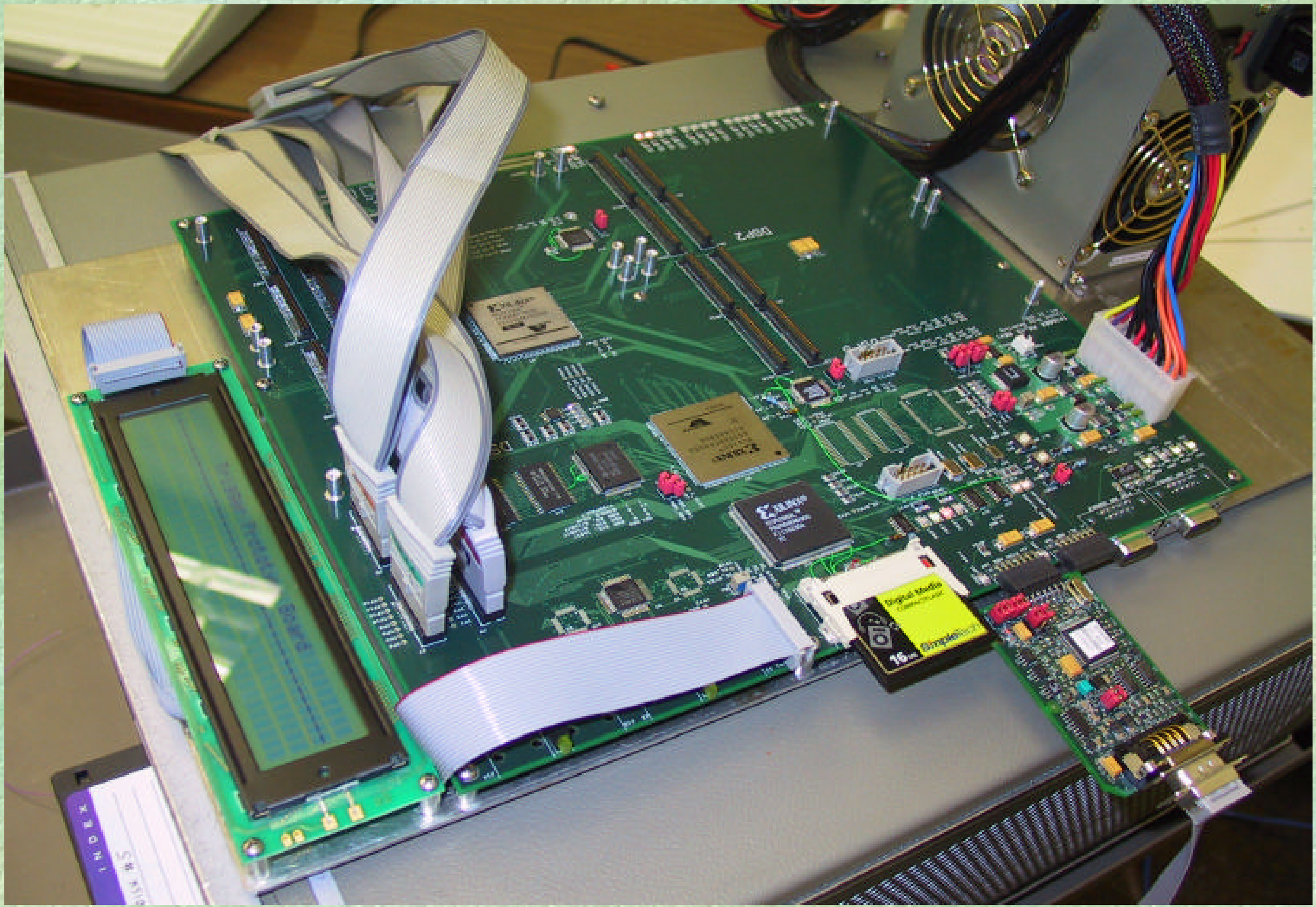
At this point we have introduced the hits from the non-bend view into the trigger algorithm. This step eliminates some of the fake tracks, but more importantly it improves our ability to reconstruct the primary interaction point for each event.

You may have noticed two of the faketracks disappear.



(movie courtesy of Erik Gottschalk)

Level 1 trigger 4-DSP prototype board



BTeV Trigger on detached tracks

Generate Level-1 accept if >2 "detached" tracks in the same arm of the BTeV detector with:

$$p_T^2 > 0.25 \ (\text{GeV/c})^2$$

$$d > 6\sigma$$

$$d \leq 0.2 \ \text{cm}$$

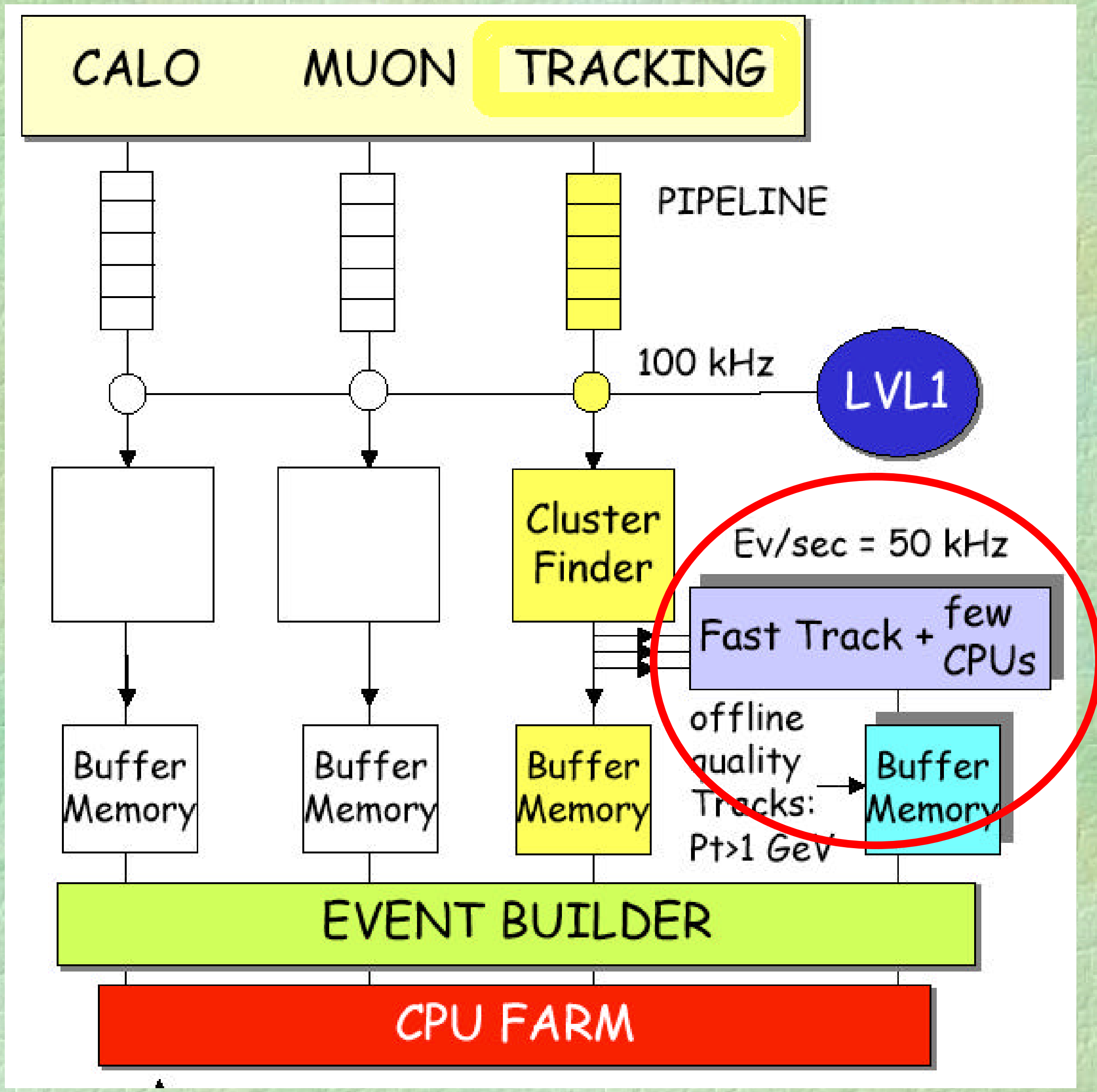
BTeV Level 1 vertex trigger efficiency

Process	Eff. (%)	Monte Carlo
Minimum bias	**1**	**BTeVGeant**
$B_s \rightarrow D^+_s K^-$	**74**	**BTeVGeant**
$B^0 \rightarrow D^{*+} r^-$	**64**	**BTeVGeant**
$B^0 \rightarrow r^0 p^0$	**56**	**BTeVGeant**
$B^0 \rightarrow J/y K_s$	**50**	**BTeVGeant**
$B_s \rightarrow J/y K^{*0}$	**68**	**MCFast**
$B^- \rightarrow D^0 K^-$	**70**	**MCFast**
$B^- \rightarrow K_s p^-$	**27**	**MCFast**
$B^0 \rightarrow$ **2-body modes** (p^+p^-, K^+p^-, K^+K^-)	**63**	**MCFast**

FUTURE: Towards the LHC

- New complex detectors being built
- L1+L3 DAQ systems, connected by a switch - no hardware L2
- Harder to clarify physics targets
- Tracking mainly viewed as L3 (CPU) task
- Hardware detached track finders are being studied as pre-processors before the switch, after L1 accept

LHC-type trigger/DAQ: L1-L3



- Track/vertex processor as a "cluster finder"

- Preprocessed data, smaller size, ready for L3 to use

R&D on Fast Tracking*

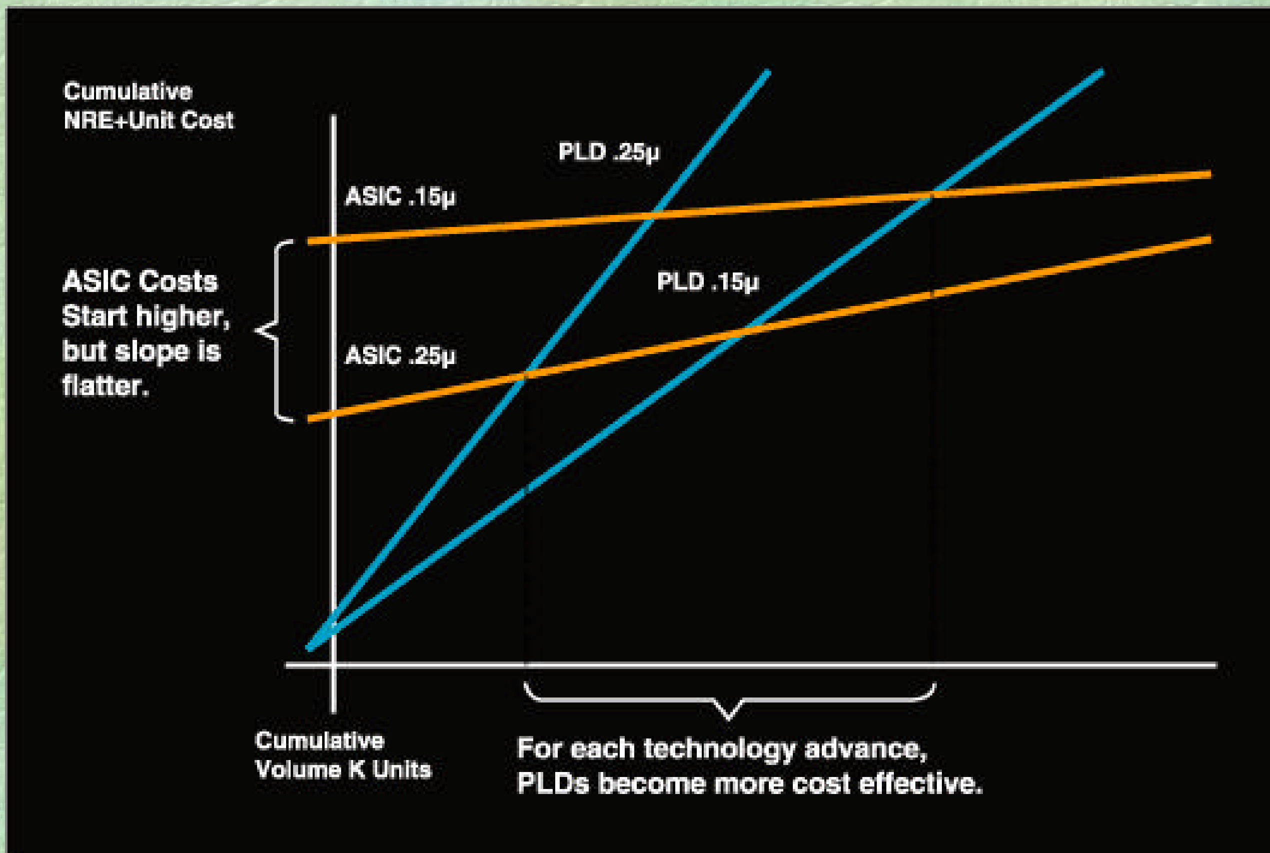
- "CDF-like" system, based on Associative Memory
- Large Si trackers
- No L1 tracks, must use several Si layers
- Larger data volume
- Need larger AMs, ~10 layers, **~10^7 patterns**

* IEEE Trans. on Nucl. Sc., Vol 48, No 3, 575, (2001).

Progress in AM implementations

- ('90) CDF Amchip, full custom 0.7 µm:
  - 6 layers, 12-bit, **16 kpatt/board**
- ('01) XC2S200E 0.18µm (80$/kpatt)
  - 6 layers, **38 kpatt/board**
- ('01) XC2V1000 0.15µm (170$/kpatt)
  - 8 layers, **153 kpatt/board**
- ('98) Stand. Cell 0.35µm (~100k$ + 25$/kpatt)
  - 6 layers, **800 kpatt/board**
- ('05) Virtex? (.1µm) (ITRS98)
  - 12 layers, 18 bits, **330 kpatt/board**
- ('05) Stand.Cell ?(.1µm) (ITRS98)
  - 12 layers, 18 bits, **5600 kpatt/board**
- System: 0.4Mpatt $\rightarrow$ 4 Mpatt, B/W: 0.4Gb/s $\rightarrow$ 4Gb/s

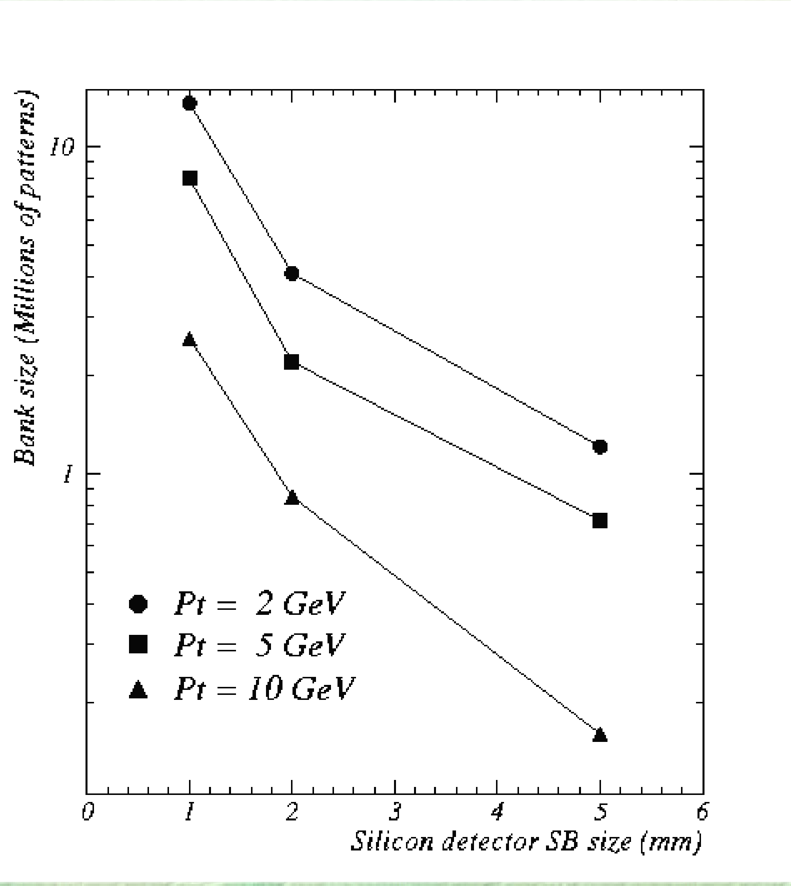
ASIC vs FPGA (from Xilinx)

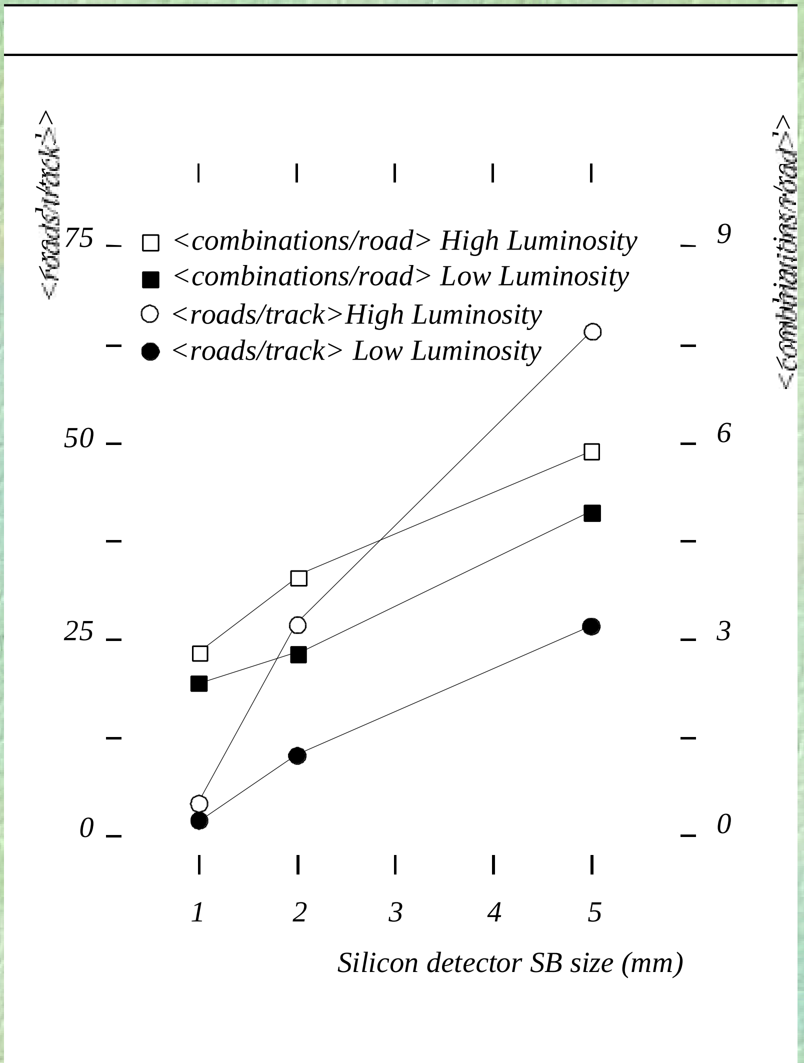


FPGA is best for development/small systems

ASIC may be still better for large systems at future experiment

AM size & fit workload vs bin size





Next-generation AM system

Quick summary

- CDF and D0: ~10μs latency=proc.time (L2)
  - **CDF**: parallel pattern matching (AM 400kcells) + linearized fit (FPGA)
  - **D0** Seed road+association (FPGA)+linearized fit(DSP)
- BTeV: 350μs latency/(N=2500) ⇒132ns (L1)
  - Extensive buffer memories , long L1 pipeline
  - Tracking by growth: hit pairs→triplets →tracks → vertices (FPGA + DSP)
- LHC R&D: Large size AM (FPGA → ASIC)

Concluding remarks

- Triggering on displaced vertices is complex, but it is now a well-established technique
- It is starting to produce hot physics results
- It it likely to play a role in most future experiments