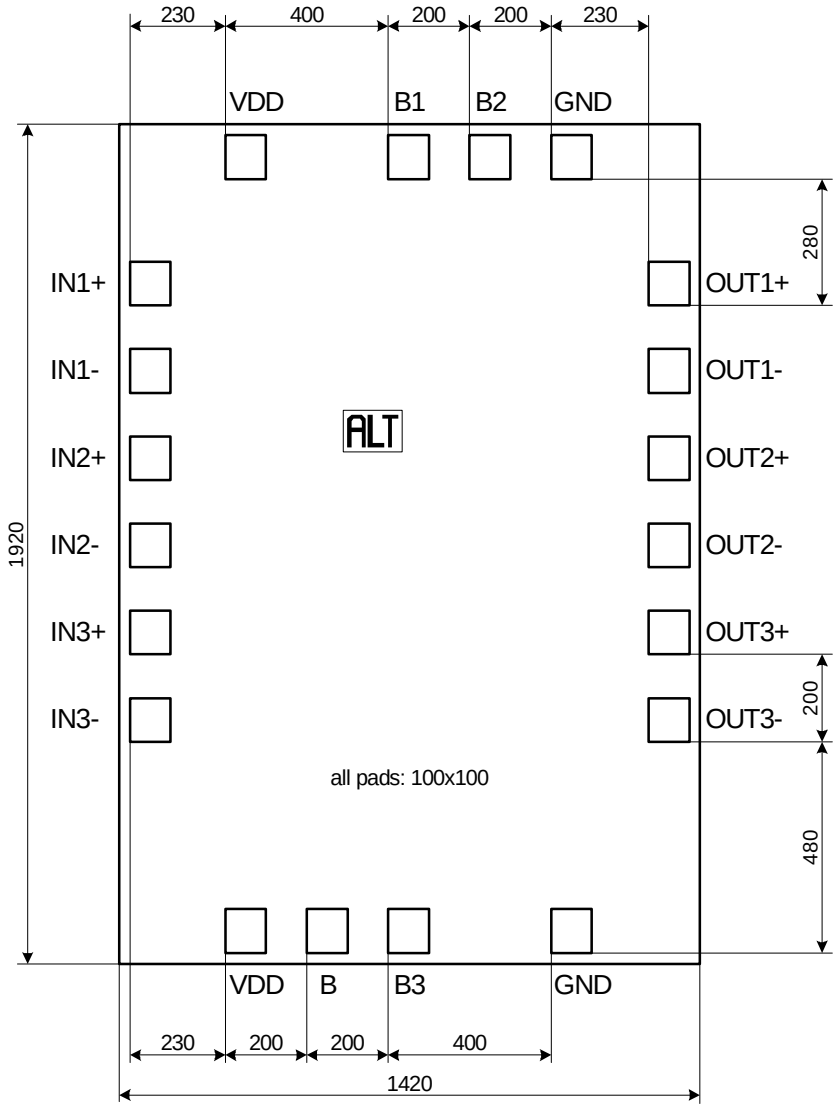
Analog Level Translator (ALT)

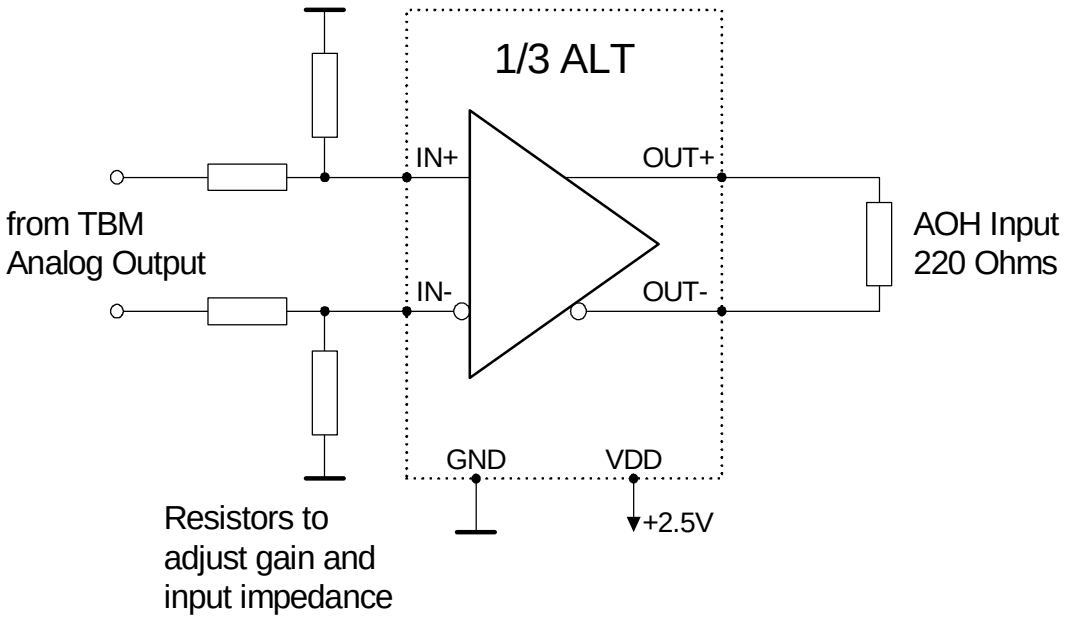
Chip Layout



Pin Description

Signal	*Description*
GND	Power Ground
VDD	Power +2.5V to Ground
IN1+/IN1-	Differential Input of Amplifier 1 (High Impedance)
IN2+/IN2-	Differential Input of Amplifier 2 (High Impedance)
IN3+/IN3-	Differential Input of Amplifier 3 (High Impedance)
OUT1+/OUT1-	Differential Voltage Output of Amplifier 1
OUT2+/OUT2-	Differential Voltage Output of Amplifier 2
OUT3+/OUT3-	Differential Voltage Output of Amplifier 3
B	Bias for Amplifier 1 to 3 (do not connect)
B1	Bias for the Output Stage of Amplifier 1 (do not connect)
B2	Bias for the Output Stage of Amplifier 2 (do not connect)
B3	Bias for the Output Stage of Amplifier 3 (do not connect)

Electrical Specifications *(VDD = 2.5V, Output Load = 220Ω)*

Parameter	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage VDD	2.3	2.5	2.7	V
Total Supply Current		50		mA
Input Voltage Range (In+ - In-)	-100		+100	mV
Input Common-Mode Voltage	-0.4		0.8	V
Input Offset Voltage				mV
Voltage Gain		6.5		
Output common mode Voltage		1.20		V
Output Resistance		450		Ohm

Typical Application Circuit