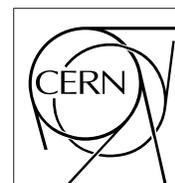


The Compact Muon Solenoid Experiment

CMS Note

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1 April 2006

Naming Convention for Forward Pixel Detector

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Abstract

Initial thoughts of a naming convention for the Forward Pixel detector are described. Large fraction of this draft is from discussions with experts and Simon's talks.

Preliminary version

1 Motivation

Try to lay out consistent naming schemes used in different aspects of the Forward Pixel detector operation, control, data monitoring, etc.

2 Global coordinate

The global coordinate of the CMS detector is defined to be a right-handed coordinate, where the origin is in the Interaction Point (IP), the z-axis is along the positive side of the magnetic field, and the x-axis is pointing to the center of the LHC ring.

A convention way of identifying the components on the CMS detector is like this. For ϕ direction components, we start from number one for smallest ϕ component, and increase index with increasing ϕ angle. For z-axis components, we group them into positive and negative z-axis first; then name the component starting from one and increase the index with increasing distance from origin. For r distributed components, the index starts from one for smallest r and is increased with increasing r value.

3 Overview of the Forward Pixel System

Before laying out different logical views of the Forward Pixel system, we tried to physically identify the major components in this system.

3.1 Electronics Components in US5

In US5, the relevant components are the VME crates and the physically-connected Linux PCs. A rack number followed by a crate location number is then used to identify the VME crates. The naming convention for the rack and crate has been determined already. The boards on a VME crate are then identified by the slot number, and an appendix is added to identify the property of this board. So a naming for a VME board might be something like this:

$$\text{RackID_CrateID_s(slot ID)-(xxxx)}$$

, where (xxxx) is appendix to identify the board property, e.g. LTC and PxIFED. Following the pre-determined name convention for VME crates, Table 1 listed the VME boards related to the Forward Pixel detector.

Table 1: List of electronics components for Forward Pixel detector at US5.

Crate ID	S1G01e	S1G03e	S1E02p	
CAEN controller	S1G01e_S01-CTR	S1G03e_S01-CTR	S1E02p_S01-CTR	
VME boards	S1G01e_S05-PxIFEC	S1G03e_S06-PxIFED	S1E02p_S02-LTC	
	S1G01e_S06-PxIFEC	S1G03e_S07-PxIFED	S1E02p_S08-TTCci	
		S1G03e_S08-PxIFED	S1E02p_S09-TTCex	
		S1G03e_S09-PxIFED		
		S1G03e_S10-PxIFED		
		S1G03e_S11-PxIFED		
		S1G03e_S12-PxIFED		
		S1G03e_S13-PxIFED		
		S1G01e_S06_CcsFEC		
	Linux PC	S1G01e_PC	S1G03e_PC	S1E02p_PC

For each one of the VME boards (PxIFEC, CcsFEC, and PxIFED), there are several optical inputs. These are labeled from top to bottom of the board as Ch1 to Ch3 for PxIFEDs or Ch1 to Ch8 for PxIFECs or CcsFEC. These channels of the FECs or FEDs represent physical connections and are different from the logical view described later. So optical connectors for a PxIFEC (S1G01e_S06-PxIFEC) are named as:

$$\text{S1G01e_S06-PxIFEC_Ch1, S1G01e_S06-PxIFEC_Ch2, ..., S1G01e_S06-PxIFEC_Ch8.}$$

Note that each connector is a 12-channel multi-mode fiber. **One thing is not mentioned here is the location and naming of the 1:32 tree optical coupler.**

3.2 On-detector Components

The naming of the Forward Pixel on-detector components always start with FPix. The components on the positive z-axis side and the negative z-axis side are prefixed with Bp and Bm, respectively. So there are two major groups of components: FPix_Bp and FPix_Bm.

3.2.1 Disk Groups

	BLD	ADP	PRT	LV (Blades)	LV (Port Card)	HV	Cooling		
1/2-Disk	1					B1	1	IN	
	2	1	1	1		B2			
	3					B1			
	4						2	OUT	
	5	2	2	2		B2			
	6					1	B1	IN	
	7						3	2	
	8	3	3	3		B2			
	9						B1		
	10							4	OUT
	11	4	4	4		B2			
	12						B1	IN	
1/2-Disk	13					B2	5	3	
	14	5	5	5		B1			
	15								
	16						6	OUT	
	17	6	6	6		B2			
	18						B1	IN	
	19					2	7	4	
	20	7	7	7		B2			
	21						B1		
	22							8	OUT
	23	8	8	8		B2			
	24						B1		

Figure 1: Components included in a disk group.

For the same side detector components, one way to organize them is to divide them into disk groups, which include the detector components, front-end electronics, low voltages, high voltages, coolings, RTDs used to operate and monitor a disk. These disk groups are still labeled as D1, D2 and D3, where the index increases with the distance from the IP. Note there is an exception here that we separate out the slow I2C control components for a disk. Figure 1 is a initial trying of exhausting the components in a disk group. As shown, it contains 24 blades (BLD), 8 adapter card (ADP), 8 port cards (PRT), and other high/low voltage channels and cooling channels. On one side of the Forward Pixel detector, there are two disks (D1 and D2) in current on-construction configuration.

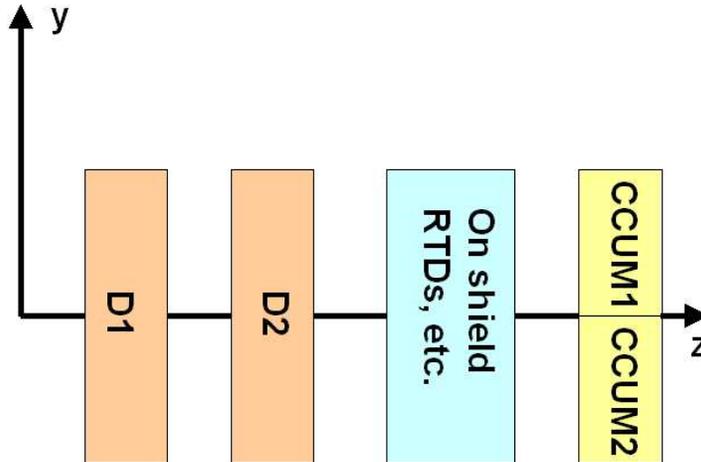


Figure 2: Block of components for the Bp side of the Forward Pixel detector.

Further, there are some other left components are not grouped into disk groups, e.g on-shield RTDs. Another very

important piece at this levels is the CCUM boards. there are a total of four boards for the Forward Pixel System, one for each half-cylinder. Figure 2 shows a block organization of the detector components for the Bp side of the Forward Pixel detector: FPix_Bp_D1, FPix_Bp_D2, CCUM boards (FPix_Bp_CCUM1 and FPix_Bp_CCUM2), and other components like RTDs.

Up to this level, a blade can be named as FPix_Bp_D1_BLD24 and a port card has a name of FPix_Bp_D1_PRT8.

3.2.2 Breakdown of a Blade

A blade within a disk group has a complicated structure. Further breakdown of it follows the way shown in Figure 3. Every blade (BLD) contains two panels (PNL), which are indexed from 1 to 2 with increasing distance

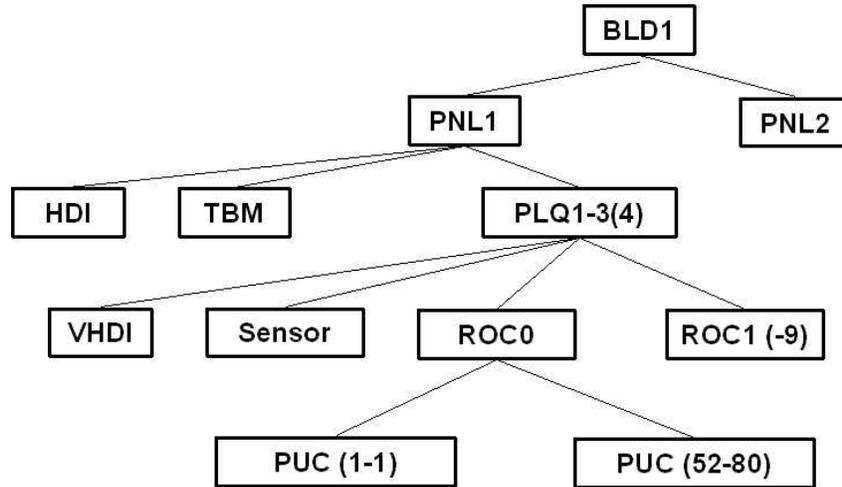


Figure 3: Breakdown of the major components of a blade.

from IP. Several major components are contained in a panel: HDI, TBM, and several plaquettes (PLQs). There are three or four plaquettes on a panel, which are numbered from 1 to 3 (or 4) with increasing radius from beam line. A plaquette also has a complicated structure, which contains VHDI, Sensor, and several Readout chips (ROCs). **ROCs are numbered from 0 to 1 (up to 9) following the token path for each plaquette (it might be more consistent if we number ROC starting from 1?). Further, every pixel unit cell (PUC) on a ROC can be identified by the col number and row number of this cell.**

So a plaquette in the Forward Pixel detector can be identified as

FPix_Bp_D1_BLD24.PNL2_PLQ2.

A plaquette is a detector unit (DetUnit) for the forward pixel detector. In this scheme, the numbering of a DetUnit is identical as used in simulation. Further down to a specified pixel unit cell can be identified as

FPix_Bp_D1_BLD24.PNL2_PLQ2_ROC3_PUC23-56,

where the last two numbers show the column number and row number for this cell.

3.2.3 Breakdown of Port Card

A portcard contains the following pieces and has very complicated tasks in the detector operation.

- one Detector Control Unit (DCU).
- one mDOH, which contains two laser diodes and one Linear Laser Driver (LLD).
- one Tracker PLL (TPLL).
- one Delay 25 (Delay25).
- one Gate Keeper (GateKeeper).

- one AOH board, which contains two LLDs and two ALTs.
- one RTD.

It is essentially the interface between the front-end and the electronics in the US5. In the forseen operations of the detector (e.g. run monitoring), identification of the major components on this board is needed. Figure 4 shows a

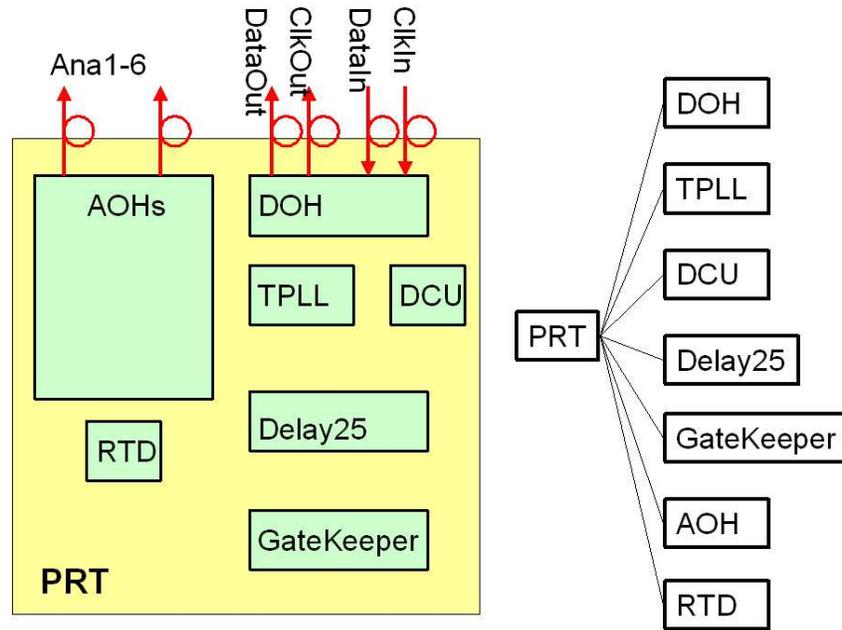


Figure 4: Breakdown of the major components for a port card (PRT).

block diagram of a port card and names used to identify each major block. Following this convention, the AOH on a port card of the Forward Pixel detector can be named as,

Fpix_Bp_D1_PRT7_AOH.

Correspondingly, the AOH optical output channels are numbered from Ana1 to Ana6; the optical inputs and outputs for the DOH are named as DataIn, DataOut, ClkIn, and ClkOut. **Since the port card is still in a prototype design phase, physical locations of the channels are not yet identified.**

3.2.4 CCUM boards

Similarly as port cards, we further break down the major components of the CCUM boards, Figure 5 shows a block diagram of the major components. With this convention, these components can be labeled as:

FPix_Bp_CCUM1_CCU1, etc.

Note that the CCUM board is still in design phase. Physical locations of each major block can't be identified. Also, these boards also introduction more low-voltage supply channels. We also identify the optical inputs and outputs to CCUMs board, as shown in Figure 5.

3.2.5 Summary of the Physical Naming for On-detector Components

With the conventions as described above, the names of on-detector components can be summarized in Figure 6. Here we used mainly the electronics components as examples, however, the naming for other parts can be done in a similar and consistent way. **Further, we should check if the identification of a pixel unit cell (PUC) is the same as used in calibration, etc.**

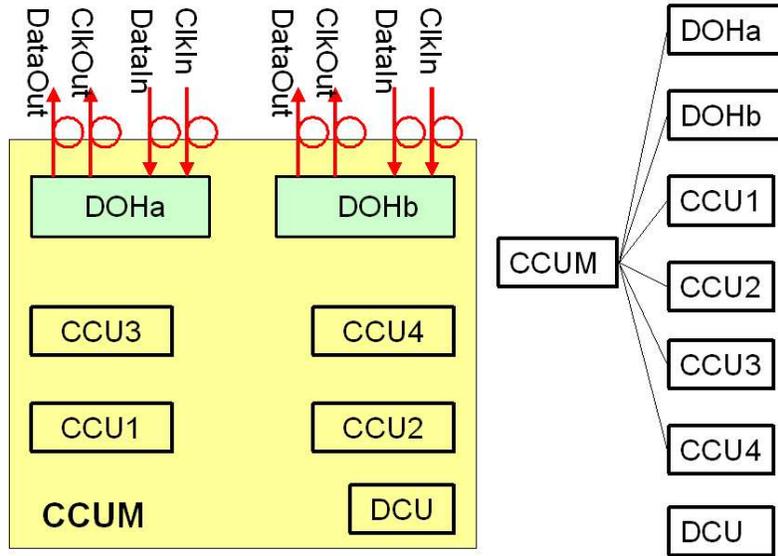


Figure 5: Breakdown of the major components for a CCUM board.

Description	Detector	Side	Groups						Name
Blades Panels Panel ROCs PUC									
TBM	FPix	Bp	D1	BLD1	PNL2	TBM			FPix_Bp_D1_BLD1_PNL2_TBM
DetUnit/PLQ	FPix	Bp	D1	BLD1	PNL2	PLQ1			FPix_Bp_D1_BLD1_PNL2_PLQ1
ROC	FPix	Bp	D1	BLD1	PNL2	PLQ1	ROC2		FPix_Bp_D1_BLD1_PNL2_PLQ1_ROC2
PUC	FPix	Bp	D1	BLD1	PNL2	PLQ1	ROC2	PUC36-48	FPix_Bp_D1_BLD1_PNL2_PLQ1_ROC2_PUC36-48
PRTs PRT									
DOH/PRT	FPix	Bp	D1	PRT1	DOH				FPix_Bp_D1_PRT1_DOH
AOH	FPix	Bp	D1	PRT1	AOH				FPix_Bp_D1_PRT1_AOH
DCU	FPix	Bp	D1	PRT1	DCU				FPix_Bp_D1_PRT1_DCU
CCUMs CCUM									
DOH/CCUM	FPix	Bp	CCUM1	DOH					FPix_Bp_CCUM1_DOHa
CCU	FPix	Bp	CCUM1	CCU1					FPix_Bp_CCUM1_CCU1

Figure 6: Summary of physical naming convention for on-detector components. Examples are used to illustrate this convention.

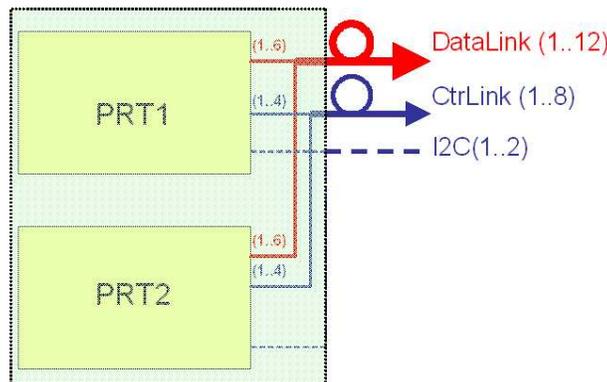


Figure 7: A logical organization of port cards. See the content for detailed descriptions.

3.3 Cabling

The following is just a trying to link the front-end electronics with the VME boards in the US5, which may have nothing to do with the final cable connections for this system. Before doing that, a logical organization of the port cards seems to be very helpful: for port cards on the same disk group, we group the two consecutive port cards into a logical unit, called as a quadrant, as shown in Figure 7. The reasoning is as follows: there are only six optical readout channels and four optical channels for PSI2C communication on each port card; however, to physically connect them to 1:12 connectors of a PxIFED or PxIFEC and save cost, it is very necessary to combine optical channels from port cards; this is done either at PP0 or PP1. A logical naming is given for convenience: CtrLink for PSI2C communications, and DataLink for optical readout channels.

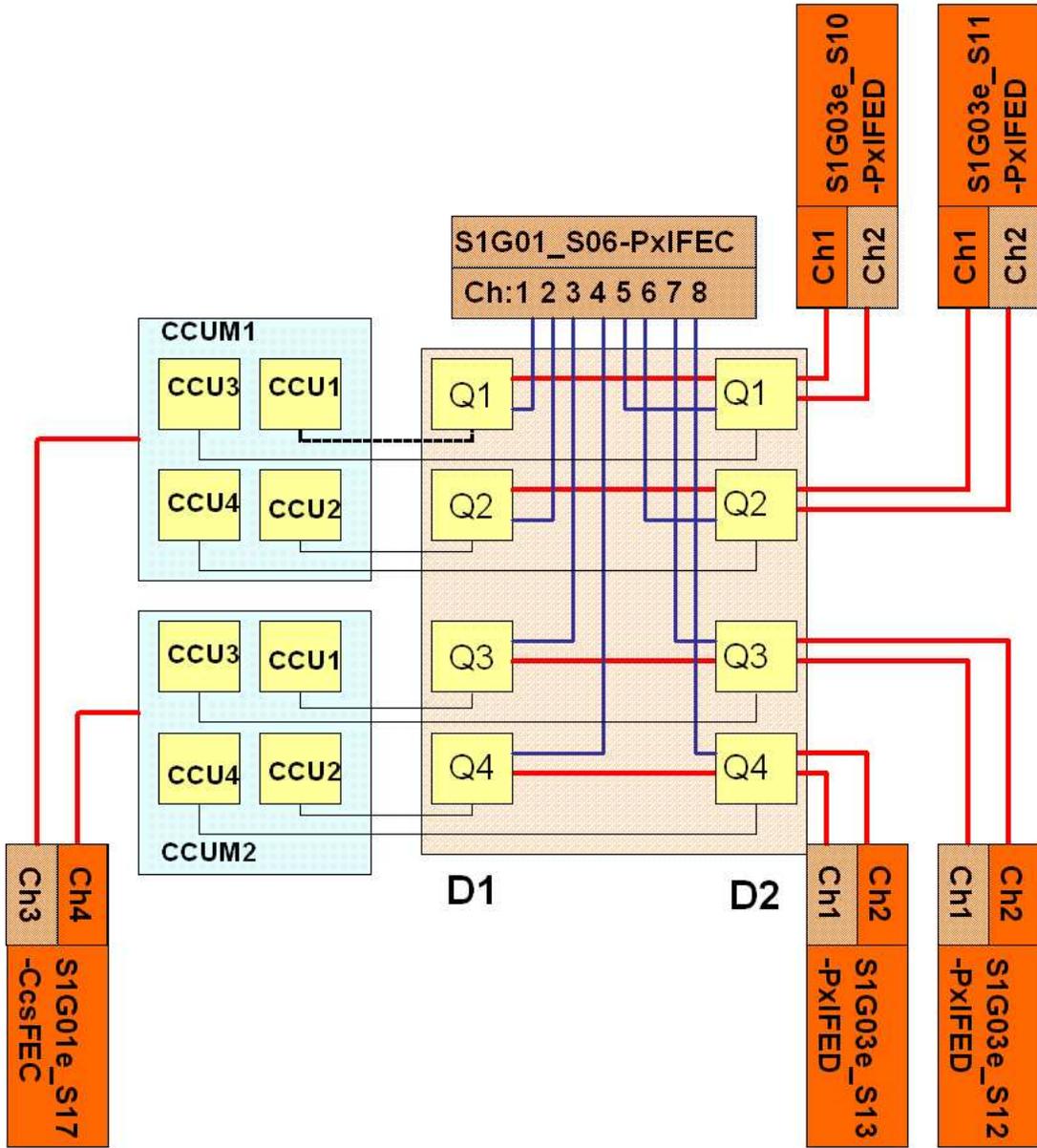


Figure 8: A block diagram of the positive z-axis side of the Forward Pixel detector. The connections are identified between the VME modules and quadrants. Here red lines are 12-channel optical fibers; blue lines are also 12-channel optical fibers, however, only eight of these 12 channels are used; each black line between a quadrant and a CCU contains two I2C network, network one goes to CCU channel one and network two goes to CCU channel two.

As described in Appendix, on a port card, there are total of about 30 registers to control the port card and slow control readouts. These registers are linked in a standard I2C network. When building a port card, chip IDs has

to be set in advance. To avoid I2C address conflict-ions, it is proposed to have an independent I2C net work for each port card. So for a quadrant, these are two I2C networks, which is also shown in Figure 7. The port card with smaller index is on I2C network one.

At this stage, the numbering within a CtrLink or DataLink is not possible to identify. However, it is proposed that the optical links from the port card of smaller index occupy the low six (one to six) or four (one to four) channels of the optical connector; the optical links from the port card of larger index occupy the high six (one to six) or four (eight to twelve) channels of the optical connector

Until now, we can try to lay out the cabling between the front-end to the VME modules in the electronics house. In an attempt, we work this layout for the positive z-axis side of the detector, as shown in Figure 8; the negative z-axis can be worked in a similar way. In this layout, four PxIFED are used to readout the positive z-axis side of the detector; only PxIFEC is used to configure the front-end ROCs; two channels of the CcsFEC are used control two CCU rings, which serves as I2C master to control I2C networks on port cards. We can work out few examples of the cabling as illustration:

S1G03e_S10-PxIFED_Ch1 → FPix_Bp_D1_PRT1(PRT2),

S1G01e_S06-PxIFEC_Ch1 → FPix_Bp_D1_PRT1(PRT2),

S1G01e_S17-CcsFEC_Ch3 → FPix_Bp_CCUM1, FPix_Bp_CCUM1_CCU1 → FPix_Bp_D1_PRT1(PRT2).

For the last example, the connection from the CCU to port cards contains two I2C networks. As a summary, this proposes of one CcsFEC, two PxIFEC, and eight PxIFED to operate and control the Forward Pixel detector.

4 Logical View of the Forward Pixel System

With the proposed control and data links described above, we can try to lay out a logical view of the pixel system on the control & data link side. Figure 9 and Figure 10 show such an attempt to name the electronics components related to the pixel data acquisition system. This scheme could be use in the DAQ configuration & control to access each component.

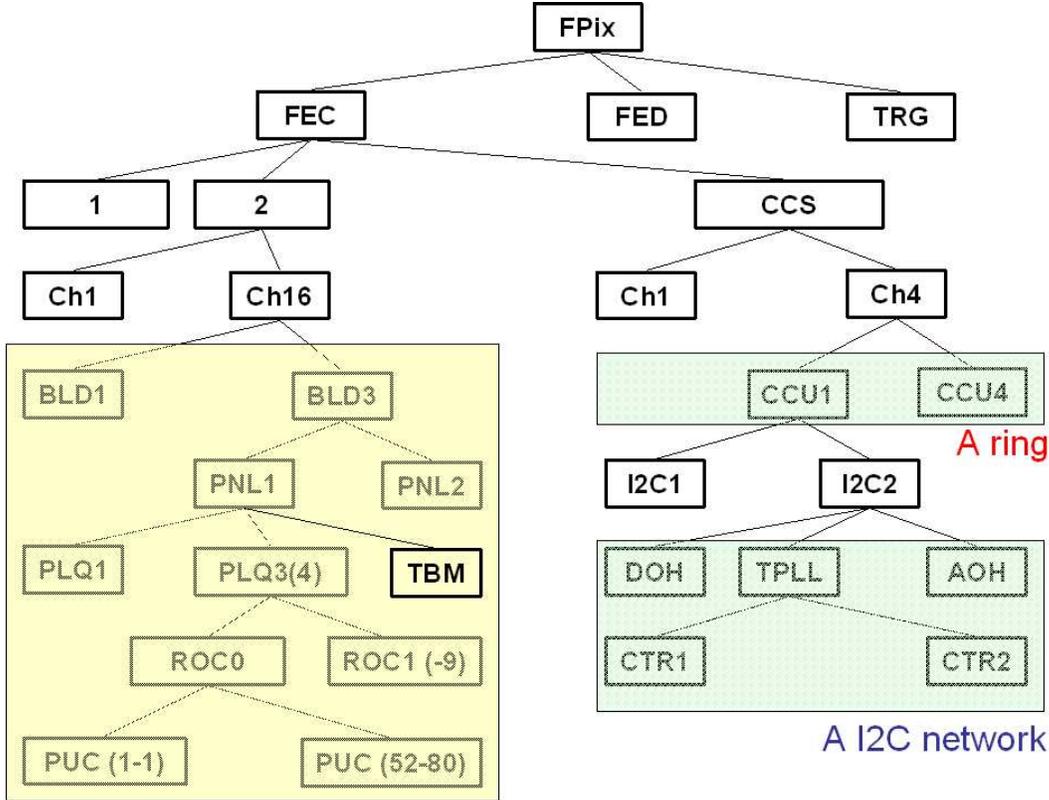


Figure 9: Logical hierarchy of the pixel control system. See content for detailed descriptions.

In Figure 9 and Figure 10, the yellow-shaded region propose to follow the identical structure as proposed in the physical view; whatever modification on physical view will be followed here. The naming of the within a port card are also identical. This is simply because we used a logical breakdown when we do the physical naming. Figure 9 shows the pixel control system, both with PxlFEC and with CcsFEC (or tracker FEC). At each stage of this logical view, a logical name is linked to a physical device/component.

With this logical view, the naming of a ROC can be written as,

$$\text{FPix_FEC1_Ch16_BLD3_PLN1_PLQ3_ROC0}$$

Figure 9 also shows second control line for the pixel detector, which ends up to port card level, where a control ring is built with several CCU devices and each channel of the CCU control a I2C network. This I2C network is physically located on a port card. **The CCUM boards also has a I2C network, which is not listed here yet.** The naming for a TPLL in a I2C network can be written as,

$$\text{FPix_CCS_Ch4_CCU1_I2C2_TPLL.}$$

A register on this TPLL can has a name,

$$\text{FPix_CCS_Ch4_CCU1_I2C2_TPLL_REG0,}$$

where the name of the registers can be referred in the appendix.

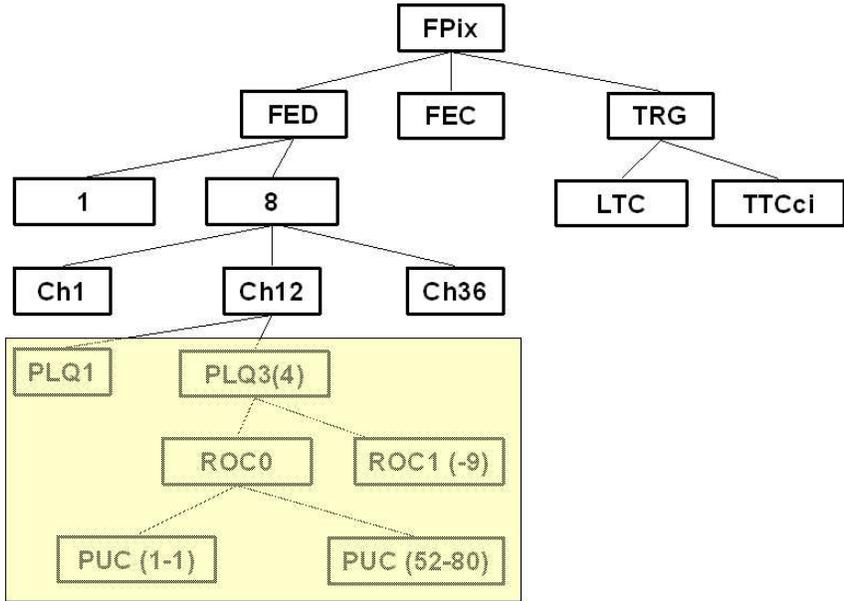


Figure 10: Logical hierarchy of the pixel experimental data-taking components and the trigger components. See content for detailed descriptions.

Figure 10 shows the logical view of the trigger components and the experimental readout. The shaded yellow region is proposed to follow the same convention used in the physical naming and **the breakdown to PUC level might not be necessary here.** Here every FED channels (1 to 36) is used to read out a panel. So a ROC in this view can be named as,

$$\text{FPix_FED1_Ch12_PLQ3_ROC0.}$$

The trigger components are very simple, as shown in the same figure.

5 Few Applications

In the following, we are attempt to work out few examples in the pixel detector operation. Hope this will help us check the consistence of the physical & logical naming.

5.1 Configure a ROC

5.2 Configure a Port Card

5.3 Configure a FED

5.4 Read out RTDs

6 Ongoing work

This has been described in the previous section for now.

References

- [1] G. Cervelli *et al.*, Radiation Tolerant Linear Laser Driver IC (reference and technical manual), CERN-EP Division, Geneva, Switzerland, 2003.
- [2] G. Magazzu, A. Marchioro, and P. Moreira, DCUF User Guide, CERN-EP/MIC, Geneva, Switzerland, 2003.
- [3] P. Placidi, A. Marchioro, and P. Moreira, CMS Trakcer PLL Reference Manual, CERN-EP/MIC, Geneva, Switzerland, 2000.
- [4] H. Correia *et al.*, Delay25, CERN-EP/MIC, Geneva, Switzerland, 2004.

A Linear Laser Driver

The Linear Laser Driver (LLD) used in the Pixel detector is described in Ref. [1]. Here we just summarize the relevant information, the I2C interface, as follows.

The I2C interface of the LLD is a standard I2C protocol. In a 7-bit addressing mode, the highest five bits are decoded as the chip address, which are set by connecting to external pull-down resistors when power up. This also means that there are at most 32 LLDs in a I2C network. The lowest two bits are used to access the four internal registers: REG0 (0x0), REG1 (0x1), REG2 (0x2), and GAINREG (0x3). These registers are seven bits wide. REG0, REG1, and REG2 are used to adjust the bias current for channel 0 to channel 2, respectively. For the DOH, initially these registers are set to 0x70. The GAINREG register sets the gain for each channel, with two bits per channel. The highest bit is used to flag the Single Event Upset (SEU). For DOHs, the initial gain is set to maximum (0x2) for each channel.

B Detector Control Unit

The Detector Control Unit (DCU) is described in Ref. [2]. Here we only summarize the I2C interface. The physical input for each channel need be considered in a later stage. The DCU I2C interface implement the standard I2C protocol. In a 7-bit addressing mode, the most significant four bits are compared with the chip address. The lowest three bits are then used to address the eight internal registers: CREG, SHREG, AREG, LREG, TREG, IDLREG, IDMREG, and IDHREG in correspondence of address 0x0 to 0x7, respectively.

There are eight input channels for each DCU chip. Since the last channel (0x7) is used to connect the embedded temperature sensor, there are at most seven external inputs.

C Tracker PLL

The Tracker PLL [3] also has a standard I2C interface. It uses a 7-bit addressing mode. The five most significant bits are compared to identify the chip address. The lowest two bits are then used to identify the five internal registers: CTR1 (0x0), CTR2 (0x1), CTR3 (0x2), CTR4 (0x3) and CTR5 (0x3). Note that CTR4 and CTR5 share the same I2C address, and they are distinguished by the bit five of CTR2.

D Delay 25

The I2C interface to Delay 25 [4] is implemented with a standard I2C protocol. In a 7-bit addressing mode, the most significant four bits are used to decode the chip address, and the lowest three bits are used to access the six control registers: CR0, CR1, CR2, CR3, CR4, and CR5 with address increased from 0x0 to 0x5, respectively.