

Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB minus	3	7	16r	18	1	1	0	1	2	3	1	0	0	T	9	3	1
HB minus	3	7	15r	13	1	1	1	1	2	3	1	0	1	T	9	3	1
HB minus	3	7	14	14	1	1	2	1	2	3	1	0	2	T	9	3	1
HB minus	3	7	16f	17	1	1	3	2	2	3	1	1	2	T	9	3	1
HB minus	3	7	15f	19	1	1	4	2	2	3	1	1	0	T	9	3	1
HB minus	3	7	13	15	1	1	5	2	2	3	1	1	1	T	9	3	1
HB minus	3	7	10	9	1	2	0	3	2	2	0	1	0	T	9	3	0
HB minus	3	7	6	5	1	2	1	3	2	2	0	1	1	T	9	3	0
HB minus	3	7	2	2	1	2	2	3	2	2	0	1	2	T	9	3	0
HB minus	3	7	12	16	1	2	3	4	2	2	0	0	2	B	9	3	0
HB minus	3	7	8	12	1	2	4	4	2	2	0	0	0	B	9	3	0
HB minus	3	7	4	7	1	2	5	4	2	2	0	0	1	B	9	3	0
HB minus	3	7	11	8	1	3	0	5	2	2	0	1	0	B	9	3	0
HB minus	3	7	7	4	1	3	1	5	2	2	0	1	1	B	9	3	0
HB minus	3	7	3	1	1	3	2	5	2	2	0	1	2	B	9	3	0
HB minus	3	7	9	11	1	3	3	6	2	2	0	0	2	T	9	3	0
HB minus	3	7	5	6	1	3	4	6	2	2	0	0	0	T	9	3	0
HB minus	3	7	1	3	1	3	5	6	2	2	0	0	1	T	9	3	0
Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB minus	3	8	16r	17	2	1	0	1	2	3	1	2	0	T	9	3	1
HB minus	3	8	15r	3	2	1	1	1	2	3	1	2	1	T	9	3	1
HB minus	3	8	14	1	2	1	2	1	2	3	1	2	2	T	9	3	1
HB minus	3	8	16f	19	2	1	3	2	2	3	1	3	2	T	9	3	1
HB minus	3	8	15f	2	2	1	4	2	2	3	1	3	0	T	9	3	1
HB minus	3	8	13	7	2	1	5	2	2	3	1	3	1	T	9	3	1
HB minus	3	8	10	4	2	2	0	3	2	2	0	3	0	T	9	3	0
HB minus	3	8	6	8	2	2	1	3	2	2	0	3	1	T	9	3	0
HB minus	3	8	2	13	2	2	2	3	2	2	0	3	2	T	9	3	0
HB minus	3	8	12	6	2	2	3	4	2	2	0	2	2	B	9	3	0
HB minus	3	8	8	11	2	2	4	4	2	2	0	2	0	B	9	3	0
HB minus	3	8	4	15	2	2	5	4	2	2	0	2	1	B	9	3	0
HB minus	3	8	11	5	2	3	0	5	2	2	0	3	0	B	9	3	0
HB minus	3	8	7	9	2	3	1	5	2	2	0	3	1	B	9	3	0
HB minus	3	8	3	14	2	3	2	5	2	2	0	3	2	B	9	3	0
HB minus	3	8	9	12	2	3	3	6	2	2	0	2	2	T	9	3	0
HB minus	3	8	5	16	2	3	4	6	2	2	0	2	0	T	9	3	0
HB minus	3	8	1	18	2	3	5	6	2	2	0	2	1	T	9	3	0
Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB minus	3	9	16r	3	3	1	0	1	2	3	1	0	0	B	9	3	1
HB minus	3	9	15r	17	3	1	1	1	2	3	1	0	1	B	9	3	1
HB minus	3	9	14	19	3	1	2	1	2	3	1	0	2	B	9	3	1
HB minus	3	9	16f	1	3	1	3	2	2	3	1	1	2	B	9	3	1
HB minus	3	9	15f	18	3	1	4	2	2	3	1	1	0	B	9	3	1
HB minus	3	9	13	13	3	1	5	2	2	3	1	1	1	B	9	3	1
HB minus	3	9	10	16	3	2	0	3	2	2	0	5	0	T	9	3	0
HB minus	3	9	6	12	3	2	1	3	2	2	0	5	1	T	9	3	0
HB minus	3	9	2	7	3	2	2	3	2	2	0	5	2	T	9	3	0
HB minus	3	9	12	14	3	2	3	4	2	2	0	4	2	B	9	3	0
HB minus	3	9	8	9	3	2	4	4	2	2	0	4	0	B	9	3	0

HB minus	3	9	4	5	3	2	5	4	2	2	0	4	1	B	9	3	0
HB minus	3	9	11	15	3	3	0	5	2	2	0	5	0	B	9	3	0
HB minus	3	9	7	11	3	3	1	5	2	2	0	5	1	B	9	3	0
HB minus	3	9	3	6	3	3	2	5	2	2	0	5	2	B	9	3	0
HB minus	3	9	9	8	3	3	3	6	2	2	0	4	2	T	9	3	0
HB minus	3	9	5	4	3	3	4	6	2	2	0	4	0	T	9	3	0
HB minus	3	9	1	2	3	3	5	6	2	2	0	4	1	T	9	3	0
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB minus	3	10	16r	2	4	1	0	1	2	3	1	2	0	B	9	3	1
HB minus	3	10	15r	7	4	1	1	1	2	3	1	2	1	B	9	3	1
HB minus	3	10	14	6	4	1	2	1	2	3	1	2	2	B	9	3	1
HB minus	3	10	16f	3	4	1	3	2	2	3	1	3	2	B	9	3	1
HB minus	3	10	15f	1	4	1	4	2	2	3	1	3	0	B	9	3	1
HB minus	3	10	13	5	4	1	5	2	2	3	1	3	1	B	9	3	1
HB minus	3	10	10	11	4	2	0	3	2	2	0	7	0	T	9	3	0
HB minus	3	10	6	15	4	2	1	3	2	2	0	7	1	T	9	3	0
HB minus	3	10	2	18	4	2	2	3	2	2	0	7	2	T	9	3	0
HB minus	3	10	12	4	4	2	3	4	2	2	0	6	2	B	9	3	0
HB minus	3	10	8	8	4	2	4	4	2	2	0	6	0	B	9	3	0
HB minus	3	10	4	13	4	2	5	4	2	2	0	6	1	B	9	3	0
HB minus	3	10	11	12	4	3	0	5	2	2	0	7	0	B	9	3	0
HB minus	3	10	7	16	4	3	1	5	2	2	0	7	1	B	9	3	0
HB minus	3	10	3	19	4	3	2	5	2	2	0	7	2	B	9	3	0
HB minus	3	10	9	9	4	3	3	6	2	2	0	6	2	T	9	3	0
HB minus	3	10	5	14	4	3	4	6	2	2	0	6	0	T	9	3	0
HB minus	3	10	1	17	4	3	5	6	2	2	0	6	1	T	9	3	0
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	3	7	17	12	1	1	0	1	2	3	1	4	0	T	9	3	1
HE minus	3	7	16	16	1	1	1	1	2	3	1	4	1	T	9	3	1
HE minus	3	7-8	26f	7	1	1	2	1	2	3	1	4	2	T	9	3	1
HE minus	3	7-8	26r	3	1	1	3	2	2	3	1	5	2	T	9	3	1
HE minus	3	7	18f	11	1	1	4	2	2	3	1	5	0	T	9	3	1
HE minus	3	7	18r	19	1	1	5	2	2	3	1	5	1	T	9	3	1
HE minus	3	7-8	28f	15	1	2	0	3	2	4	2	0	0	B	9	3	2
HE minus	3	7-8	28m	2	1	2	1	3	2	4	2	0	1	B	9	3	2
HE minus	3	7-8	29f	6	1	2	2	3	2	4	2	0	2	B	9	3	2
HE minus	3	7-8	28r	5	1	2	3	4	2	4	2	1	2	B	9	3	2
HE minus	3	7-8	24r	14	1	2	4	4	2	4	2	1	0	B	9	3	2
HE minus	3	7-8	24f	18	1	2	5	4	2	4	2	1	1	B	9	3	2
HE minus	3	7	19r	17	1	3	0	5	2	4	2	0	0	T	9	3	2
HE minus	3	7	20f	9	1	3	1	5	2	4	2	0	1	T	9	3	2
HE minus	3	7-8	22r	4	1	3	2	5	2	4	2	0	2	T	9	3	2
HE minus	3	7	19f	13	1	3	3	6	2	4	2	1	2	T	9	3	2
HE minus	3	7	20r	8	1	3	4	6	2	4	2	1	0	T	9	3	2
HE minus	3	7-8	22f	1	1	3	5	6	2	4	2	1	1	T	9	3	2
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	3	8	17	12	2	1	0	1	2	3	1	6	0	T	9	3	1
HE minus	3	8	16	7	2	1	1	1	2	3	1	6	1	T	9	3	1
HE minus	3	7-8	25f	16	2	1	2	1	2	3	1	6	2	T	9	3	1
HE minus	3	7-8	25r	19	2	1	3	2	2	3	1	7	2	T	9	3	1
HE minus	3	8	18f	11	2	1	4	2	2	3	1	7	0	T	9	3	1

HE minus	3	8	18r	3	2	1	5	2	2	3	1	7	1	T	9	3	1
HE minus	3	7-8	27f	15	2	2	0	3	2	4	2	4	0	B	9	3	2
HE minus	3	7-8	27m	18	2	2	1	3	2	4	2	4	1	B	9	3	2
HE minus	3	7-8	29m	6	2	2	2	3	2	4	2	4	2	B	9	3	2
HE minus	3	7-8	23f	2	2	2	3	4	2	4	2	5	2	B	9	3	2
HE minus	3	7-8	27r	14	2	2	4	4	2	4	2	5	0	B	9	3	2
HE minus	3	7-8	23r	5	2	2	5	4	2	4	2	5	1	B	9	3	2
HE minus	3	8	19r	1	2	3	0	5	2	4	2	2	0	T	9	3	2
HE minus	3	8	20f	9	2	3	1	5	2	4	2	2	1	T	9	3	2
HE minus	3	7-8	21r	17	2	3	2	5	2	4	2	2	2	T	9	3	2
HE minus	3	8	21f	13	2	3	3	6	2	4	2	3	2	T	9	3	2
HE minus	3	8	19f	4	2	3	4	6	2	4	2	3	0	T	9	3	2
HE minus	3	7-8	20r	8	2	3	5	6	2	4	2	3	1	T	9	3	2
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	3	9	17	12	3	1	0	1	2	3	1	4	0	B	9	3	1
HE minus	3	9	16	16	3	1	1	1	2	3	1	4	1	B	9	3	1
HE minus	3	9-10	25f	7	3	1	2	1	2	3	1	4	2	B	9	3	1
HE minus	3	0-10	25r	3	3	1	3	2	2	3	1	5	2	B	9	3	1
HE minus	3	9	18f	11	3	1	4	2	2	3	1	5	0	B	9	3	1
HE minus	3	9	18r	19	3	1	5	2	2	3	1	5	1	B	9	3	1
HE minus	3	9-10	27f	6	3	2	0	3	2	4	2	6	0	B	9	3	2
HE minus	3	9-10	27m	2	3	2	1	3	2	4	2	6	1	B	9	3	2
HE minus	3	9-10	29m	15	3	2	2	3	2	4	2	6	2	B	9	3	2
HE minus	3	9-10	23f	18	3	2	3	4	2	4	2	7	2	B	9	3	2
HE minus	3	9-10	27r	5	3	2	4	4	2	4	2	7	0	B	9	3	2
HE minus	3	9-10	23r	14	3	2	5	4	2	4	2	7	1	B	9	3	2
HE minus	3	9	19r	17	3	3	0	5	2	4	2	6	0	T	9	3	2
HE minus	3	9	20f	9	3	3	1	5	2	4	2	6	1	T	9	3	2
HE minus	3	9-10	21r	1	3	3	2	5	2	4	2	6	2	T	9	3	2
HE minus	3	9	21f	4	3	3	3	6	2	4	2	7	2	T	9	3	2
HE minus	3	9	19f	13	3	3	4	6	2	4	2	7	0	T	9	3	2
HE minus	3	9-10	20r	8	3	3	5	6	2	4	2	7	1	T	9	3	2
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	3	10	17	12	4	1	0	1	2	3	1	6	0	B	9	3	1
HE minus	3	10	16	7	4	1	1	1	2	3	1	6	1	B	9	3	1
HE minus	3	9-10	26f	16	4	1	2	1	2	3	1	6	2	B	9	3	1
HE minus	3	0-10	26r	19	4	1	3	2	2	3	1	7	2	B	9	3	1
HE minus	3	10	18f	11	4	1	4	2	2	3	1	7	0	B	9	3	1
HE minus	3	10	18r	3	4	1	5	2	2	3	1	7	1	B	9	3	1
HE minus	3	9-10	28f	6	4	2	0	3	2	4	2	2	0	B	9	3	2
HE minus	3	9-10	28m	18	4	2	1	3	2	4	2	2	1	B	9	3	2
HE minus	3	9-10	29f	15	4	2	2	3	2	4	2	2	2	B	9	3	2
HE minus	3	9-10	28r	14	4	2	3	4	2	4	2	3	2	B	9	3	2
HE minus	3	9-10	24r	5	4	2	4	4	2	4	2	3	0	B	9	3	2
HE minus	3	9-10	24f	2	4	2	5	4	2	4	2	3	1	B	9	3	2
HE minus	3	10	19r	1	4	3	0	5	2	4	2	4	0	T	9	3	2
HE minus	3	10	20f	9	4	3	1	5	2	4	2	4	1	T	9	3	2
HE minus	3	9-10	22r	17	4	3	2	5	2	4	2	4	2	T	9	3	2
HE minus	3	10	19f	4	4	3	3	6	2	4	2	5	2	T	9	3	2
HE minus	3	10	20r	8	4	3	4	6	2	4	2	5	0	T	9	3	2
HE minus	3	9-10	22f	13	4	3	5	6	2	4	2	5	1	T	9	3	2

Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB plus	3	7	16r	2	4	1	0	1	2	6	4	0	0	T	9	3	4
HB plus	3	7	15r	7	4	1	1	1	2	6	4	0	1	T	9	3	4
HB plus	3	7	14	6	4	1	2	1	2	6	4	0	2	T	9	3	4
HB plus	3	7	16f	3	4	1	3	2	2	6	4	1	2	T	9	3	4
HB plus	3	7	15f	1	4	1	4	2	2	6	4	1	0	T	9	3	4
HB plus	3	7	13	5	4	1	5	2	2	6	4	1	1	T	9	3	4
HB plus	3	7	10	11	4	2	0	3	2	5	3	1	0	T	9	3	3
HB plus	3	7	6	15	4	2	1	3	2	5	3	1	1	T	9	3	3
HB plus	3	7	2	18	4	2	2	3	2	5	3	1	2	T	9	3	3
HB plus	3	7	12	4	4	2	3	4	2	5	3	0	2	B	9	3	3
HB plus	3	7	8	8	4	2	4	4	2	5	3	0	0	B	9	3	3
HB plus	3	7	4	13	4	2	5	4	2	5	3	0	1	B	9	3	3
HB plus	3	7	11	12	4	3	0	5	2	5	3	1	0	B	9	3	3
HB plus	3	7	7	16	4	3	1	5	2	5	3	1	1	B	9	3	3
HB plus	3	7	3	19	4	3	2	5	2	5	3	1	2	B	9	3	3
HB plus	3	7	9	9	4	3	3	6	2	5	3	0	2	T	9	3	3
HB plus	3	7	5	14	4	3	4	6	2	5	3	0	0	T	9	3	3
HB plus	3	7	1	17	4	3	5	6	2	5	3	0	1	T	9	3	3
Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB plus	3	8	16r	3	3	1	0	1	2	6	4	2	0	T	9	3	4
HB plus	3	8	15r	17	3	1	1	1	2	6	4	2	1	T	9	3	4
HB plus	3	8	14	19	3	1	2	1	2	6	4	2	2	T	9	3	4
HB plus	3	8	16f	1	3	1	3	2	2	6	4	3	2	T	9	3	4
HB plus	3	8	15f	18	3	1	4	2	2	6	4	3	0	T	9	3	4
HB plus	3	8	13	13	3	1	5	2	2	6	4	3	1	T	9	3	4
HB plus	3	8	10	16	3	2	0	3	2	5	3	3	0	T	9	3	3
HB plus	3	8	6	12	3	2	1	3	2	5	3	3	1	T	9	3	3
HB plus	3	8	2	7	3	2	2	3	2	5	3	3	2	T	9	3	3
HB plus	3	8	12	14	3	2	3	4	2	5	3	2	2	B	9	3	3
HB plus	3	8	8	9	3	2	4	4	2	5	3	2	0	B	9	3	3
HB plus	3	8	4	5	3	2	5	4	2	5	3	2	1	B	9	3	3
HB plus	3	8	11	15	3	3	0	5	2	5	3	3	0	B	9	3	3
HB plus	3	8	7	11	3	3	1	5	2	5	3	3	1	B	9	3	3
HB plus	3	8	3	6	3	3	2	5	2	5	3	3	2	B	9	3	3
HB plus	3	8	9	8	3	3	3	6	2	5	3	2	2	T	9	3	3
HB plus	3	8	5	4	3	3	4	6	2	5	3	2	0	T	9	3	3
HB plus	3	8	1	2	3	3	5	6	2	5	3	2	1	T	9	3	3
Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB plus	3	9	16r	17	2	1	0	1	2	6	4	0	0	B	9	3	4
HB plus	3	9	15r	3	2	1	1	1	2	6	4	0	1	B	9	3	4
HB plus	3	9	14	1	2	1	2	1	2	6	4	0	2	B	9	3	4
HB plus	3	9	16f	19	2	1	3	2	2	6	4	1	2	B	9	3	4
HB plus	3	9	15f	2	2	1	4	2	2	6	4	1	0	B	9	3	4
HB plus	3	9	13	7	2	1	5	2	2	6	4	1	1	B	9	3	4
HB plus	3	9	10	4	2	2	0	3	2	5	3	5	0	T	9	3	3
HB plus	3	9	6	8	2	2	1	3	2	5	3	5	1	T	9	3	3
HB plus	3	9	2	13	2	2	2	3	2	5	3	5	2	T	9	3	3
HB plus	3	9	12	6	2	2	3	4	2	5	3	4	2	B	9	3	3
HB plus	3	9	8	11	2	2	4	4	2	5	3	4	0	B	9	3	3
HB plus	3	9	4	15	2	2	5	4	2	5	3	4	1	B	9	3	3

HB plus	3	9	11	5	2	3	0	5	2	5	3	5	0	B	9	3	3
HB plus	3	9	7	9	2	3	1	5	2	5	3	5	1	B	9	3	3
HB plus	3	9	3	14	2	3	2	5	2	5	3	5	2	B	9	3	3
HB plus	3	9	9	12	2	3	3	6	2	5	3	4	2	T	9	3	3
HB plus	3	9	5	16	2	3	4	6	2	5	3	4	0	T	9	3	3
HB plus	3	9	1	18	2	3	5	6	2	5	3	4	1	T	9	3	3
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB plus	3	10	16r	18	1	1	0	1	2	6	4	2	0	B	9	3	4
HB plus	3	10	15r	13	1	1	1	1	2	6	4	2	1	B	9	3	4
HB plus	3	10	14	14	1	1	2	1	2	6	4	2	2	B	9	3	4
HB plus	3	10	16f	17	1	1	3	2	2	6	4	3	2	B	9	3	4
HB plus	3	10	15f	19	1	1	4	2	2	6	4	3	0	B	9	3	4
HB plus	3	10	13	15	1	1	5	2	2	6	4	3	1	B	9	3	4
HB plus	3	10	10	9	1	2	0	3	2	5	3	7	0	T	9	3	3
HB plus	3	10	6	5	1	2	1	3	2	5	3	7	1	T	9	3	3
HB plus	3	10	2	2	1	2	2	3	2	5	3	7	2	T	9	3	3
HB plus	3	10	12	16	1	2	3	4	2	5	3	6	2	B	9	3	3
HB plus	3	10	8	12	1	2	4	4	2	5	3	6	0	B	9	3	3
HB plus	3	10	4	7	1	2	5	4	2	5	3	6	1	B	9	3	3
HB plus	3	10	11	8	1	3	0	5	2	5	3	7	0	B	9	3	3
HB plus	3	10	7	4	1	3	1	5	2	5	3	7	1	B	9	3	3
HB plus	3	10	3	1	1	3	2	5	2	5	3	7	2	B	9	3	3
HB plus	3	10	9	11	1	3	3	6	2	5	3	6	2	T	9	3	3
HB plus	3	10	5	6	1	3	4	6	2	5	3	6	0	T	9	3	3
HB plus	3	10	1	3	1	3	5	6	2	5	3	6	1	T	9	3	3
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	3	7	17	12	4	1	0	1	2	6	4	4	0	T	9	3	4
HE plus	3	7	16	7	4	1	1	1	2	6	4	4	1	T	9	3	4
HE plus	3	7-8	26f	16	4	1	2	1	2	6	4	4	2	T	9	3	4
HE plus	3	7-8	26r	19	4	1	3	2	2	6	4	5	2	T	9	3	4
HE plus	3	7	18f	11	4	1	4	2	2	6	4	5	0	T	9	3	4
HE plus	3	7	18r	3	4	1	5	2	2	6	4	5	1	T	9	3	4
HE plus	3	7-8	28f	6	4	2	0	3	2	7	5	0	0	B	9	3	5
HE plus	3	7-8	28m	18	4	2	1	3	2	7	5	0	1	B	9	3	5
HE plus	3	7-8	29f	15	4	2	2	3	2	7	5	0	2	B	9	3	5
HE plus	3	7-8	28r	14	4	2	3	4	2	7	5	1	2	B	9	3	5
HE plus	3	7-8	24r	5	4	2	4	4	2	7	5	1	0	B	9	3	5
HE plus	3	7-8	24f	2	4	2	5	4	2	7	5	1	1	B	9	3	5
HE plus	3	7	19r	1	4	3	0	5	2	7	5	0	0	T	9	3	5
HE plus	3	7	20f	9	4	3	1	5	2	7	5	0	1	T	9	3	5
HE plus	3	7-8	22r	17	4	3	2	5	2	7	5	0	2	T	9	3	5
HE plus	3	7	19f	4	4	3	3	6	2	7	5	1	2	T	9	3	5
HE plus	3	7	20r	8	4	3	4	6	2	7	5	1	0	T	9	3	5
HE plus	3	7-8	22f	13	4	3	5	6	2	7	5	1	1	T	9	3	5
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	3	8	17	12	3	1	0	1	2	6	4	6	0	T	9	3	4
HE plus	3	8	16	16	3	1	1	1	2	6	4	6	1	T	9	3	4
HE plus	3	7-8	25f	7	3	1	2	1	2	6	4	6	2	T	9	3	4
HE plus	3	7-8	25r	3	3	1	3	2	2	6	4	7	2	T	9	3	4
HE plus	3	8	18f	11	3	1	4	2	2	6	4	7	0	T	9	3	4
HE plus	3	8	18r	19	3	1	5	2	2	6	4	7	1	T	9	3	4

HE plus	3	7-8	27f	6	3	2	0	3	2	7	5	4	0	B	9	3	5
HE plus	3	7-8	27m	2	3	2	1	3	2	7	5	4	1	B	9	3	5
HE plus	3	7-8	29m	15	3	2	2	3	2	7	5	4	2	B	9	3	5
HE plus	3	7-8	23f	18	3	2	3	4	2	7	5	5	2	B	9	3	5
HE plus	3	7-8	27r	5	3	2	4	4	2	7	5	5	0	B	9	3	5
HE plus	3	7-8	23r	14	3	2	5	4	2	7	5	5	1	B	9	3	5
HE plus	3	8	19r	17	3	3	0	5	2	7	5	2	0	T	9	3	5
HE plus	3	8	20f	9	3	3	1	5	2	7	5	2	1	T	9	3	5
HE plus	3	7-8	21r	1	3	3	2	5	2	7	5	2	2	T	9	3	5
HE plus	3	8	21f	4	3	3	3	6	2	7	5	3	2	T	9	3	5
HE plus	3	8	19f	13	3	3	4	6	2	7	5	3	0	T	9	3	5
HE plus	3	7-8	20r	8	3	3	5	6	2	7	5	3	1	T	9	3	5
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	3	9	17	12	2	1	0	1	2	6	4	4	0	B	9	3	4
HE plus	3	9	16	7	2	1	1	1	2	6	4	4	1	B	9	3	4
HE plus	3	9-10	25f	16	2	1	2	1	2	6	4	4	2	B	9	3	4
HE plus	3	0-10	25r	19	2	1	3	2	2	6	4	5	2	B	9	3	4
HE plus	3	9	18f	11	2	1	4	2	2	6	4	5	0	B	9	3	4
HE plus	3	9	18r	3	2	1	5	2	2	6	4	5	1	B	9	3	4
HE plus	3	9-10	27f	15	2	2	0	3	2	7	5	6	0	B	9	3	5
HE plus	3	9-10	27m	18	2	2	1	3	2	7	5	6	1	B	9	3	5
HE plus	3	9-10	29m	6	2	2	2	3	2	7	5	6	2	B	9	3	5
HE plus	3	9-10	23f	2	2	2	3	4	2	7	5	7	2	B	9	3	5
HE plus	3	9-10	27r	14	2	2	4	4	2	7	5	7	0	B	9	3	5
HE plus	3	9-10	23r	5	2	2	5	4	2	7	5	7	1	B	9	3	5
HE plus	3	9	19r	1	2	3	0	5	2	7	5	6	0	T	9	3	5
HE plus	3	9	20f	9	2	3	1	5	2	7	5	6	1	T	9	3	5
HE plus	3	9-10	21r	17	2	3	2	5	2	7	5	6	2	T	9	3	5
HE plus	3	9	21f	13	2	3	3	6	2	7	5	7	2	T	9	3	5
HE plus	3	9	19f	4	2	3	4	6	2	7	5	7	0	T	9	3	5
HE plus	3	9-10	20r	8	2	3	5	6	2	7	5	7	1	T	9	3	5
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	3	10	17	12	1	1	0	1	2	6	4	6	0	B	9	3	4
HE plus	3	10	16	16	1	1	1	1	2	6	4	6	1	B	9	3	4
HE plus	3	9-10	26f	7	1	1	2	1	2	6	4	6	2	B	9	3	4
HE plus	3	0-10	26r	3	1	1	3	2	2	6	4	7	2	B	9	3	4
HE plus	3	10	18f	11	1	1	4	2	2	6	4	7	0	B	9	3	4
HE plus	3	10	18r	19	1	1	5	2	2	6	4	7	1	B	9	3	4
HE plus	3	9-10	28f	15	1	2	0	3	2	7	5	2	0	B	9	3	5
HE plus	3	9-10	28m	2	1	2	1	3	2	7	5	2	1	B	9	3	5
HE plus	3	9-10	29f	6	1	2	2	3	2	7	5	2	2	B	9	3	5
HE plus	3	9-10	28r	5	1	2	3	4	2	7	5	3	2	B	9	3	5
HE plus	3	9-10	24r	14	1	2	4	4	2	7	5	3	0	B	9	3	5
HE plus	3	9-10	24f	18	1	2	5	4	2	7	5	3	1	B	9	3	5
HE plus	3	10	19r	17	1	3	0	5	2	7	5	4	0	T	9	3	5
HE plus	3	10	20f	9	1	3	1	5	2	7	5	4	1	T	9	3	5
HE plus	3	9-10	22r	4	1	3	2	5	2	7	5	4	2	T	9	3	5
HE plus	3	10	19f	13	1	3	3	6	2	7	5	5	2	T	9	3	5
HE plus	3	10	20r	8	1	3	4	6	2	7	5	5	0	T	9	3	5
HE plus	3	9-10	22f	1	1	3	5	6	2	7	5	5	1	T	9	3	5
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	

HB minus	4	11	16r	18	1	1	0	1	2	14	7	0	0	T	19	4	7
HB minus	4	11	15r	13	1	1	1	1	2	14	7	0	1	T	19	4	7
HB minus	4	11	14	14	1	1	2	1	2	14	7	0	2	T	19	4	7
HB minus	4	11	16f	17	1	1	3	2	2	14	7	1	2	T	19	4	7
HB minus	4	11	15f	19	1	1	4	2	2	14	7	1	0	T	19	4	7
HB minus	4	11	13	15	1	1	5	2	2	14	7	1	1	T	19	4	7
HB minus	4	11	10	9	1	2	0	3	2	13	6	1	0	T	19	4	6
HB minus	4	11	6	5	1	2	1	3	2	13	6	1	1	T	19	4	6
HB minus	4	11	2	2	1	2	2	3	2	13	6	1	2	T	19	4	6
HB minus	4	11	12	16	1	2	3	4	2	13	6	0	2	B	19	4	6
HB minus	4	11	8	12	1	2	4	4	2	13	6	0	0	B	19	4	6
HB minus	4	11	4	7	1	2	5	4	2	13	6	0	1	B	19	4	6
HB minus	4	11	11	8	1	3	0	5	2	13	6	1	0	B	19	4	6
HB minus	4	11	7	4	1	3	1	5	2	13	6	1	1	B	19	4	6
HB minus	4	11	3	1	1	3	2	5	2	13	6	1	2	B	19	4	6
HB minus	4	11	9	11	1	3	3	6	2	13	6	0	2	T	19	4	6
HB minus	4	11	5	6	1	3	4	6	2	13	6	0	0	T	19	4	6
HB minus	4	11	1	3	1	3	5	6	2	13	6	0	1	T	19	4	6
Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB minus	4	12	16r	17	2	1	0	1	2	14	7	2	0	T	19	4	7
HB minus	4	12	15r	3	2	1	1	1	2	14	7	2	1	T	19	4	7
HB minus	4	12	14	1	2	1	2	1	2	14	7	2	2	T	19	4	7
HB minus	4	12	16f	19	2	1	3	2	2	14	7	3	2	T	19	4	7
HB minus	4	12	15f	2	2	1	4	2	2	14	7	3	0	T	19	4	7
HB minus	4	12	13	7	2	1	5	2	2	14	7	3	1	T	19	4	7
HB minus	4	12	10	4	2	2	0	3	2	13	6	3	0	T	19	4	6
HB minus	4	12	6	8	2	2	1	3	2	13	6	3	1	T	19	4	6
HB minus	4	12	2	13	2	2	2	3	2	13	6	3	2	T	19	4	6
HB minus	4	12	12	6	2	2	3	4	2	13	6	2	2	B	19	4	6
HB minus	4	12	8	11	2	2	4	4	2	13	6	2	0	B	19	4	6
HB minus	4	12	4	15	2	2	5	4	2	13	6	2	1	B	19	4	6
HB minus	4	12	11	5	2	3	0	5	2	13	6	3	0	B	19	4	6
HB minus	4	12	7	9	2	3	1	5	2	13	6	3	1	B	19	4	6
HB minus	4	12	3	14	2	3	2	5	2	13	6	3	2	B	19	4	6
HB minus	4	12	9	12	2	3	3	6	2	13	6	2	2	T	19	4	6
HB minus	4	12	5	16	2	3	4	6	2	13	6	2	0	T	19	4	6
HB minus	4	12	1	18	2	3	5	6	2	13	6	2	1	T	19	4	6
Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB minus	4	13	16r	3	3	1	0	1	2	14	7	0	0	B	19	4	7
HB minus	4	13	15r	17	3	1	1	1	2	14	7	0	1	B	19	4	7
HB minus	4	13	14	19	3	1	2	1	2	14	7	0	2	B	19	4	7
HB minus	4	13	16f	1	3	1	3	2	2	14	7	1	2	B	19	4	7
HB minus	4	13	15f	18	3	1	4	2	2	14	7	1	0	B	19	4	7
HB minus	4	13	13	13	3	1	5	2	2	14	7	1	1	B	19	4	7
HB minus	4	13	10	16	3	2	0	3	2	13	6	5	0	T	19	4	6
HB minus	4	13	6	12	3	2	1	3	2	13	6	5	1	T	19	4	6
HB minus	4	13	2	7	3	2	2	3	2	13	6	5	2	T	19	4	6
HB minus	4	13	12	14	3	2	3	4	2	13	6	4	2	B	19	4	6
HB minus	4	13	8	9	3	2	4	4	2	13	6	4	0	B	19	4	6
HB minus	4	13	4	5	3	2	5	4	2	13	6	4	1	B	19	4	6
HB minus	4	13	11	15	3	3	0	5	2	13	6	5	0	B	19	4	6

HB minus	4	13	7	11	3	3	1	5	2	13	6	5	1	B	19	4	6
HB minus	4	13	3	6	3	3	2	5	2	13	6	5	2	B	19	4	6
HB minus	4	13	9	8	3	3	3	6	2	13	6	4	2	T	19	4	6
HB minus	4	13	5	4	3	3	4	6	2	13	6	4	0	T	19	4	6
HB minus	4	13	1	2	3	3	5	6	2	13	6	4	1	T	19	4	6
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB minus	4	14	16r	2	4	1	0	1	2	14	7	2	0	B	19	4	7
HB minus	4	14	15r	7	4	1	1	1	2	14	7	2	1	B	19	4	7
HB minus	4	14	14	6	4	1	2	1	2	14	7	2	2	B	19	4	7
HB minus	4	14	16f	3	4	1	3	2	2	14	7	3	2	B	19	4	7
HB minus	4	14	15f	1	4	1	4	2	2	14	7	3	0	B	19	4	7
HB minus	4	14	13	5	4	1	5	2	2	14	7	3	1	B	19	4	7
HB minus	4	14	10	11	4	2	0	3	2	13	6	7	0	T	19	4	6
HB minus	4	14	6	15	4	2	1	3	2	13	6	7	1	T	19	4	6
HB minus	4	14	2	18	4	2	2	3	2	13	6	7	2	T	19	4	6
HB minus	4	14	12	4	4	2	3	4	2	13	6	6	2	B	19	4	6
HB minus	4	14	8	8	4	2	4	4	2	13	6	6	0	B	19	4	6
HB minus	4	14	4	13	4	2	5	4	2	13	6	6	1	B	19	4	6
HB minus	4	14	11	12	4	3	0	5	2	13	6	7	0	B	19	4	6
HB minus	4	14	7	16	4	3	1	5	2	13	6	7	1	B	19	4	6
HB minus	4	14	3	19	4	3	2	5	2	13	6	7	2	B	19	4	6
HB minus	4	14	9	9	4	3	3	6	2	13	6	6	2	T	19	4	6
HB minus	4	14	5	14	4	3	4	6	2	13	6	6	0	T	19	4	6
HB minus	4	14	1	17	4	3	5	6	2	13	6	6	1	T	19	4	6
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	4	11	17	12	1	1	0	1	2	14	7	4	0	T	19	4	7
HE minus	4	11	16	16	1	1	1	1	2	14	7	4	1	T	19	4	7
HE minus	4	11-12	26f	7	1	1	2	1	2	14	7	4	2	T	19	4	7
HE minus	4	11-12	26r	3	1	1	3	2	2	14	7	5	2	T	19	4	7
HE minus	4	11	18f	11	1	1	4	2	2	14	7	5	0	T	19	4	7
HE minus	4	11	18r	19	1	1	5	2	2	14	7	5	1	T	19	4	7
HE minus	4	11-12	28f	15	1	2	0	3	2	15	8	0	0	B	19	4	8
HE minus	4	11-12	28m	2	1	2	1	3	2	15	8	0	1	B	19	4	8
HE minus	4	11-12	29f	6	1	2	2	3	2	15	8	0	2	B	19	4	8
HE minus	4	11-12	28r	5	1	2	3	4	2	15	8	1	2	B	19	4	8
HE minus	4	11-12	24r	14	1	2	4	4	2	15	8	1	0	B	19	4	8
HE minus	4	11-12	24f	18	1	2	5	4	2	15	8	1	1	B	19	4	8
HE minus	4	11	19r	17	1	3	0	5	2	15	8	0	0	T	19	4	8
HE minus	4	11	20f	9	1	3	1	5	2	15	8	0	1	T	19	4	8
HE minus	4	11-12	22r	4	1	3	2	5	2	15	8	0	2	T	19	4	8
HE minus	4	11	19f	13	1	3	3	6	2	15	8	1	2	T	19	4	8
HE minus	4	11	20r	8	1	3	4	6	2	15	8	1	0	T	19	4	8
HE minus	4	11-12	22f	1	1	3	5	6	2	15	8	1	1	T	19	4	8
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	4	12	17	12	2	1	0	1	2	14	7	6	0	T	19	4	7
HE minus	4	12	16	7	2	1	1	1	2	14	7	6	1	T	19	4	7
HE minus	4	11-12	25f	16	2	1	2	1	2	14	7	6	2	T	19	4	7
HE minus	4	11-12	25r	19	2	1	3	2	2	14	7	7	2	T	19	4	7
HE minus	4	12	18f	11	2	1	4	2	2	14	7	7	0	T	19	4	7
HE minus	4	12	18r	3	2	1	5	2	2	14	7	7	1	T	19	4	7
HE minus	4	11-12	27f	15	2	2	0	3	2	15	8	4	0	B	19	4	8

HE minus	4	11-12	27m	18	2	2	1	3	2	15	8	4	1	B	19	4	8
HE minus	4	11-12	29m	6	2	2	2	3	2	15	8	4	2	B	19	4	8
HE minus	4	11-12	23f	2	2	2	3	4	2	15	8	5	2	B	19	4	8
HE minus	4	11-12	27r	14	2	2	4	4	2	15	8	5	0	B	19	4	8
HE minus	4	11-12	23r	5	2	2	5	4	2	15	8	5	1	B	19	4	8
HE minus	4	12	19r	1	2	3	0	5	2	15	8	2	0	T	19	4	8
HE minus	4	12	20f	9	2	3	1	5	2	15	8	2	1	T	19	4	8
HE minus	4	11-12	21r	17	2	3	2	5	2	15	8	2	2	T	19	4	8
HE minus	4	12	21f	13	2	3	3	6	2	15	8	3	2	T	19	4	8
HE minus	4	12	19f	4	2	3	4	6	2	15	8	3	0	T	19	4	8
HE minus	4	11-12	20r	8	2	3	5	6	2	15	8	3	1	T	19	4	8
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	4	13	17	12	3	1	0	1	2	14	7	4	0	B	19	4	7
HE minus	4	13	16	16	3	1	1	1	2	14	7	4	1	B	19	4	7
HE minus	4	13-14	25f	7	3	1	2	1	2	14	7	4	2	B	19	4	7
HE minus	4	13-14	25r	3	3	1	3	2	2	14	7	5	2	B	19	4	7
HE minus	4	13	18f	11	3	1	4	2	2	14	7	5	0	B	19	4	7
HE minus	4	13	18r	19	3	1	5	2	2	14	7	5	1	B	19	4	7
HE minus	4	13-14	27f	6	3	2	0	3	2	15	8	6	0	B	19	4	8
HE minus	4	13-14	27m	2	3	2	1	3	2	15	8	6	1	B	19	4	8
HE minus	4	13-14	29m	15	3	2	2	3	2	15	8	6	2	B	19	4	8
HE minus	4	13-14	23f	18	3	2	3	4	2	15	8	7	2	B	19	4	8
HE minus	4	13-14	27r	5	3	2	4	4	2	15	8	7	0	B	19	4	8
HE minus	4	13-14	23r	14	3	2	5	4	2	15	8	7	1	B	19	4	8
HE minus	4	13	19r	17	3	3	0	5	2	15	8	6	0	T	19	4	8
HE minus	4	13	20f	9	3	3	1	5	2	15	8	6	1	T	19	4	8
HE minus	4	13-14	21r	1	3	3	2	5	2	15	8	6	2	T	19	4	8
HE minus	4	13	21f	4	3	3	3	6	2	15	8	7	2	T	19	4	8
HE minus	4	13	19f	13	3	3	4	6	2	15	8	7	0	T	19	4	8
HE minus	4	13-14	20r	8	3	3	5	6	2	15	8	7	1	T	19	4	8
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	4	14	17	12	4	1	0	1	2	14	7	6	0	B	19	4	7
HE minus	4	14	16	7	4	1	1	1	2	14	7	6	1	B	19	4	7
HE minus	4	13-14	26f	16	4	1	2	1	2	14	7	6	2	B	19	4	7
HE minus	4	13-14	26r	19	4	1	3	2	2	14	7	7	2	B	19	4	7
HE minus	4	14	18f	11	4	1	4	2	2	14	7	7	0	B	19	4	7
HE minus	4	14	18r	3	4	1	5	2	2	14	7	7	1	B	19	4	7
HE minus	4	13-14	28f	6	4	2	0	3	2	15	8	2	0	B	19	4	8
HE minus	4	13-14	28m	18	4	2	1	3	2	15	8	2	1	B	19	4	8
HE minus	4	13-14	29f	15	4	2	2	3	2	15	8	2	2	B	19	4	8
HE minus	4	13-14	28r	14	4	2	3	4	2	15	8	3	2	B	19	4	8
HE minus	4	13-14	24r	5	4	2	4	4	2	15	8	3	0	B	19	4	8
HE minus	4	13-14	24f	2	4	2	5	4	2	15	8	3	1	B	19	4	8
HE minus	4	14	19r	1	4	3	0	5	2	15	8	4	0	T	19	4	8
HE minus	4	14	20f	9	4	3	1	5	2	15	8	4	1	T	19	4	8
HE minus	4	13-14	22r	17	4	3	2	5	2	15	8	4	2	T	19	4	8
HE minus	4	14	19f	4	4	3	3	6	2	15	8	5	2	T	19	4	8
HE minus	4	14	20r	8	4	3	4	6	2	15	8	5	0	T	19	4	8
HE minus	4	13-14	22f	13	4	3	5	6	2	15	8	5	1	T	19	4	8
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB plus	4	11	16r	2	4	1	0	1	2	17	10	0	0	T	19	4	10

HB plus	4	11	15r	7	4	1	1	1	2	17	10	0	1	T	19	4	10
HB plus	4	11	14	6	4	1	2	1	2	17	10	0	2	T	19	4	10
HB plus	4	11	16f	3	4	1	3	2	2	17	10	1	2	T	19	4	10
HB plus	4	11	15f	1	4	1	4	2	2	17	10	1	0	T	19	4	10
HB plus	4	11	13	5	4	1	5	2	2	17	10	1	1	T	19	4	10
HB plus	4	11	10	11	4	2	0	3	2	16	9	1	0	T	19	4	9
HB plus	4	11	6	15	4	2	1	3	2	16	9	1	1	T	19	4	9
HB plus	4	11	2	18	4	2	2	3	2	16	9	1	2	T	19	4	9
HB plus	4	11	12	4	4	2	3	4	2	16	9	0	2	B	19	4	9
HB plus	4	11	8	8	4	2	4	4	2	16	9	0	0	B	19	4	9
HB plus	4	11	4	13	4	2	5	4	2	16	9	0	1	B	19	4	9
HB plus	4	11	11	12	4	3	0	5	2	16	9	1	0	B	19	4	9
HB plus	4	11	7	16	4	3	1	5	2	16	9	1	1	B	19	4	9
HB plus	4	11	3	19	4	3	2	5	2	16	9	1	2	B	19	4	9
HB plus	4	11	9	9	4	3	3	6	2	16	9	0	2	T	19	4	9
HB plus	4	11	5	14	4	3	4	6	2	16	9	0	0	T	19	4	9
HB plus	4	11	1	17	4	3	5	6	2	16	9	0	1	T	19	4	9
Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB plus	4	12	16r	3	3	1	0	1	2	17	10	2	0	T	19	4	10
HB plus	4	12	15r	17	3	1	1	1	2	17	10	2	1	T	19	4	10
HB plus	4	12	14	19	3	1	2	1	2	17	10	2	2	T	19	4	10
HB plus	4	12	16f	1	3	1	3	2	2	17	10	3	2	T	19	4	10
HB plus	4	12	15f	18	3	1	4	2	2	17	10	3	0	T	19	4	10
HB plus	4	12	13	13	3	1	5	2	2	17	10	3	1	T	19	4	10
HB plus	4	12	10	16	3	2	0	3	2	16	9	3	0	T	19	4	9
HB plus	4	12	6	12	3	2	1	3	2	16	9	3	1	T	19	4	9
HB plus	4	12	2	7	3	2	2	3	2	16	9	3	2	T	19	4	9
HB plus	4	12	12	14	3	2	3	4	2	16	9	2	2	B	19	4	9
HB plus	4	12	8	9	3	2	4	4	2	16	9	2	0	B	19	4	9
HB plus	4	12	4	5	3	2	5	4	2	16	9	2	1	B	19	4	9
HB plus	4	12	11	15	3	3	0	5	2	16	9	3	0	B	19	4	9
HB plus	4	12	7	11	3	3	1	5	2	16	9	3	1	B	19	4	9
HB plus	4	12	3	6	3	3	2	5	2	16	9	3	2	B	19	4	9
HB plus	4	12	9	8	3	3	3	6	2	16	9	2	2	T	19	4	9
HB plus	4	12	5	4	3	3	4	6	2	16	9	2	0	T	19	4	9
HB plus	4	12	1	2	3	3	5	6	2	16	9	2	1	T	19	4	9
Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB plus	4	13	16r	17	2	1	0	1	2	17	10	0	0	B	19	4	10
HB plus	4	13	15r	3	2	1	1	1	2	17	10	0	1	B	19	4	10
HB plus	4	13	14	1	2	1	2	1	2	17	10	0	2	B	19	4	10
HB plus	4	13	16f	19	2	1	3	2	2	17	10	1	2	B	19	4	10
HB plus	4	13	15f	2	2	1	4	2	2	17	10	1	0	B	19	4	10
HB plus	4	13	13	7	2	1	5	2	2	17	10	1	1	B	19	4	10
HB plus	4	13	10	4	2	2	0	3	2	16	9	5	0	T	19	4	9
HB plus	4	13	6	8	2	2	1	3	2	16	9	5	1	T	19	4	9
HB plus	4	13	2	13	2	2	2	3	2	16	9	5	2	T	19	4	9
HB plus	4	13	12	6	2	2	3	4	2	16	9	4	2	B	19	4	9
HB plus	4	13	8	11	2	2	4	4	2	16	9	4	0	B	19	4	9
HB plus	4	13	4	15	2	2	5	4	2	16	9	4	1	B	19	4	9
HB plus	4	13	11	5	2	3	0	5	2	16	9	5	0	B	19	4	9
HB plus	4	13	7	9	2	3	1	5	2	16	9	5	1	B	19	4	9

HB plus	4	13	3	14	2	3	2	5	2	16	9	5	2	B	19	4	9
HB plus	4	13	9	12	2	3	3	6	2	16	9	4	2	T	19	4	9
HB plus	4	13	5	16	2	3	4	6	2	16	9	4	0	T	19	4	9
HB plus	4	13	1	18	2	3	5	6	2	16	9	4	1	T	19	4	9
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB plus	4	14	16r	18	1	1	0	1	2	17	10	2	0	B	19	4	10
HB plus	4	14	15r	13	1	1	1	1	2	17	10	2	1	B	19	4	10
HB plus	4	14	14	14	1	1	2	1	2	17	10	2	2	B	19	4	10
HB plus	4	14	16f	17	1	1	3	2	2	17	10	3	2	B	19	4	10
HB plus	4	14	15f	19	1	1	4	2	2	17	10	3	0	B	19	4	10
HB plus	4	14	13	15	1	1	5	2	2	17	10	3	1	B	19	4	10
HB plus	4	14	10	9	1	2	0	3	2	16	9	7	0	T	19	4	9
HB plus	4	14	6	5	1	2	1	3	2	16	9	7	1	T	19	4	9
HB plus	4	14	2	2	1	2	2	3	2	16	9	7	2	T	19	4	9
HB plus	4	14	12	16	1	2	3	4	2	16	9	6	2	B	19	4	9
HB plus	4	14	8	12	1	2	4	4	2	16	9	6	0	B	19	4	9
HB plus	4	14	4	7	1	2	5	4	2	16	9	6	1	B	19	4	9
HB plus	4	14	11	8	1	3	0	5	2	16	9	7	0	B	19	4	9
HB plus	4	14	7	4	1	3	1	5	2	16	9	7	1	B	19	4	9
HB plus	4	14	3	1	1	3	2	5	2	16	9	7	2	B	19	4	9
HB plus	4	14	9	11	1	3	3	6	2	16	9	6	2	T	19	4	9
HB plus	4	14	5	6	1	3	4	6	2	16	9	6	0	T	19	4	9
HB plus	4	14	1	3	1	3	5	6	2	16	9	6	1	T	19	4	9
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	4	11	17	12	4	1	0	1	2	17	10	4	0	T	19	4	10
HE plus	4	11	16	7	4	1	1	1	2	17	10	4	1	T	19	4	10
HE plus	4	11-12	26f	16	4	1	2	1	2	17	10	4	2	T	19	4	10
HE plus	4	11-12	26r	19	4	1	3	2	2	17	10	5	2	T	19	4	10
HE plus	4	11	18f	11	4	1	4	2	2	17	10	5	0	T	19	4	10
HE plus	4	11	18r	3	4	1	5	2	2	17	10	5	1	T	19	4	10
HE plus	4	11-12	28f	6	4	2	0	3	2	18	11	0	0	B	19	4	11
HE plus	4	11-12	28m	18	4	2	1	3	2	18	11	0	1	B	19	4	11
HE plus	4	11-12	29f	15	4	2	2	3	2	18	11	0	2	B	19	4	11
HE plus	4	11-12	28r	14	4	2	3	4	2	18	11	1	2	B	19	4	11
HE plus	4	11-12	24r	5	4	2	4	4	2	18	11	1	0	B	19	4	11
HE plus	4	11-12	24f	2	4	2	5	4	2	18	11	1	1	B	19	4	11
HE plus	4	11	19r	1	4	3	0	5	2	18	11	0	0	T	19	4	11
HE plus	4	11	20f	9	4	3	1	5	2	18	11	0	1	T	19	4	11
HE plus	4	11-12	22r	17	4	3	2	5	2	18	11	0	2	T	19	4	11
HE plus	4	11	19f	4	4	3	3	6	2	18	11	1	2	T	19	4	11
HE plus	4	11	20r	8	4	3	4	6	2	18	11	1	0	T	19	4	11
HE plus	4	11-12	22f	13	4	3	5	6	2	18	11	1	1	T	19	4	11
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	4	12	17	12	3	1	0	1	2	17	10	6	0	T	19	4	10
HE plus	4	12	16	16	3	1	1	1	2	17	10	6	1	T	19	4	10
HE plus	4	11-12	25f	7	3	1	2	1	2	17	10	6	2	T	19	4	10
HE plus	4	11-12	25r	3	3	1	3	2	2	17	10	7	2	T	19	4	10
HE plus	4	12	18f	11	3	1	4	2	2	17	10	7	0	T	19	4	10
HE plus	4	12	18r	19	3	1	5	2	2	17	10	7	1	T	19	4	10
HE plus	4	11-12	27f	6	3	2	0	3	2	18	11	4	0	B	19	4	11
HE plus	4	11-12	27m	2	3	2	1	3	2	18	11	4	1	B	19	4	11

HE plus	4	11-12	29m	15	3	2	2	3	2	18	11	4	2	B	19	4	11
HE plus	4	11-12	23f	18	3	2	3	4	2	18	11	5	2	B	19	4	11
HE plus	4	11-12	27r	5	3	2	4	4	2	18	11	5	0	B	19	4	11
HE plus	4	11-12	23r	14	3	2	5	4	2	18	11	5	1	B	19	4	11
HE plus	4	12	19r	17	3	3	0	5	2	18	11	2	0	T	19	4	11
HE plus	4	12	20f	9	3	3	1	5	2	18	11	2	1	T	19	4	11
HE plus	4	11-12	21r	1	3	3	2	5	2	18	11	2	2	T	19	4	11
HE plus	4	12	21f	4	3	3	3	6	2	18	11	3	2	T	19	4	11
HE plus	4	12	19f	13	3	3	4	6	2	18	11	3	0	T	19	4	11
HE plus	4	11-12	20r	8	3	3	5	6	2	18	11	3	1	T	19	4	11
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	4	13	17	12	2	1	0	1	2	17	10	4	0	B	19	4	10
HE plus	4	13	16	7	2	1	1	1	2	17	10	4	1	B	19	4	10
HE plus	4	13-14	25f	16	2	1	2	1	2	17	10	4	2	B	19	4	10
HE plus	4	13-14	25r	19	2	1	3	2	2	17	10	5	2	B	19	4	10
HE plus	4	13	18f	11	2	1	4	2	2	17	10	5	0	B	19	4	10
HE plus	4	13	18r	3	2	1	5	2	2	17	10	5	1	B	19	4	10
HE plus	4	13-14	27f	15	2	2	0	3	2	18	11	6	0	B	19	4	11
HE plus	4	13-14	27m	18	2	2	1	3	2	18	11	6	1	B	19	4	11
HE plus	4	13-14	29m	6	2	2	2	3	2	18	11	6	2	B	19	4	11
HE plus	4	13-14	23f	2	2	2	3	4	2	18	11	7	2	B	19	4	11
HE plus	4	13-14	27r	14	2	2	4	4	2	18	11	7	0	B	19	4	11
HE plus	4	13-14	23r	5	2	2	5	4	2	18	11	7	1	B	19	4	11
HE plus	4	13	19r	1	2	3	0	5	2	18	11	6	0	T	19	4	11
HE plus	4	13	20f	9	2	3	1	5	2	18	11	6	1	T	19	4	11
HE plus	4	13-14	21r	17	2	3	2	5	2	18	11	6	2	T	19	4	11
HE plus	4	13	21f	13	2	3	3	6	2	18	11	7	2	T	19	4	11
HE plus	4	13	19f	4	2	3	4	6	2	18	11	7	0	T	19	4	11
HE plus	4	13-14	20r	8	2	3	5	6	2	18	11	7	1	T	19	4	11
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	4	14	17	12	1	1	0	1	2	17	10	6	0	B	19	4	10
HE plus	4	14	16	16	1	1	1	1	2	17	10	6	1	B	19	4	10
HE plus	4	13-14	26f	7	1	1	2	1	2	17	10	6	2	B	19	4	10
HE plus	4	13-14	26r	3	1	1	3	2	2	17	10	7	2	B	19	4	10
HE plus	4	14	18f	11	1	1	4	2	2	17	10	7	0	B	19	4	10
HE plus	4	14	18r	19	1	1	5	2	2	17	10	7	1	B	19	4	10
HE plus	4	13-14	28f	15	1	2	0	3	2	18	11	2	0	B	19	4	11
HE plus	4	13-14	28m	2	1	2	1	3	2	18	11	2	1	B	19	4	11
HE plus	4	13-14	29f	6	1	2	2	3	2	18	11	2	2	B	19	4	11
HE plus	4	13-14	28r	5	1	2	3	4	2	18	11	3	2	B	19	4	11
HE plus	4	13-14	24r	14	1	2	4	4	2	18	11	3	0	B	19	4	11
HE plus	4	13-14	24f	18	1	2	5	4	2	18	11	3	1	B	19	4	11
HE plus	4	14	19r	17	1	3	0	5	2	18	11	4	0	T	19	4	11
HE plus	4	14	20f	9	1	3	1	5	2	18	11	4	1	T	19	4	11
HE plus	4	13-14	22r	4	1	3	2	5	2	18	11	4	2	T	19	4	11
HE plus	4	14	19f	13	1	3	3	6	2	18	11	5	2	T	19	4	11
HE plus	4	14	20r	8	1	3	4	6	2	18	11	5	0	T	19	4	11
HE plus	4	13-14	22f	1	1	3	5	6	2	18	11	5	1	T	19	4	11
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	