

Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB minus	5	15	16r	18	1	1	0	1	3	3	1	0	0	T	9	5	1
HB minus	5	15	15r	13	1	1	1	1	3	3	1	0	1	T	9	5	1
HB minus	5	15	14	14	1	1	2	1	3	3	1	0	2	T	9	5	1
HB minus	5	15	16f	17	1	1	3	2	3	3	1	1	2	T	9	5	1
HB minus	5	15	15f	19	1	1	4	2	3	3	1	1	0	T	9	5	1
HB minus	5	15	13	15	1	1	5	2	3	3	1	1	1	T	9	5	1
HB minus	5	15	10	9	1	2	0	3	3	2	0	1	0	T	9	5	0
HB minus	5	15	6	5	1	2	1	3	3	2	0	1	1	T	9	5	0
HB minus	5	15	2	2	1	2	2	3	3	2	0	1	2	T	9	5	0
HB minus	5	15	12	16	1	2	3	4	3	2	0	0	2	B	9	5	0
HB minus	5	15	8	12	1	2	4	4	3	2	0	0	0	B	9	5	0
HB minus	5	15	4	7	1	2	5	4	3	2	0	0	1	B	9	5	0
HB minus	5	15	11	8	1	3	0	5	3	2	0	1	0	B	9	5	0
HB minus	5	15	7	4	1	3	1	5	3	2	0	1	1	B	9	5	0
HB minus	5	15	3	1	1	3	2	5	3	2	0	1	2	B	9	5	0
HB minus	5	15	9	11	1	3	3	6	3	2	0	0	2	T	9	5	0
HB minus	5	15	5	6	1	3	4	6	3	2	0	0	0	T	9	5	0
HB minus	5	15	1	3	1	3	5	6	3	2	0	0	1	T	9	5	0
Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB minus	5	16	16r	17	2	1	0	1	3	3	1	2	0	T	9	5	1
HB minus	5	16	15r	3	2	1	1	1	3	3	1	2	1	T	9	5	1
HB minus	5	16	14	1	2	1	2	1	3	3	1	2	2	T	9	5	1
HB minus	5	16	16f	19	2	1	3	2	3	3	1	3	2	T	9	5	1
HB minus	5	16	15f	2	2	1	4	2	3	3	1	3	0	T	9	5	1
HB minus	5	16	13	7	2	1	5	2	3	3	1	3	1	T	9	5	1
HB minus	5	16	10	4	2	2	0	3	3	2	0	3	0	T	9	5	0
HB minus	5	16	6	8	2	2	1	3	3	2	0	3	1	T	9	5	0
HB minus	5	16	2	13	2	2	2	3	3	2	0	3	2	T	9	5	0
HB minus	5	16	12	6	2	2	3	4	3	2	0	2	2	B	9	5	0
HB minus	5	16	8	11	2	2	4	4	3	2	0	2	0	B	9	5	0
HB minus	5	16	4	15	2	2	5	4	3	2	0	2	1	B	9	5	0
HB minus	5	16	11	5	2	3	0	5	3	2	0	3	0	B	9	5	0
HB minus	5	16	7	9	2	3	1	5	3	2	0	3	1	B	9	5	0
HB minus	5	16	3	14	2	3	2	5	3	2	0	3	2	B	9	5	0
HB minus	5	16	9	12	2	3	3	6	3	2	0	2	2	T	9	5	0
HB minus	5	16	5	16	2	3	4	6	3	2	0	2	0	T	9	5	0
HB minus	5	16	1	18	2	3	5	6	3	2	0	2	1	T	9	5	0
Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB minus	5	17	16r	3	3	1	0	1	3	3	1	0	0	B	9	5	1
HB minus	5	17	15r	17	3	1	1	1	3	3	1	0	1	B	9	5	1
HB minus	5	17	14	19	3	1	2	1	3	3	1	0	2	B	9	5	1
HB minus	5	17	16f	1	3	1	3	2	3	3	1	1	2	B	9	5	1
HB minus	5	17	15f	18	3	1	4	2	3	3	1	1	0	B	9	5	1
HB minus	5	17	13	13	3	1	5	2	3	3	1	1	1	B	9	5	1
HB minus	5	17	10	16	3	2	0	3	3	2	0	5	0	T	9	5	0
HB minus	5	17	6	12	3	2	1	3	3	2	0	5	1	T	9	5	0
HB minus	5	17	2	7	3	2	2	3	3	2	0	5	2	T	9	5	0
HB minus	5	17	12	14	3	2	3	4	3	2	0	4	2	B	9	5	0
HB minus	5	17	8	9	3	2	4	4	3	2	0	4	0	B	9	5	0

HB minus	5	17	4	5	3	2	5	4	3	2	0	4	1	B	9	5	0
HB minus	5	17	11	15	3	3	0	5	3	2	0	5	0	B	9	5	0
HB minus	5	17	7	11	3	3	1	5	3	2	0	5	1	B	9	5	0
HB minus	5	17	3	6	3	3	2	5	3	2	0	5	2	B	9	5	0
HB minus	5	17	9	8	3	3	3	6	3	2	0	4	2	T	9	5	0
HB minus	5	17	5	4	3	3	4	6	3	2	0	4	0	T	9	5	0
HB minus	5	17	1	2	3	3	5	6	3	2	0	4	1	T	9	5	0
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB minus	5	18	16r	2	4	1	0	1	3	3	1	2	0	B	9	5	1
HB minus	5	18	15r	7	4	1	1	1	3	3	1	2	1	B	9	5	1
HB minus	5	18	14	6	4	1	2	1	3	3	1	2	2	B	9	5	1
HB minus	5	18	16f	3	4	1	3	2	3	3	1	3	2	B	9	5	1
HB minus	5	18	15f	1	4	1	4	2	3	3	1	3	0	B	9	5	1
HB minus	5	18	13	5	4	1	5	2	3	3	1	3	1	B	9	5	1
HB minus	5	18	10	11	4	2	0	3	3	2	0	7	0	T	9	5	0
HB minus	5	18	6	15	4	2	1	3	3	2	0	7	1	T	9	5	0
HB minus	5	18	2	18	4	2	2	3	3	2	0	7	2	T	9	5	0
HB minus	5	18	12	4	4	2	3	4	3	2	0	6	2	B	9	5	0
HB minus	5	18	8	8	4	2	4	4	3	2	0	6	0	B	9	5	0
HB minus	5	18	4	13	4	2	5	4	3	2	0	6	1	B	9	5	0
HB minus	5	18	11	12	4	3	0	5	3	2	0	7	0	B	9	5	0
HB minus	5	18	7	16	4	3	1	5	3	2	0	7	1	B	9	5	0
HB minus	5	18	3	19	4	3	2	5	3	2	0	7	2	B	9	5	0
HB minus	5	18	9	9	4	3	3	6	3	2	0	6	2	T	9	5	0
HB minus	5	18	5	14	4	3	4	6	3	2	0	6	0	T	9	5	0
HB minus	5	18	1	17	4	3	5	6	3	2	0	6	1	T	9	5	0
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	5	15	17	12	1	1	0	1	3	3	1	4	0	T	9	5	1
HE minus	5	15	16	16	1	1	1	1	3	3	1	4	1	T	9	5	1
HE minus	5	15-16	26f	7	1	1	2	1	3	3	1	4	2	T	9	5	1
HE minus	5	15-16	26r	3	1	1	3	2	3	3	1	5	2	T	9	5	1
HE minus	5	15	18f	11	1	1	4	2	3	3	1	5	0	T	9	5	1
HE minus	5	15	18r	19	1	1	5	2	3	3	1	5	1	T	9	5	1
HE minus	5	15-16	28f	15	1	2	0	3	3	4	2	0	0	B	9	5	2
HE minus	5	15-16	28m	2	1	2	1	3	3	4	2	0	1	B	9	5	2
HE minus	5	15-16	29f	6	1	2	2	3	3	4	2	0	2	B	9	5	2
HE minus	5	15-16	28r	5	1	2	3	4	3	4	2	1	2	B	9	5	2
HE minus	5	15-16	24r	14	1	2	4	4	3	4	2	1	0	B	9	5	2
HE minus	5	15-16	24f	18	1	2	5	4	3	4	2	1	1	B	9	5	2
HE minus	5	15	19r	17	1	3	0	5	3	4	2	0	0	T	9	5	2
HE minus	5	15	20f	9	1	3	1	5	3	4	2	0	1	T	9	5	2
HE minus	5	15-16	22r	4	1	3	2	5	3	4	2	0	2	T	9	5	2
HE minus	5	15	19f	13	1	3	3	6	3	4	2	1	2	T	9	5	2
HE minus	5	15	20r	8	1	3	4	6	3	4	2	1	0	T	9	5	2
HE minus	5	15-16	22f	1	1	3	5	6	3	4	2	1	1	T	9	5	2
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	5	16	17	12	2	1	0	1	3	3	1	6	0	T	9	5	1
HE minus	5	16	16	7	2	1	1	1	3	3	1	6	1	T	9	5	1
HE minus	5	15-16	25f	16	2	1	2	1	3	3	1	6	2	T	9	5	1
HE minus	5	15-16	25r	19	2	1	3	2	3	3	1	7	2	T	9	5	1
HE minus	5	16	18f	11	2	1	4	2	3	3	1	7	0	T	9	5	1

HE minus	5	16	18r	3	2	1	5	2	3	3	1	7	1	T	9	5	1
HE minus	5	15-16	27f	15	2	2	0	3	3	4	2	4	0	B	9	5	2
HE minus	5	15-16	27m	18	2	2	1	3	3	4	2	4	1	B	9	5	2
HE minus	5	15-16	29m	6	2	2	2	3	3	4	2	4	2	B	9	5	2
HE minus	5	15-16	23f	2	2	2	3	4	3	4	2	5	2	B	9	5	2
HE minus	5	15-16	27r	14	2	2	4	4	3	4	2	5	0	B	9	5	2
HE minus	5	15-16	23r	5	2	2	5	4	3	4	2	5	1	B	9	5	2
HE minus	5	16	19r	1	2	3	0	5	3	4	2	2	0	T	9	5	2
HE minus	5	16	20f	9	2	3	1	5	3	4	2	2	1	T	9	5	2
HE minus	5	15-16	21r	17	2	3	2	5	3	4	2	2	2	T	9	5	2
HE minus	5	16	21f	13	2	3	3	6	3	4	2	3	2	T	9	5	2
HE minus	5	16	19f	4	2	3	4	6	3	4	2	3	0	T	9	5	2
HE minus	5	15-16	20r	8	2	3	5	6	3	4	2	3	1	T	9	5	2
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	5	17	17	12	3	1	0	1	3	3	1	4	0	B	9	5	1
HE minus	5	17	16	16	3	1	1	1	3	3	1	4	1	B	9	5	1
HE minus	5	17-18	25f	7	3	1	2	1	3	3	1	4	2	B	9	5	1
HE minus	5	17-18	25r	3	3	1	3	2	3	3	1	5	2	B	9	5	1
HE minus	5	17	18f	11	3	1	4	2	3	3	1	5	0	B	9	5	1
HE minus	5	17	18r	19	3	1	5	2	3	3	1	5	1	B	9	5	1
HE minus	5	17-18	27f	6	3	2	0	3	3	4	2	6	0	B	9	5	2
HE minus	5	17-18	27m	2	3	2	1	3	3	4	2	6	1	B	9	5	2
HE minus	5	17-18	29m	15	3	2	2	3	3	4	2	6	2	B	9	5	2
HE minus	5	17-18	23f	18	3	2	3	4	3	4	2	7	2	B	9	5	2
HE minus	5	17-18	27r	5	3	2	4	4	3	4	2	7	0	B	9	5	2
HE minus	5	17-18	23r	14	3	2	5	4	3	4	2	7	1	B	9	5	2
HE minus	5	17	19r	17	3	3	0	5	3	4	2	6	0	T	9	5	2
HE minus	5	17	20f	9	3	3	1	5	3	4	2	6	1	T	9	5	2
HE minus	5	17-18	21r	1	3	3	2	5	3	4	2	6	2	T	9	5	2
HE minus	5	17	21f	4	3	3	3	6	3	4	2	7	2	T	9	5	2
HE minus	5	17	19f	13	3	3	4	6	3	4	2	7	0	T	9	5	2
HE minus	5	17-18	20r	8	3	3	5	6	3	4	2	7	1	T	9	5	2
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	5	18	17	12	4	1	0	1	3	3	1	6	0	B	9	5	1
HE minus	5	18	16	7	4	1	1	1	3	3	1	6	1	B	9	5	1
HE minus	5	17-18	26f	16	4	1	2	1	3	3	1	6	2	B	9	5	1
HE minus	5	17-18	26r	19	4	1	3	2	3	3	1	7	2	B	9	5	1
HE minus	5	18	18f	11	4	1	4	2	3	3	1	7	0	B	9	5	1
HE minus	5	18	18r	3	4	1	5	2	3	3	1	7	1	B	9	5	1
HE minus	5	17-18	28f	6	4	2	0	3	3	4	2	2	0	B	9	5	2
HE minus	5	17-18	28m	18	4	2	1	3	3	4	2	2	1	B	9	5	2
HE minus	5	17-18	29f	15	4	2	2	3	3	4	2	2	2	B	9	5	2
HE minus	5	17-18	28r	14	4	2	3	4	3	4	2	3	2	B	9	5	2
HE minus	5	17-18	24r	5	4	2	4	4	3	4	2	3	0	B	9	5	2
HE minus	5	17-18	24f	2	4	2	5	4	3	4	2	3	1	B	9	5	2
HE minus	5	18	19r	1	4	3	0	5	3	4	2	4	0	T	9	5	2
HE minus	5	18	20f	9	4	3	1	5	3	4	2	4	1	T	9	5	2
HE minus	5	17-18	22r	17	4	3	2	5	3	4	2	4	2	T	9	5	2
HE minus	5	18	19f	4	4	3	3	6	3	4	2	5	2	T	9	5	2
HE minus	5	18	20r	8	4	3	4	6	3	4	2	5	0	T	9	5	2
HE minus	5	17-18	22f	13	4	3	5	6	3	4	2	5	1	T	9	5	2

Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB plus	5	15	16r	2	4	1	0	1	3	6	4	0	0	T	9	5	4
HB plus	5	15	15r	7	4	1	1	1	3	6	4	0	1	T	9	5	4
HB plus	5	15	14	6	4	1	2	1	3	6	4	0	2	T	9	5	4
HB plus	5	15	16f	3	4	1	3	2	3	6	4	1	2	T	9	5	4
HB plus	5	15	15f	1	4	1	4	2	3	6	4	1	0	T	9	5	4
HB plus	5	15	13	5	4	1	5	2	3	6	4	1	1	T	9	5	4
HB plus	5	15	10	11	4	2	0	3	3	5	3	1	0	T	9	5	3
HB plus	5	15	6	15	4	2	1	3	3	5	3	1	1	T	9	5	3
HB plus	5	15	2	18	4	2	2	3	3	5	3	1	2	T	9	5	3
HB plus	5	15	12	4	4	2	3	4	3	5	3	0	2	B	9	5	3
HB plus	5	15	8	8	4	2	4	4	3	5	3	0	0	B	9	5	3
HB plus	5	15	4	13	4	2	5	4	3	5	3	0	1	B	9	5	3
HB plus	5	15	11	12	4	3	0	5	3	5	3	1	0	B	9	5	3
HB plus	5	15	7	16	4	3	1	5	3	5	3	1	1	B	9	5	3
HB plus	5	15	3	19	4	3	2	5	3	5	3	1	2	B	9	5	3
HB plus	5	15	9	9	4	3	3	6	3	5	3	0	2	T	9	5	3
HB plus	5	15	5	14	4	3	4	6	3	5	3	0	0	T	9	5	3
HB plus	5	15	1	17	4	3	5	6	3	5	3	0	1	T	9	5	3
Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB plus	5	16	16r	3	3	1	0	1	3	6	4	2	0	T	9	5	4
HB plus	5	16	15r	17	3	1	1	1	3	6	4	2	1	T	9	5	4
HB plus	5	16	14	19	3	1	2	1	3	6	4	2	2	T	9	5	4
HB plus	5	16	16f	1	3	1	3	2	3	6	4	3	2	T	9	5	4
HB plus	5	16	15f	18	3	1	4	2	3	6	4	3	0	T	9	5	4
HB plus	5	16	13	13	3	1	5	2	3	6	4	3	1	T	9	5	4
HB plus	5	16	10	16	3	2	0	3	3	5	3	3	0	T	9	5	3
HB plus	5	16	6	12	3	2	1	3	3	5	3	3	1	T	9	5	3
HB plus	5	16	2	7	3	2	2	3	3	5	3	3	2	T	9	5	3
HB plus	5	16	12	14	3	2	3	4	3	5	3	2	2	B	9	5	3
HB plus	5	16	8	9	3	2	4	4	3	5	3	2	0	B	9	5	3
HB plus	5	16	4	5	3	2	5	4	3	5	3	2	1	B	9	5	3
HB plus	5	16	11	15	3	3	0	5	3	5	3	3	0	B	9	5	3
HB plus	5	16	7	11	3	3	1	5	3	5	3	3	1	B	9	5	3
HB plus	5	16	3	6	3	3	2	5	3	5	3	3	2	B	9	5	3
HB plus	5	16	9	8	3	3	3	6	3	5	3	2	2	T	9	5	3
HB plus	5	16	5	4	3	3	4	6	3	5	3	2	0	T	9	5	3
HB plus	5	16	1	2	3	3	5	6	3	5	3	2	1	T	9	5	3
Det	W	Phi	tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch
HB plus	5	17	16r	17	2	1	0	1	3	6	4	0	0	B	9	5	4
HB plus	5	17	15r	3	2	1	1	1	3	6	4	0	1	B	9	5	4
HB plus	5	17	14	1	2	1	2	1	3	6	4	0	2	B	9	5	4
HB plus	5	17	16f	19	2	1	3	2	3	6	4	1	2	B	9	5	4
HB plus	5	17	15f	2	2	1	4	2	3	6	4	1	0	B	9	5	4
HB plus	5	17	13	7	2	1	5	2	3	6	4	1	1	B	9	5	4
HB plus	5	17	10	4	2	2	0	3	3	5	3	5	0	T	9	5	3
HB plus	5	17	6	8	2	2	1	3	3	5	3	5	1	T	9	5	3
HB plus	5	17	2	13	2	2	2	3	3	5	3	5	2	T	9	5	3
HB plus	5	17	12	6	2	2	3	4	3	5	3	4	2	B	9	5	3
HB plus	5	17	8	11	2	2	4	4	3	5	3	4	0	B	9	5	3
HB plus	5	17	4	15	2	2	5	4	3	5	3	4	1	B	9	5	3

HB plus	5	17	11	5	2	3	0	5	3	5	3	5	0	B	9	5	3
HB plus	5	17	7	9	2	3	1	5	3	5	3	5	1	B	9	5	3
HB plus	5	17	3	14	2	3	2	5	3	5	3	5	2	B	9	5	3
HB plus	5	17	9	12	2	3	3	6	3	5	3	4	2	T	9	5	3
HB plus	5	17	5	16	2	3	4	6	3	5	3	4	0	T	9	5	3
HB plus	5	17	1	18	2	3	5	6	3	5	3	4	1	T	9	5	3
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB plus	5	18	16r	18	1	1	0	1	3	6	4	2	0	B	9	5	4
HB plus	5	18	15r	13	1	1	1	1	3	6	4	2	1	B	9	5	4
HB plus	5	18	14	14	1	1	2	1	3	6	4	2	2	B	9	5	4
HB plus	5	18	16f	17	1	1	3	2	3	6	4	3	2	B	9	5	4
HB plus	5	18	15f	19	1	1	4	2	3	6	4	3	0	B	9	5	4
HB plus	5	18	13	15	1	1	5	2	3	6	4	3	1	B	9	5	4
HB plus	5	18	10	9	1	2	0	3	3	5	3	7	0	T	9	5	3
HB plus	5	18	6	5	1	2	1	3	3	5	3	7	1	T	9	5	3
HB plus	5	18	2	2	1	2	2	3	3	5	3	7	2	T	9	5	3
HB plus	5	18	12	16	1	2	3	4	3	5	3	6	2	B	9	5	3
HB plus	5	18	8	12	1	2	4	4	3	5	3	6	0	B	9	5	3
HB plus	5	18	4	7	1	2	5	4	3	5	3	6	1	B	9	5	3
HB plus	5	18	11	8	1	3	0	5	3	5	3	7	0	B	9	5	3
HB plus	5	18	7	4	1	3	1	5	3	5	3	7	1	B	9	5	3
HB plus	5	18	3	1	1	3	2	5	3	5	3	7	2	B	9	5	3
HB plus	5	18	9	11	1	3	3	6	3	5	3	6	2	T	9	5	3
HB plus	5	18	5	6	1	3	4	6	3	5	3	6	0	T	9	5	3
HB plus	5	18	1	3	1	3	5	6	3	5	3	6	1	T	9	5	3
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	5	15	17	12	4	1	0	1	3	6	4	4	0	T	9	5	4
HE plus	5	15	16	7	4	1	1	1	3	6	4	4	1	T	9	5	4
HE plus	5	15-16	26f	16	4	1	2	1	3	6	4	4	2	T	9	5	4
HE plus	5	15-16	26r	19	4	1	3	2	3	6	4	5	2	T	9	5	4
HE plus	5	15	18f	11	4	1	4	2	3	6	4	5	0	T	9	5	4
HE plus	5	15	18r	3	4	1	5	2	3	6	4	5	1	T	9	5	4
HE plus	5	15-16	28f	6	4	2	0	3	3	7	5	0	0	B	9	5	5
HE plus	5	15-16	28m	18	4	2	1	3	3	7	5	0	1	B	9	5	5
HE plus	5	15-16	29f	15	4	2	2	3	3	7	5	0	2	B	9	5	5
HE plus	5	15-16	28r	14	4	2	3	4	3	7	5	1	2	B	9	5	5
HE plus	5	15-16	24r	5	4	2	4	4	3	7	5	1	0	B	9	5	5
HE plus	5	15-16	24f	2	4	2	5	4	3	7	5	1	1	B	9	5	5
HE plus	5	15	19r	1	4	3	0	5	3	7	5	0	0	T	9	5	5
HE plus	5	15	20f	9	4	3	1	5	3	7	5	0	1	T	9	5	5
HE plus	5	15-16	22r	17	4	3	2	5	3	7	5	0	2	T	9	5	5
HE plus	5	15	19f	4	4	3	3	6	3	7	5	1	2	T	9	5	5
HE plus	5	15	20r	8	4	3	4	6	3	7	5	1	0	T	9	5	5
HE plus	5	15-16	22f	13	4	3	5	6	3	7	5	1	1	T	9	5	5
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	5	16	17	12	3	1	0	1	3	6	4	6	0	T	9	5	4
HE plus	5	16	16	16	3	1	1	1	3	6	4	6	1	T	9	5	4
HE plus	5	15-16	25f	7	3	1	2	1	3	6	4	6	2	T	9	5	4
HE plus	5	15-16	25r	3	3	1	3	2	3	6	4	7	2	T	9	5	4
HE plus	5	16	18f	11	3	1	4	2	3	6	4	7	0	T	9	5	4
HE plus	5	16	18r	19	3	1	5	2	3	6	4	7	1	T	9	5	4

HE plus	5	15-16	27f	6	3	2	0	3	3	7	5	4	0	B	9	5	5
HE plus	5	15-16	27m	2	3	2	1	3	3	7	5	4	1	B	9	5	5
HE plus	5	15-16	29m	15	3	2	2	3	3	7	5	4	2	B	9	5	5
HE plus	5	15-16	23f	18	3	2	3	4	3	7	5	5	2	B	9	5	5
HE plus	5	15-16	27r	5	3	2	4	4	3	7	5	5	0	B	9	5	5
HE plus	5	15-16	23r	14	3	2	5	4	3	7	5	5	1	B	9	5	5
HE plus	5	16	19r	17	3	3	0	5	3	7	5	2	0	T	9	5	5
HE plus	5	16	20f	9	3	3	1	5	3	7	5	2	1	T	9	5	5
HE plus	5	15-16	21r	1	3	3	2	5	3	7	5	2	2	T	9	5	5
HE plus	5	16	21f	4	3	3	3	6	3	7	5	3	2	T	9	5	5
HE plus	5	16	19f	13	3	3	4	6	3	7	5	3	0	T	9	5	5
HE plus	5	15-16	20r	8	3	3	5	6	3	7	5	3	1	T	9	5	5
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	5	17	17	12	2	1	0	1	3	6	4	4	0	B	9	5	4
HE plus	5	17	16	7	2	1	1	1	3	6	4	4	1	B	9	5	4
HE plus	5	17-18	25f	16	2	1	2	1	3	6	4	4	2	B	9	5	4
HE plus	5	17-18	25r	19	2	1	3	2	3	6	4	5	2	B	9	5	4
HE plus	5	17	18f	11	2	1	4	2	3	6	4	5	0	B	9	5	4
HE plus	5	17	18r	3	2	1	5	2	3	6	4	5	1	B	9	5	4
HE plus	5	17-18	27f	15	2	2	0	3	3	7	5	6	0	B	9	5	5
HE plus	5	17-18	27m	18	2	2	1	3	3	7	5	6	1	B	9	5	5
HE plus	5	17-18	29m	6	2	2	2	3	3	7	5	6	2	B	9	5	5
HE plus	5	17-18	23f	2	2	2	3	4	3	7	5	7	2	B	9	5	5
HE plus	5	17-18	27r	14	2	2	4	4	3	7	5	7	0	B	9	5	5
HE plus	5	17-18	23r	5	2	2	5	4	3	7	5	7	1	B	9	5	5
HE plus	5	17	19r	1	2	3	0	5	3	7	5	6	0	T	9	5	5
HE plus	5	17	20f	9	2	3	1	5	3	7	5	6	1	T	9	5	5
HE plus	5	17-18	21r	17	2	3	2	5	3	7	5	6	2	T	9	5	5
HE plus	5	17	21f	13	2	3	3	6	3	7	5	7	2	T	9	5	5
HE plus	5	17	19f	4	2	3	4	6	3	7	5	7	0	T	9	5	5
HE plus	5	17-18	20r	8	2	3	5	6	3	7	5	7	1	T	9	5	5
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	5	18	17	12	1	1	0	1	3	6	4	6	0	B	9	5	4
HE plus	5	18	16	16	1	1	1	1	3	6	4	6	1	B	9	5	4
HE plus	5	17-18	26f	7	1	1	2	1	3	6	4	6	2	B	9	5	4
HE plus	5	17-18	26r	3	1	1	3	2	3	6	4	7	2	B	9	5	4
HE plus	5	18	18f	11	1	1	4	2	3	6	4	7	0	B	9	5	4
HE plus	5	18	18r	19	1	1	5	2	3	6	4	7	1	B	9	5	4
HE plus	5	17-18	28f	15	1	2	0	3	3	7	5	2	0	B	9	5	5
HE plus	5	17-18	28m	2	1	2	1	3	3	7	5	2	1	B	9	5	5
HE plus	5	17-18	29f	6	1	2	2	3	3	7	5	2	2	B	9	5	5
HE plus	5	17-18	28r	5	1	2	3	4	3	7	5	3	2	B	9	5	5
HE plus	5	17-18	24r	14	1	2	4	4	3	7	5	3	0	B	9	5	5
HE plus	5	17-18	24f	18	1	2	5	4	3	7	5	3	1	B	9	5	5
HE plus	5	18	19r	17	1	3	0	5	3	7	5	4	0	T	9	5	5
HE plus	5	18	20f	9	1	3	1	5	3	7	5	4	1	T	9	5	5
HE plus	5	17-18	22r	4	1	3	2	5	3	7	5	4	2	T	9	5	5
HE plus	5	18	19f	13	1	3	3	6	3	7	5	5	2	T	9	5	5
HE plus	5	18	20r	8	1	3	4	6	3	7	5	5	0	T	9	5	5
HE plus	5	17-18	22f	1	1	3	5	6	3	7	5	5	1	T	9	5	5
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	

HB minus	6	19	16r	18	1	1	0	1	3	14	7	0	0	T	19	6	7
HB minus	6	19	15r	13	1	1	1	1	3	14	7	0	1	T	19	6	7
HB minus	6	19	14	14	1	1	2	1	3	14	7	0	2	T	19	6	7
HB minus	6	19	16f	17	1	1	3	2	3	14	7	1	2	T	19	6	7
HB minus	6	19	15f	19	1	1	4	2	3	14	7	1	0	T	19	6	7
HB minus	6	19	13	15	1	1	5	2	3	14	7	1	1	T	19	6	7
HB minus	6	19	10	9	1	2	0	3	3	13	6	1	0	T	19	6	6
HB minus	6	19	6	5	1	2	1	3	3	13	6	1	1	T	19	6	6
HB minus	6	19	2	2	1	2	2	3	3	13	6	1	2	T	19	6	6
HB minus	6	19	12	16	1	2	3	4	3	13	6	0	2	B	19	6	6
HB minus	6	19	8	12	1	2	4	4	3	13	6	0	0	B	19	6	6
HB minus	6	19	4	7	1	2	5	4	3	13	6	0	1	B	19	6	6
HB minus	6	19	11	8	1	3	0	5	3	13	6	1	0	B	19	6	6
HB minus	6	19	7	4	1	3	1	5	3	13	6	1	1	B	19	6	6
HB minus	6	19	3	1	1	3	2	5	3	13	6	1	2	B	19	6	6
HB minus	6	19	9	11	1	3	3	6	3	13	6	0	2	T	19	6	6
HB minus	6	19	5	6	1	3	4	6	3	13	6	0	0	T	19	6	6
HB minus	6	19	1	3	1	3	5	6	3	13	6	0	1	T	19	6	6
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB minus	6	20	16r	17	2	1	0	1	3	14	7	2	0	T	19	6	7
HB minus	6	20	15r	3	2	1	1	1	3	14	7	2	1	T	19	6	7
HB minus	6	20	14	1	2	1	2	1	3	14	7	2	2	T	19	6	7
HB minus	6	20	16f	19	2	1	3	2	3	14	7	3	2	T	19	6	7
HB minus	6	20	15f	2	2	1	4	2	3	14	7	3	0	T	19	6	7
HB minus	6	20	13	7	2	1	5	2	3	14	7	3	1	T	19	6	7
HB minus	6	20	10	4	2	2	0	3	3	13	6	3	0	T	19	6	6
HB minus	6	20	6	8	2	2	1	3	3	13	6	3	1	T	19	6	6
HB minus	6	20	2	13	2	2	2	3	3	13	6	3	2	T	19	6	6
HB minus	6	20	12	6	2	2	3	4	3	13	6	2	2	B	19	6	6
HB minus	6	20	8	11	2	2	4	4	3	13	6	2	0	B	19	6	6
HB minus	6	20	4	15	2	2	5	4	3	13	6	2	1	B	19	6	6
HB minus	6	20	11	5	2	3	0	5	3	13	6	3	0	B	19	6	6
HB minus	6	20	7	9	2	3	1	5	3	13	6	3	1	B	19	6	6
HB minus	6	20	3	14	2	3	2	5	3	13	6	3	2	B	19	6	6
HB minus	6	20	9	12	2	3	3	6	3	13	6	2	2	T	19	6	6
HB minus	6	20	5	16	2	3	4	6	3	13	6	2	0	T	19	6	6
HB minus	6	20	1	18	2	3	5	6	3	13	6	2	1	T	19	6	6
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB minus	6	21	16r	3	3	1	0	1	3	14	7	0	0	B	19	6	7
HB minus	6	21	15r	17	3	1	1	1	3	14	7	0	1	B	19	6	7
HB minus	6	21	14	19	3	1	2	1	3	14	7	0	2	B	19	6	7
HB minus	6	21	16f	1	3	1	3	2	3	14	7	1	2	B	19	6	7
HB minus	6	21	15f	18	3	1	4	2	3	14	7	1	0	B	19	6	7
HB minus	6	21	13	13	3	1	5	2	3	14	7	1	1	B	19	6	7
HB minus	6	21	10	16	3	2	0	3	3	13	6	5	0	T	19	6	6
HB minus	6	21	6	12	3	2	1	3	3	13	6	5	1	T	19	6	6
HB minus	6	21	2	7	3	2	2	3	3	13	6	5	2	T	19	6	6
HB minus	6	21	12	14	3	2	3	4	3	13	6	4	2	B	19	6	6
HB minus	6	21	8	9	3	2	4	4	3	13	6	4	0	B	19	6	6
HB minus	6	21	4	5	3	2	5	4	3	13	6	4	1	B	19	6	6
HB minus	6	21	11	15	3	3	0	5	3	13	6	5	0	B	19	6	6

HB minus	6	21	7	11	3	3	1	5	3	13	6	5	1	B	19	6	6
HB minus	6	21	3	6	3	3	2	5	3	13	6	5	2	B	19	6	6
HB minus	6	21	9	8	3	3	3	6	3	13	6	4	2	T	19	6	6
HB minus	6	21	5	4	3	3	4	6	3	13	6	4	0	T	19	6	6
HB minus	6	21	1	2	3	3	5	6	3	13	6	4	1	T	19	6	6
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB minus	6	22	16r	2	4	1	0	1	3	14	7	2	0	B	19	6	7
HB minus	6	22	15r	7	4	1	1	1	3	14	7	2	1	B	19	6	7
HB minus	6	22	14	6	4	1	2	1	3	14	7	2	2	B	19	6	7
HB minus	6	22	16f	3	4	1	3	2	3	14	7	3	2	B	19	6	7
HB minus	6	22	15f	1	4	1	4	2	3	14	7	3	0	B	19	6	7
HB minus	6	22	13	5	4	1	5	2	3	14	7	3	1	B	19	6	7
HB minus	6	22	10	11	4	2	0	3	3	13	6	7	0	T	19	6	6
HB minus	6	22	6	15	4	2	1	3	3	13	6	7	1	T	19	6	6
HB minus	6	22	2	18	4	2	2	3	3	13	6	7	2	T	19	6	6
HB minus	6	22	12	4	4	2	3	4	3	13	6	6	2	B	19	6	6
HB minus	6	22	8	8	4	2	4	4	3	13	6	6	0	B	19	6	6
HB minus	6	22	4	13	4	2	5	4	3	13	6	6	1	B	19	6	6
HB minus	6	22	11	12	4	3	0	5	3	13	6	7	0	B	19	6	6
HB minus	6	22	7	16	4	3	1	5	3	13	6	7	1	B	19	6	6
HB minus	6	22	3	19	4	3	2	5	3	13	6	7	2	B	19	6	6
HB minus	6	22	9	9	4	3	3	6	3	13	6	6	2	T	19	6	6
HB minus	6	22	5	14	4	3	4	6	3	13	6	6	0	T	19	6	6
HB minus	6	22	1	17	4	3	5	6	3	13	6	6	1	T	19	6	6
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	6	19	17	12	1	1	0	1	3	14	7	4	0	T	19	6	7
HE minus	6	19	16	16	1	1	1	1	3	14	7	4	1	T	19	6	7
HE minus	6	19-20	26f	7	1	1	2	1	3	14	7	4	2	T	19	6	7
HE minus	6	19-20	26r	3	1	1	3	2	3	14	7	5	2	T	19	6	7
HE minus	6	19	18f	11	1	1	4	2	3	14	7	5	0	T	19	6	7
HE minus	6	19	18r	19	1	1	5	2	3	14	7	5	1	T	19	6	7
HE minus	6	19-20	28f	15	1	2	0	3	3	15	8	0	0	B	19	6	8
HE minus	6	19-20	28m	2	1	2	1	3	3	15	8	0	1	B	19	6	8
HE minus	6	19-20	29f	6	1	2	2	3	3	15	8	0	2	B	19	6	8
HE minus	6	19-20	28r	5	1	2	3	4	3	15	8	1	2	B	19	6	8
HE minus	6	19-20	24r	14	1	2	4	4	3	15	8	1	0	B	19	6	8
HE minus	6	19-20	24f	18	1	2	5	4	3	15	8	1	1	B	19	6	8
HE minus	6	19	19r	17	1	3	0	5	3	15	8	0	0	T	19	6	8
HE minus	6	19	20f	9	1	3	1	5	3	15	8	0	1	T	19	6	8
HE minus	6	19-20	22r	4	1	3	2	5	3	15	8	0	2	T	19	6	8
HE minus	6	19-20	19f	13	1	3	3	6	3	15	8	1	2	T	19	6	8
HE minus	6	19	20r	8	1	3	4	6	3	15	8	1	0	T	19	6	8
HE minus	6	19-20	22f	1	1	3	5	6	3	15	8	1	1	T	19	6	8
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	6	20	17	12	2	1	0	1	3	14	7	6	0	T	19	6	7
HE minus	6	20	16	7	2	1	1	1	3	14	7	6	1	T	19	6	7
HE minus	6	19-20	25f	16	2	1	2	1	3	14	7	6	2	T	19	6	7
HE minus	6	19-20	25r	19	2	1	3	2	3	14	7	7	2	T	19	6	7
HE minus	6	20	18f	11	2	1	4	2	3	14	7	7	0	T	19	6	7
HE minus	6	20	18r	3	2	1	5	2	3	14	7	7	1	T	19	6	7
HE minus	6	19-20	27f	15	2	2	0	3	3	15	8	4	0	B	19	6	8

HE minus	6	19-20	27m	18	2	2	1	3	3	15	8	4	1	B	19	6	8
HE minus	6	19-20	29m	6	2	2	2	3	3	15	8	4	2	B	19	6	8
HE minus	6	19-20	23f	2	2	2	3	4	3	15	8	5	2	B	19	6	8
HE minus	6	19-20	27r	14	2	2	4	4	3	15	8	5	0	B	19	6	8
HE minus	6	19-20	23r	5	2	2	5	4	3	15	8	5	1	B	19	6	8
HE minus	6	20	19r	1	2	3	0	5	3	15	8	2	0	T	19	6	8
HE minus	6	20	20f	9	2	3	1	5	3	15	8	2	1	T	19	6	8
HE minus	6	19-20	21r	17	2	3	2	5	3	15	8	2	2	T	19	6	8
HE minus	6	19-20	21f	13	2	3	3	6	3	15	8	3	2	T	19	6	8
HE minus	6	20	19f	4	2	3	4	6	3	15	8	3	0	T	19	6	8
HE minus	6	19-29	20r	8	2	3	5	6	3	15	8	3	1	T	19	6	8
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	6	21	17	12	3	1	0	1	3	14	7	4	0	B	19	6	7
HE minus	6	21	16	16	3	1	1	1	3	14	7	4	1	B	19	6	7
HE minus	6	21-22	25f	7	3	1	2	1	3	14	7	4	2	B	19	6	7
HE minus	6	21-22	25r	3	3	1	3	2	3	14	7	5	2	B	19	6	7
HE minus	6	21	18f	11	3	1	4	2	3	14	7	5	0	B	19	6	7
HE minus	6	21	18r	19	3	1	5	2	3	14	7	5	1	B	19	6	7
HE minus	6	21-22	27f	6	3	2	0	3	3	15	8	6	0	B	19	6	8
HE minus	6	21-22	27m	2	3	2	1	3	3	15	8	6	1	B	19	6	8
HE minus	6	21-22	29m	15	3	2	2	3	3	15	8	6	2	B	19	6	8
HE minus	6	21-22	23f	18	3	2	3	4	3	15	8	7	2	B	19	6	8
HE minus	6	21-22	27r	5	3	2	4	4	3	15	8	7	0	B	19	6	8
HE minus	6	21-22	23r	14	3	2	5	4	3	15	8	7	1	B	19	6	8
HE minus	6	21	19r	17	3	3	0	5	3	15	8	6	0	T	19	6	8
HE minus	6	21	20f	9	3	3	1	5	3	15	8	6	1	T	19	6	8
HE minus	6	21-22	21r	1	3	3	2	5	3	15	8	6	2	T	19	6	8
HE minus	6	21	21f	4	3	3	3	6	3	15	8	7	2	T	19	6	8
HE minus	6	21	19f	13	3	3	4	6	3	15	8	7	0	T	19	6	8
HE minus	6	21-22	20r	8	3	3	5	6	3	15	8	7	1	T	19	6	8
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE minus	6	22	17	12	4	1	0	1	3	14	7	6	0	B	19	6	7
HE minus	6	22	16	7	4	1	1	1	3	14	7	6	1	B	19	6	7
HE minus	6	21-22	26f	16	4	1	2	1	3	14	7	6	2	B	19	6	7
HE minus	6	21-22	26r	19	4	1	3	2	3	14	7	7	2	B	19	6	7
HE minus	6	22	18f	11	4	1	4	2	3	14	7	7	0	B	19	6	7
HE minus	6	22	18r	3	4	1	5	2	3	14	7	7	1	B	19	6	7
HE minus	6	21-22	28f	6	4	2	0	3	3	15	8	2	0	B	19	6	8
HE minus	6	21-22	28m	18	4	2	1	3	3	15	8	2	1	B	19	6	8
HE minus	6	21-22	29f	15	4	2	2	3	3	15	8	2	2	B	19	6	8
HE minus	6	21-22	28r	14	4	2	3	4	3	15	8	3	2	B	19	6	8
HE minus	6	21-22	24r	5	4	2	4	4	3	15	8	3	0	B	19	6	8
HE minus	6	21-22	24f	2	4	2	5	4	3	15	8	3	1	B	19	6	8
HE minus	6	22	19r	1	4	3	0	5	3	15	8	4	0	T	19	6	8
HE minus	6	22	20f	9	4	3	1	5	3	15	8	4	1	T	19	6	8
HE minus	6	21-22	22r	17	4	3	2	5	3	15	8	4	2	T	19	6	8
HE minus	6	22	19f	4	4	3	3	6	3	15	8	5	2	T	19	6	8
HE minus	6	22	20r	8	4	3	4	6	3	15	8	5	0	T	19	6	8
HE minus	6	21-22	22f	13	4	3	5	6	3	15	8	5	1	T	19	6	8
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB plus	6	19	16r	2	4	1	0	1	3	17	10	0	0	T	19	6	10

HB plus	6	19	15r	7	4	1	1	1	3	17	10	0	1	T	19	6	10
HB plus	6	19	14	6	4	1	2	1	3	17	10	0	2	T	19	6	10
HB plus	6	19	16f	3	4	1	3	2	3	17	10	1	2	T	19	6	10
HB plus	6	19	15f	1	4	1	4	2	3	17	10	1	0	T	19	6	10
HB plus	6	19	13	5	4	1	5	2	3	17	10	1	1	T	19	6	10
HB plus	6	19	10	11	4	2	0	3	3	16	9	1	0	T	19	6	9
HB plus	6	19	6	15	4	2	1	3	3	16	9	1	1	T	19	6	9
HB plus	6	19	2	18	4	2	2	3	3	16	9	1	2	T	19	6	9
HB plus	6	19	12	4	4	2	3	4	3	16	9	0	2	B	19	6	9
HB plus	6	19	8	8	4	2	4	4	3	16	9	0	0	B	19	6	9
HB plus	6	19	4	13	4	2	5	4	3	16	9	0	1	B	19	6	9
HB plus	6	19	11	12	4	3	0	5	3	16	9	1	0	B	19	6	9
HB plus	6	19	7	16	4	3	1	5	3	16	9	1	1	B	19	6	9
HB plus	6	19	3	19	4	3	2	5	3	16	9	1	2	B	19	6	9
HB plus	6	19	9	9	4	3	3	6	3	16	9	0	2	T	19	6	9
HB plus	6	19	5	14	4	3	4	6	3	16	9	0	0	T	19	6	9
HB plus	6	19	1	17	4	3	5	6	3	16	9	0	1	T	19	6	9
Det	W		Phi tower pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB plus	6	20	16r	3	3	1	0	1	3	17	10	2	0	T	19	6	10
HB plus	6	20	15r	17	3	1	1	1	3	17	10	2	1	T	19	6	10
HB plus	6	20	14	19	3	1	2	1	3	17	10	2	2	T	19	6	10
HB plus	6	20	16f	1	3	1	3	2	3	17	10	3	2	T	19	6	10
HB plus	6	20	15f	18	3	1	4	2	3	17	10	3	0	T	19	6	10
HB plus	6	20	13	13	3	1	5	2	3	17	10	3	1	T	19	6	10
HB plus	6	20	10	16	3	2	0	3	3	16	9	3	0	T	19	6	9
HB plus	6	20	6	12	3	2	1	3	3	16	9	3	1	T	19	6	9
HB plus	6	20	2	7	3	2	2	3	3	16	9	3	2	T	19	6	9
HB plus	6	20	12	14	3	2	3	4	3	16	9	2	2	B	19	6	9
HB plus	6	20	8	9	3	2	4	4	3	16	9	2	0	B	19	6	9
HB plus	6	20	4	5	3	2	5	4	3	16	9	2	1	B	19	6	9
HB plus	6	20	11	15	3	3	0	5	3	16	9	3	0	B	19	6	9
HB plus	6	20	7	11	3	3	1	5	3	16	9	3	1	B	19	6	9
HB plus	6	20	3	6	3	3	2	5	3	16	9	3	2	B	19	6	9
HB plus	6	20	9	8	3	3	3	6	3	16	9	2	2	T	19	6	9
HB plus	6	20	5	4	3	3	4	6	3	16	9	2	0	T	19	6	9
HB plus	6	20	1	2	3	3	5	6	3	16	9	2	1	T	19	6	9
Det	W		Phi tower pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB plus	6	21	16r	17	2	1	0	1	3	17	10	0	0	B	19	6	10
HB plus	6	21	15r	3	2	1	1	1	3	17	10	0	1	B	19	6	10
HB plus	6	21	14	1	2	1	2	1	3	17	10	0	2	B	19	6	10
HB plus	6	21	16f	19	2	1	3	2	3	17	10	1	2	B	19	6	10
HB plus	6	21	15f	2	2	1	4	2	3	17	10	1	0	B	19	6	10
HB plus	6	21	13	7	2	1	5	2	3	17	10	1	1	B	19	6	10
HB plus	6	21	10	4	2	2	0	3	3	16	9	5	0	T	19	6	9
HB plus	6	21	6	8	2	2	1	3	3	16	9	5	1	T	19	6	9
HB plus	6	21	2	13	2	2	2	3	3	16	9	5	2	T	19	6	9
HB plus	6	21	12	6	2	2	3	4	3	16	9	4	2	B	19	6	9
HB plus	6	21	8	11	2	2	4	4	3	16	9	4	0	B	19	6	9
HB plus	6	21	4	15	2	2	5	4	3	16	9	4	1	B	19	6	9
HB plus	6	21	11	5	2	3	0	5	3	16	9	5	0	B	19	6	9
HB plus	6	21	7	9	2	3	1	5	3	16	9	5	1	B	19	6	9

HB plus	6	21	3	14	2	3	2	5	3	16	9	5	2	B	19	6	9
HB plus	6	21	9	12	2	3	3	6	3	16	9	4	2	T	19	6	9
HB plus	6	21	5	16	2	3	4	6	3	16	9	4	0	T	19	6	9
HB plus	6	21	1	18	2	3	5	6	3	16	9	4	1	T	19	6	9
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HB plus	6	22	16r	18	1	1	0	1	3	17	10	2	0	B	19	6	10
HB plus	6	22	15r	13	1	1	1	1	3	17	10	2	1	B	19	6	10
HB plus	6	22	14	14	1	1	2	1	3	17	10	2	2	B	19	6	10
HB plus	6	22	16f	17	1	1	3	2	3	17	10	3	2	B	19	6	10
HB plus	6	22	15f	19	1	1	4	2	3	17	10	3	0	B	19	6	10
HB plus	6	22	13	15	1	1	5	2	3	17	10	3	1	B	19	6	10
HB plus	6	22	10	9	1	2	0	3	3	16	9	7	0	T	19	6	9
HB plus	6	22	6	5	1	2	1	3	3	16	9	7	1	T	19	6	9
HB plus	6	22	2	2	1	2	2	3	3	16	9	7	2	T	19	6	9
HB plus	6	22	12	16	1	2	3	4	3	16	9	6	2	B	19	6	9
HB plus	6	22	8	12	1	2	4	4	3	16	9	6	0	B	19	6	9
HB plus	6	22	4	7	1	2	5	4	3	16	9	6	1	B	19	6	9
HB plus	6	22	11	8	1	3	0	5	3	16	9	7	0	B	19	6	9
HB plus	6	22	7	4	1	3	1	5	3	16	9	7	1	B	19	6	9
HB plus	6	22	3	1	1	3	2	5	3	16	9	7	2	B	19	6	9
HB plus	6	22	9	11	1	3	3	6	3	16	9	6	2	T	19	6	9
HB plus	6	22	5	6	1	3	4	6	3	16	9	6	0	T	19	6	9
HB plus	6	22	1	3	1	3	5	6	3	16	9	6	1	T	19	6	9
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	6	19	17	12	4	1	0	1	3	17	10	4	0	T	19	6	10
HE plus	6	19	16	7	4	1	1	1	3	17	10	4	1	T	19	6	10
HE plus	6	19-20	26f	16	4	1	2	1	3	17	10	4	2	T	19	6	10
HE plus	6	19-20	26r	19	4	1	3	2	3	17	10	5	2	T	19	6	10
HE plus	6	19	18f	11	4	1	4	2	3	17	10	5	0	T	19	6	10
HE plus	6	19	18r	3	4	1	5	2	3	17	10	5	1	T	19	6	10
HE plus	6	19-20	28f	6	4	2	0	3	3	18	11	0	0	B	19	6	11
HE plus	6	19-20	28m	18	4	2	1	3	3	18	11	0	1	B	19	6	11
HE plus	6	19-20	29f	15	4	2	2	3	3	18	11	0	2	B	19	6	11
HE plus	6	19-20	28r	14	4	2	3	4	3	18	11	1	2	B	19	6	11
HE plus	6	19-20	24r	5	4	2	4	4	3	18	11	1	0	B	19	6	11
HE plus	6	19-20	24f	2	4	2	5	4	3	18	11	1	1	B	19	6	11
HE plus	6	19	19r	1	4	3	0	5	3	18	11	0	0	T	19	6	11
HE plus	6	19	20f	9	4	3	1	5	3	18	11	0	1	T	19	6	11
HE plus	6	19-20	22r	17	4	3	2	5	3	18	11	0	2	T	19	6	11
HE plus	6	19-20	19f	4	4	3	3	6	3	18	11	1	2	T	19	6	11
HE plus	6	19	20r	8	4	3	4	6	3	18	11	1	0	T	19	6	11
HE plus	6	19-29	22f	13	4	3	5	6	3	18	11	1	1	T	19	6	11
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	6	20	17	12	3	1	0	1	3	17	10	6	0	T	19	6	10
HE plus	6	20	16	16	3	1	1	1	3	17	10	6	1	T	19	6	10
HE plus	6	19-20	25f	7	3	1	2	1	3	17	10	6	2	T	19	6	10
HE plus	6	19-20	25r	3	3	1	3	2	3	17	10	7	2	T	19	6	10
HE plus	6	20	18f	11	3	1	4	2	3	17	10	7	0	T	19	6	10
HE plus	6	20	18r	19	3	1	5	2	3	17	10	7	1	T	19	6	10
HE plus	6	19-20	27f	6	3	2	0	3	3	18	11	4	0	B	19	6	11
HE plus	6	19-20	27m	2	3	2	1	3	3	18	11	4	1	B	19	6	11

HE plus	6	19-20	29m	15	3	2	2	3	3	18	11	4	2	B	19	6	11
HE plus	6	19-20	23f	18	3	2	3	4	3	18	11	5	2	B	19	6	11
HE plus	6	19-20	27r	5	3	2	4	4	3	18	11	5	0	B	19	6	11
HE plus	6	19-20	23r	14	3	2	5	4	3	18	11	5	1	B	19	6	11
HE plus	6	20	19r	17	3	3	0	5	3	18	11	2	0	T	19	6	11
HE plus	6	20	20f	9	3	3	1	5	3	18	11	2	1	T	19	6	11
HE plus	6	19-20	21r	1	3	3	2	5	3	18	11	2	2	T	19	6	11
HE plus	6	19-20	21f	4	3	3	3	6	3	18	11	3	2	T	19	6	11
HE plus	6	20	19f	13	3	3	4	6	3	18	11	3	0	T	19	6	11
HE plus	6	19-29	20r	8	3	3	5	6	3	18	11	3	1	T	19	6	11
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	6	21	17	12	2	1	0	1	3	17	10	4	0	B	19	6	10
HE plus	6	21	16	7	2	1	1	1	3	17	10	4	1	B	19	6	10
HE plus	6	21-22	25f	16	2	1	2	1	3	17	10	4	2	B	19	6	10
HE plus	6	21-22	25r	19	2	1	3	2	3	17	10	5	2	B	19	6	10
HE plus	6	21	18f	11	2	1	4	2	3	17	10	5	0	B	19	6	10
HE plus	6	21	18r	3	2	1	5	2	3	17	10	5	1	B	19	6	10
HE plus	6	21-22	27f	15	2	2	0	3	3	18	11	6	0	B	19	6	11
HE plus	6	21-22	27m	18	2	2	1	3	3	18	11	6	1	B	19	6	11
HE plus	6	21-22	29m	6	2	2	2	3	3	18	11	6	2	B	19	6	11
HE plus	6	21-22	23f	2	2	2	3	4	3	18	11	7	2	B	19	6	11
HE plus	6	21-22	27r	14	2	2	4	4	3	18	11	7	0	B	19	6	11
HE plus	6	21-22	23r	5	2	2	5	4	3	18	11	7	1	B	19	6	11
HE plus	6	21	19r	1	2	3	0	5	3	18	11	6	0	T	19	6	11
HE plus	6	21	20f	9	2	3	1	5	3	18	11	6	1	T	19	6	11
HE plus	6	21-22	21r	17	2	3	2	5	3	18	11	6	2	T	19	6	11
HE plus	6	21	21f	13	2	3	3	6	3	18	11	7	2	T	19	6	11
HE plus	6	21	19f	4	2	3	4	6	3	18	11	7	0	T	19	6	11
HE plus	6	21-22	20r	8	2	3	5	6	3	18	11	7	1	T	19	6	11
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	
HE plus	6	22	17	12	1	1	0	1	3	17	10	6	0	B	19	6	10
HE plus	6	22	16	16	1	1	1	1	3	17	10	6	1	B	19	6	10
HE plus	6	21-22	26f	7	1	1	2	1	3	17	10	6	2	B	19	6	10
HE plus	6	21-22	26r	3	1	1	3	2	3	17	10	7	2	B	19	6	10
HE plus	6	22	18f	11	1	1	4	2	3	17	10	7	0	B	19	6	10
HE plus	6	22	18r	19	1	1	5	2	3	17	10	7	1	B	19	6	10
HE plus	6	21-22	28f	15	1	2	0	3	3	18	11	2	0	B	19	6	11
HE plus	6	21-22	28m	2	1	2	1	3	3	18	11	2	1	B	19	6	11
HE plus	6	21-22	29f	6	1	2	2	3	3	18	11	2	2	B	19	6	11
HE plus	6	21-22	28r	5	1	2	3	4	3	18	11	3	2	B	19	6	11
HE plus	6	21-22	24r	14	1	2	4	4	3	18	11	3	0	B	19	6	11
HE plus	6	21-22	24f	18	1	2	5	4	3	18	11	3	1	B	19	6	11
HE plus	6	22	19r	17	1	3	0	5	3	18	11	4	0	T	19	6	11
HE plus	6	22	20f	9	1	3	1	5	3	18	11	4	1	T	19	6	11
HE plus	6	21-22	22r	4	1	3	2	5	3	18	11	4	2	T	19	6	11
HE plus	6	22	19f	13	1	3	3	6	3	18	11	5	2	T	19	6	11
HE plus	6	22	20r	8	1	3	4	6	3	18	11	5	0	T	19	6	11
HE plus	6	21-22	22f	1	1	3	5	6	3	18	11	5	1	T	19	6	11
Det	W	Phi tower	pixel	RM	Card	QIE	Qfib	Crate	Hslot	HTR	Hfib	Hch	FPGA	Dslot	DCC	Dch	