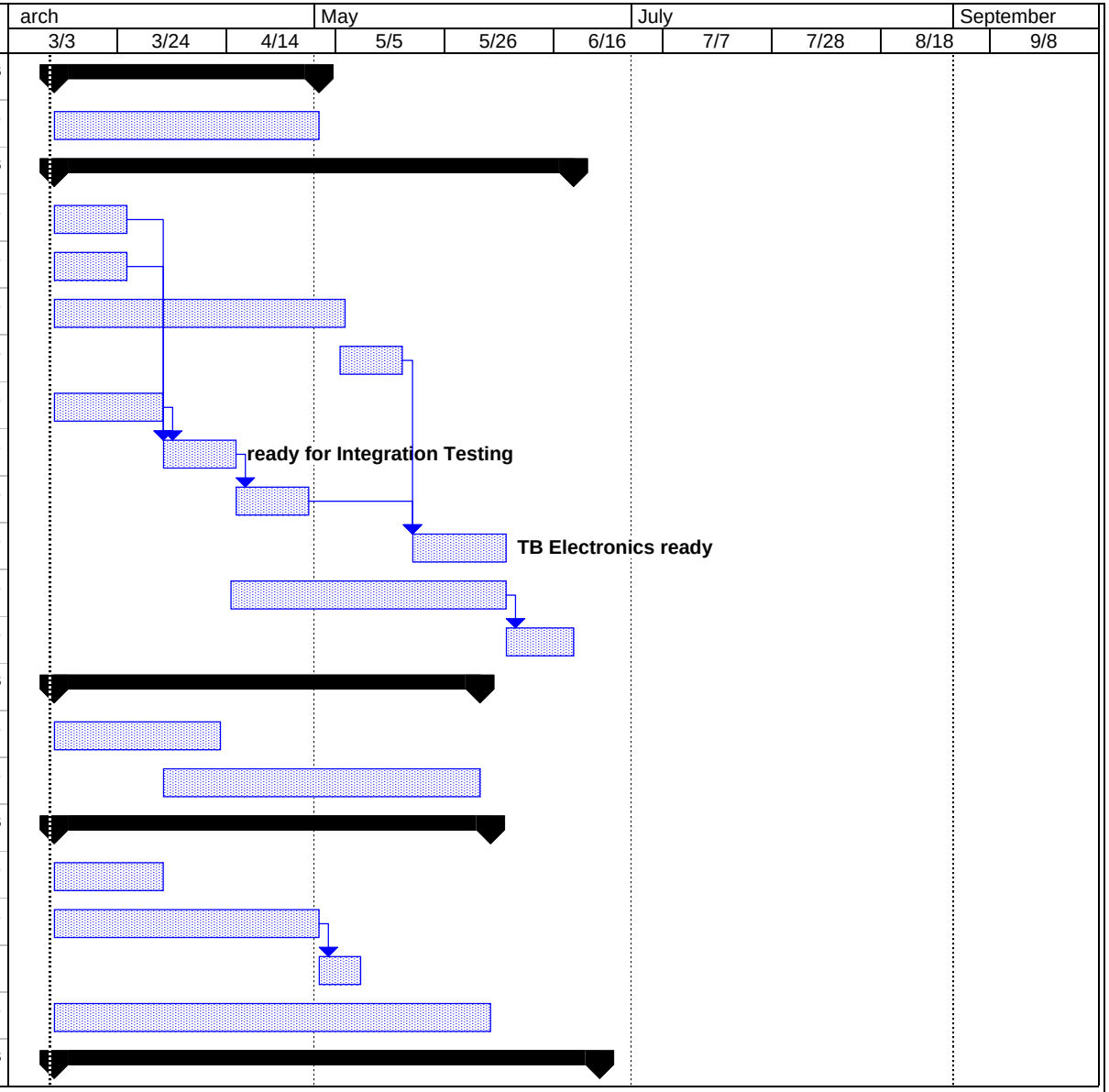
ID	Task Name	Duration
1	**Wedges**	**37 days**
2	wedge prep in 168	37 days
3	**FE TB Electronics**	**74 days**
4	package TB QIE	10 days
5	package proto CCA	10 days
6	fab eng. run CCA	40 days
7	package eng. Run CCA	10 days
8	Fab 6 Channel proto PCB(qty 4)	15 days
9	Assemble/test proto PCB	10 days
10	Fab TB 6 channel PCB(qty 30)	10 days
11	Assemble/test TB PCB	15 days
12	Submit eng. Run QIE	40 days
13	Package eng. Run QIE	10 days
14	**Clock**	**60 days**
15	Clock board (Princeton)	24 days
16	Clock/TTC fanout tests	45 days
17	**HTR**	**61 days**
18	HTR GOL input (UMd)	15 days
19	HTR board fab/test	37 days
20	HTR VME interface	6 days
21	HTR FPGA code	61 days
22	**Integration**	**77 days**



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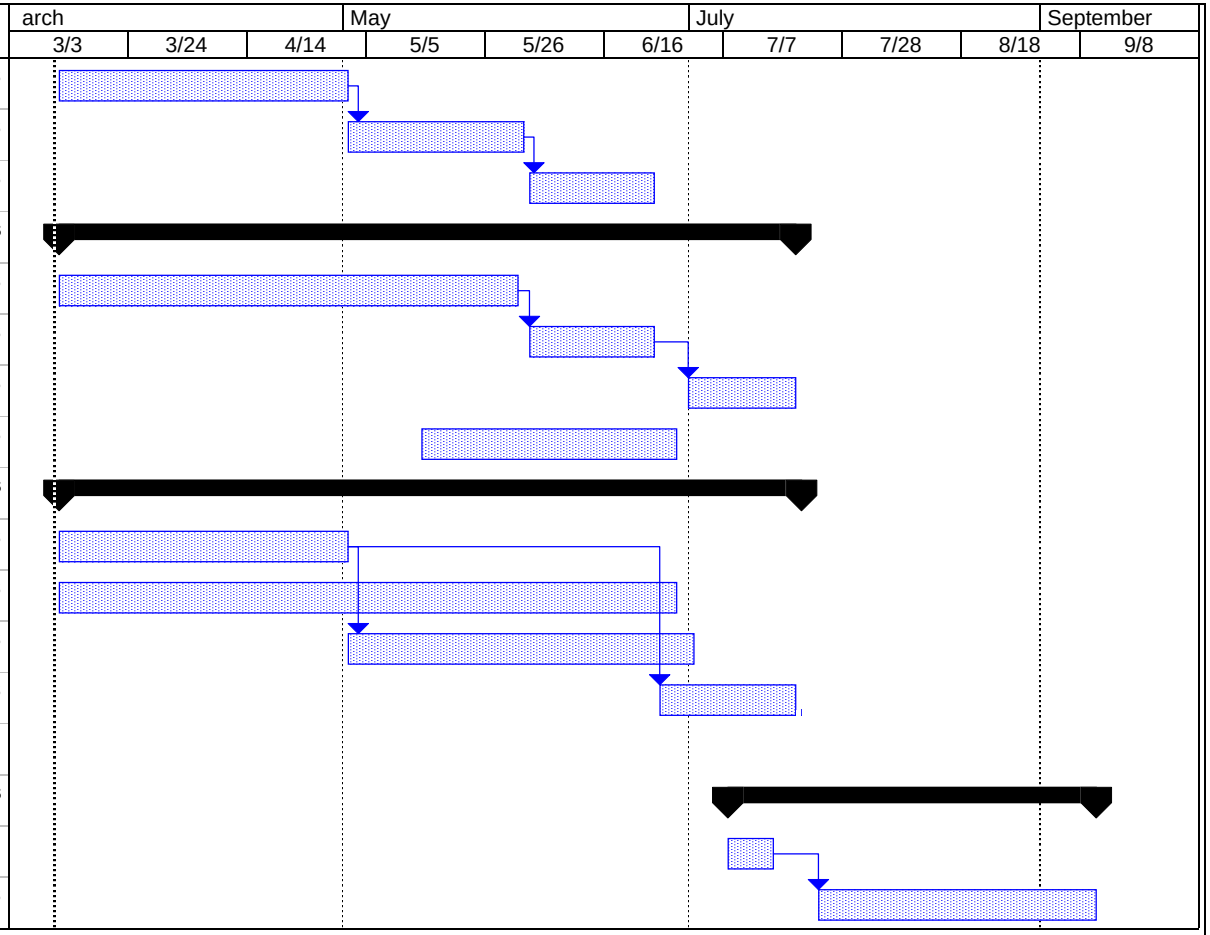
Task		Rolled Up Task		External Tasks	
Progress		Rolled Up Milestone		Project Summary	
Milestone		Rolled Up Progress			
Summary		Split			

ID	Task Name	Duration
23	DCC FPGA code	37 days
24	HTR/DCC/TCC int. (BU)	23 days
25	DCC/HTR/QIE int. (FNAL)	17 days
26	**Controls**	**96 days**
27	DCS for source	59 days
28	source scan at FNAL	17 days
29	source scan at CERN	15 days
30	HV, LV, moving table	35 days
31	**DAQ**	**96 days**
32	DAQ 6u VME/CAMAC	37 days
33	Run Control DAQ	81 days
34	VME 6u/9u integration	45 days
35	DAQ/DCS integration	18 days
36		
37	**Testbeam**	**47 days**
38	ECAL setup	6 days
39	test beam data	35 days



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Task		Rolled Up Task		External Tasks	
Progress		Rolled Up Milestone		Project Summary	
Milestone		Rolled Up Progress			
Summary		Split			