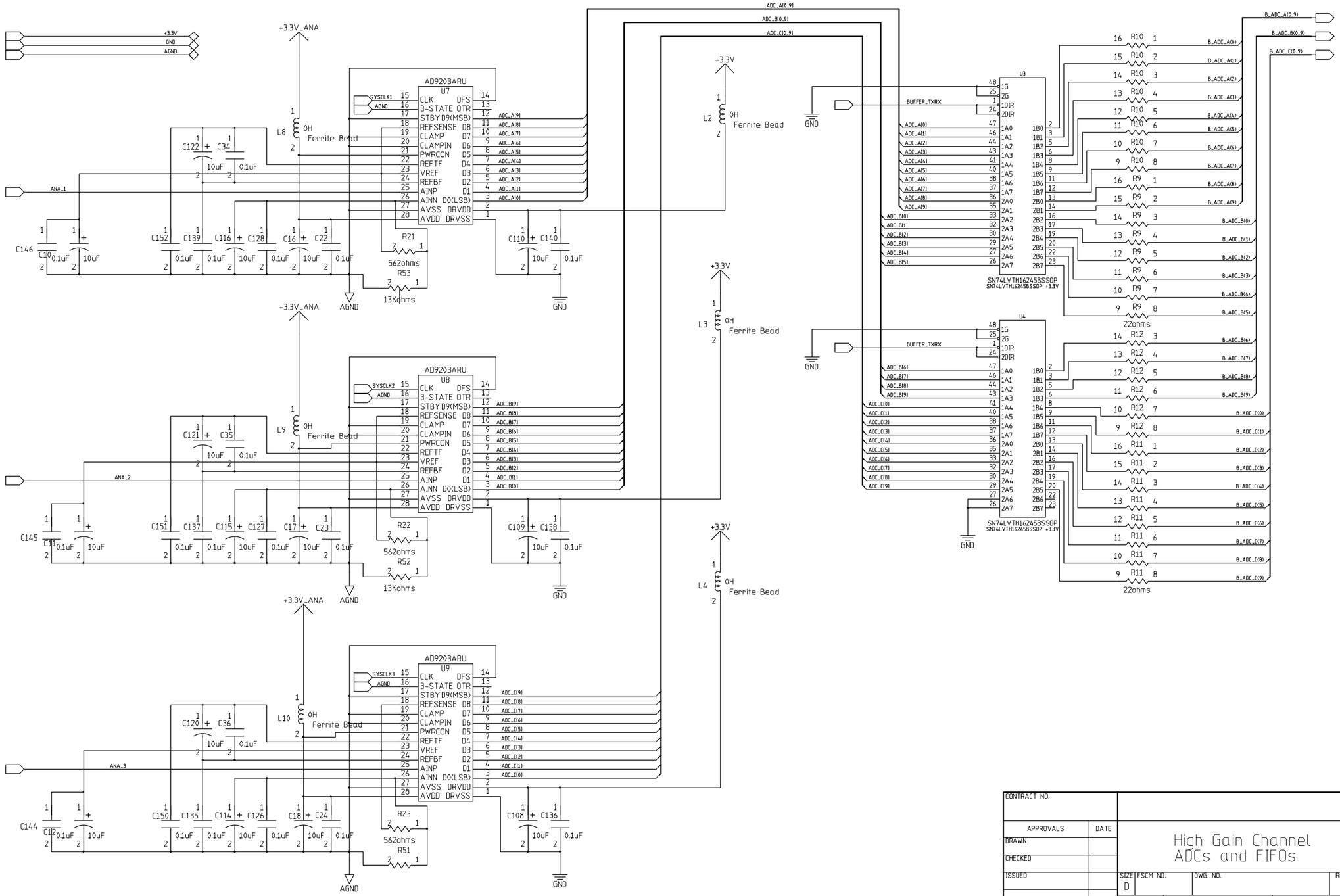
DWG. NO.	SH.	REV

REVISIONS

REV	DESCRIPTION	DATE	APPROVED



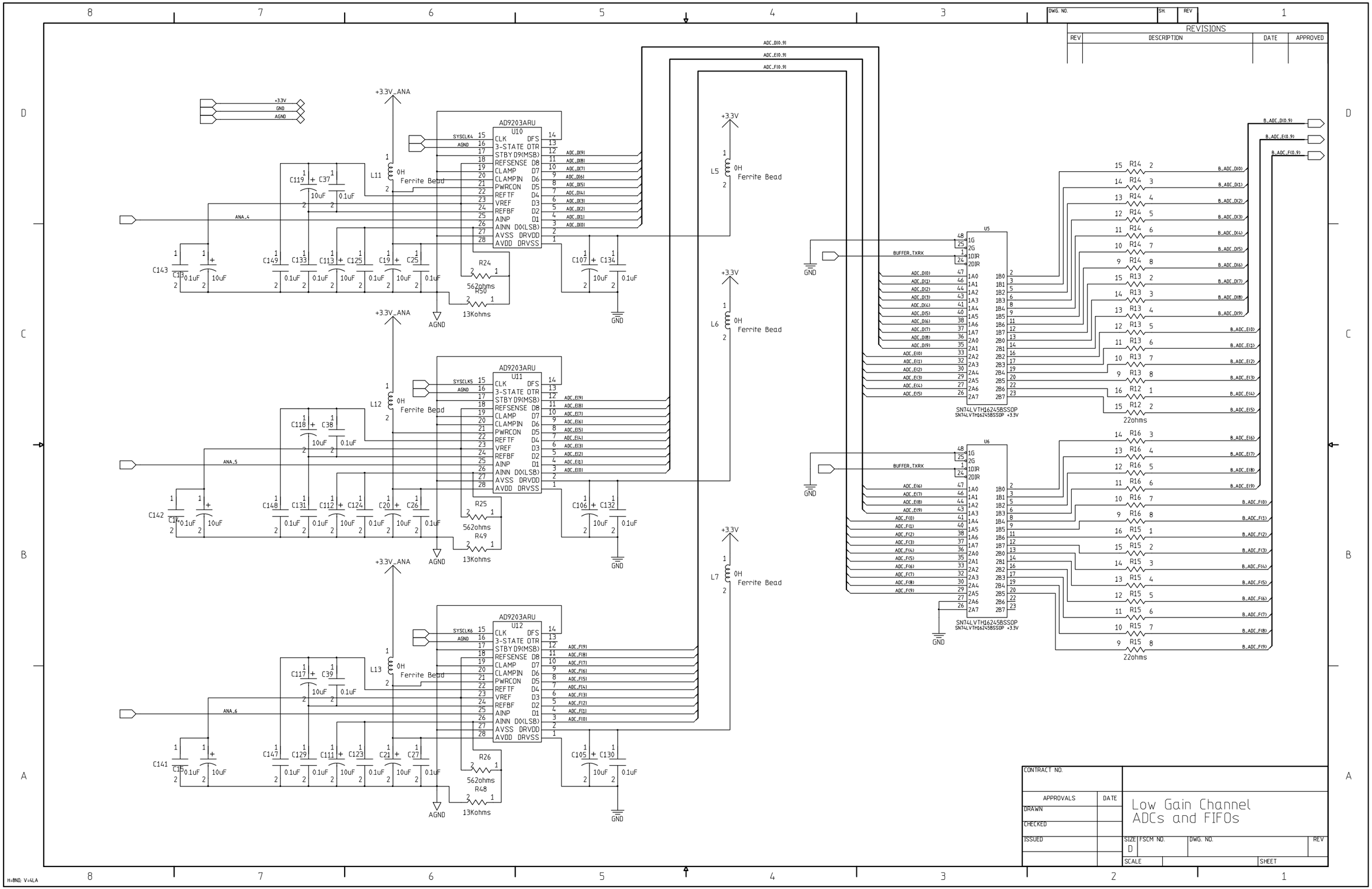
CONTRACT NO.	
APPROVALS	DATE
DRAWN	
CHECKED	
ISSUED	

High Gain Channel ADCs and FIFOs

SIZE	FSCM NO.	DWG. NO.	REV
D			

SCALE | SHEET

H=8ND; V=4LA


REVISIONS
REV
DESCRIPTION
DATE
APPROVED
DWG. NO.
SH.
REV
+3.3V
GND
AGND
+3.3V_ANA
AD9203ARU
U10
U11
U12
CLK
3-STATE
STBY
REFSENSE
CLAMP
CLAMPIN
PWRCON
REFTF
VREF
REFBF
AINP
AINN
AVSS
AVDD
DFS
OTR
D9(MSB)
D8
D7
D6
D5
D4
D3
D2
D1
D0(LSB)
DRVDD
DRVSS
SYSCLK4
SYSCLK5
SYSCLK6
ANA_4
ANA_5
ANA_6
L11
L12
L13
L5
L6
L7
0H
Ferrite Bead
C119
C37
C118
C38
C117
C39
10uF
0.1uF
C143
C149
C133
C113
C125
C19
C25
C107
C134
C142
C148
C131
C112
C124
C20
C26
C106
C132
C141
C147
C129
C111
C123
C21
C27
C105
C130
R24
R50
R25
R49
R26
R48
562ohms
13Kohms
ADC_D(0..9)
ADC_E(0..9)
ADC_F(0..9)
U5
U6
BUFFER_TXRX
SN74LVTH16245BSSOP
SN74LVTH16245BSSOP +3.3V
B_ADC_D(0..9)
B_ADC_E(0..9)
B_ADC_F(0..9)
R14
R13
R12
R16
R15
22ohms
CONTRACT NO.
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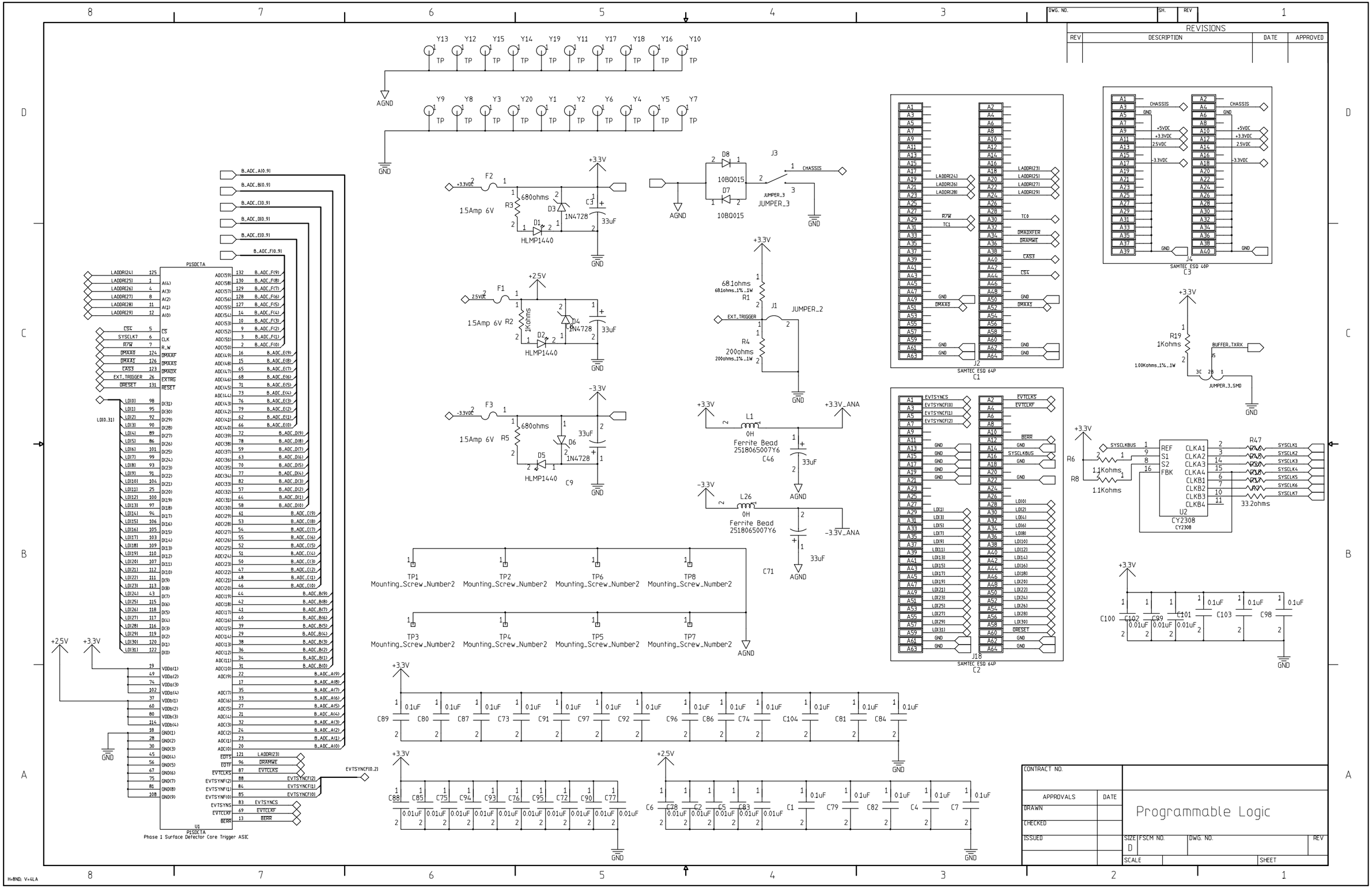
ISSUED
Low Gain Channel
ADCs and FIFOs
SIZE
D
FSCM NO.
DWG. NO.
REV
SCALE
SHEET
H=8ND; V=4LA


REVISIONS
REV
DESCRIPTION
DATE
APPROVED
DWG. NO.
SH.
REV
Y13 Y12 Y15 Y14 Y19 Y11 Y17 Y18 Y16 Y10
Y9 Y8 Y3 Y20 Y1 Y2 Y6 Y4 Y5 Y7
TP
AGND
GND
+3.3V
F2
+3.3VDC
1.5Amp 6V
680ohms
R3
D3
1N4728
C3
33uF
D1
HLMP1440
+2.5V
F1
2.5VDC
1.5Amp 6V R2
1Kohms
D4
1N4728
C8
33uF
D2
HLMP1440
-3.3V
F3
-3.3VDC
1.5Amp 6V R5
680ohms
33uF
D6
1N4728
D5
HLMP1440
C9
D8
10BQ015
D7
10BQ015
J3
JUMPER_3
CHASSIS
68.1ohms
68.1ohms_1%_1W
R1
J1
JUMPER_2
EXT_TRIGGER
R4
200ohms
200ohms_1%_1W
L1
0H
Ferrite Bead
2518065007Y6
C46
33uF
L26
0H
Ferrite Bead
2518065007Y6
-3.3V_ANA
+3.3V_ANA
C71
33uF
TP1 TP2 TP6 TP8
Mounting_Screw_Number2
TP3 TP4 TP5 TP7
Mounting_Screw_Number2
B_ADC_A(0.9)
B_ADC_B(0.9)
B_ADC_C(0.9)
B_ADC_D(0.9)
B_ADC_E(0.9)
B_ADC_F(0.9)
P1SDCTA
LADDR(24)
LADDR(25)
LADDR(26)
LADDR(27)
LADDR(28)
LADDR(29)
CSX
SYSCLK7
R/W
DMAAX0
DMAAX1
CAS3
EXT_TRIGGER
DRESET
LD(0..31)
EDTS
EDTF
EVTCLKS
EVTSYNF(2)
EVTSYNF(1)
EVTSYNF(0)
EVTSYNS
EVTCLKF
BERR
EVTSYNCF(0..2)
EVTSYNCF(2)
EVTSYNCF(1)
EVTSYNCF(0)
DRAMWE
U1
P1SDCTA
Phase 1 Surface Detector Core Trigger ASIC
+2.5V
+3.3V
GND
J2
SAMTEC ESD 64P
C1
J18
SAMTEC ESD 64P
C2
CHASSIS
GND
+5VDC
+3.3VDC
2.5VDC
-3.3VDC
J4
SAMTEC ESD 40P
C3
R19
1Kohms
1.00Kohms_1%_1W
BUFFER_TXRX
JUMPER_3_SMD
R6
1.1Kohms
R8
1.1Kohms
SYSCLKBUS
REF
S1
S2
FBK
CLKA1
CLKA2
CLKA3
CLKA4
CLKB1
CLKB2
CLKB3
CLKB4
U2
CY2308
R47
33.2ohms
SYSCLK1
SYSCLK2
SYSCLK3
SYSCLK4
SYSCLK5
SYSCLK6
SYSCLK7
C100 C102 C99 C101 C103 C98
0.1uF
0.01uF
C89 C80 C87 C73 C91 C97 C92 C96 C86 C74 C104 C81 C84
C88 C85 C75 C94 C93 C76 C95 C72 C90 C77
C6 C78 C2 C5 C83 C1 C79 C82 C4 C7
CONTRACT NO.
APPROVALS
DATE
DRAWN
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ISSUED
Programmable Logic
SIZE
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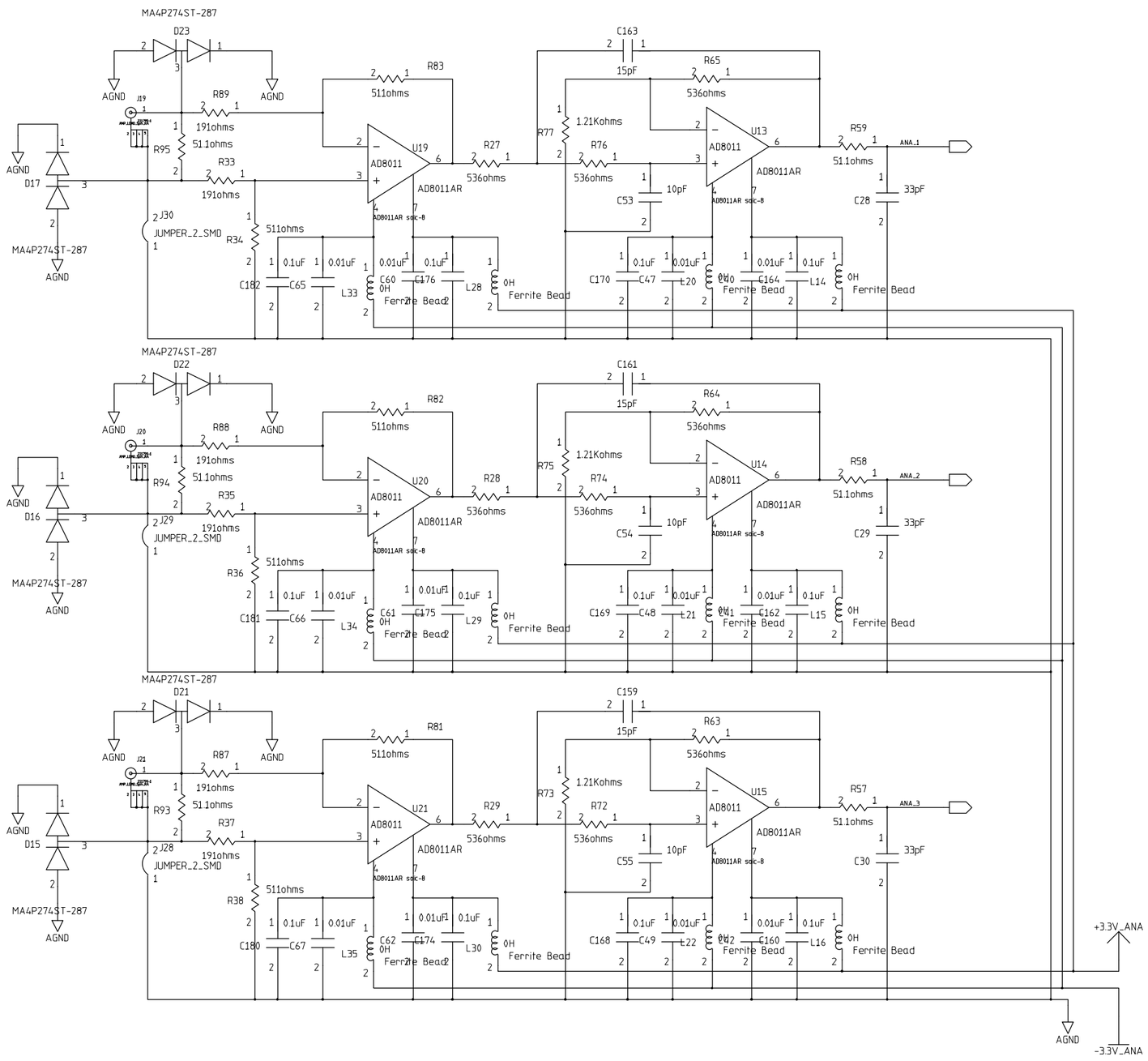
FSCM NO.
DWG. NO.
REV
SCALE
SHEET
H=8ND; V=4LA



DWG. NO.	SH.	REV

REVISIONS

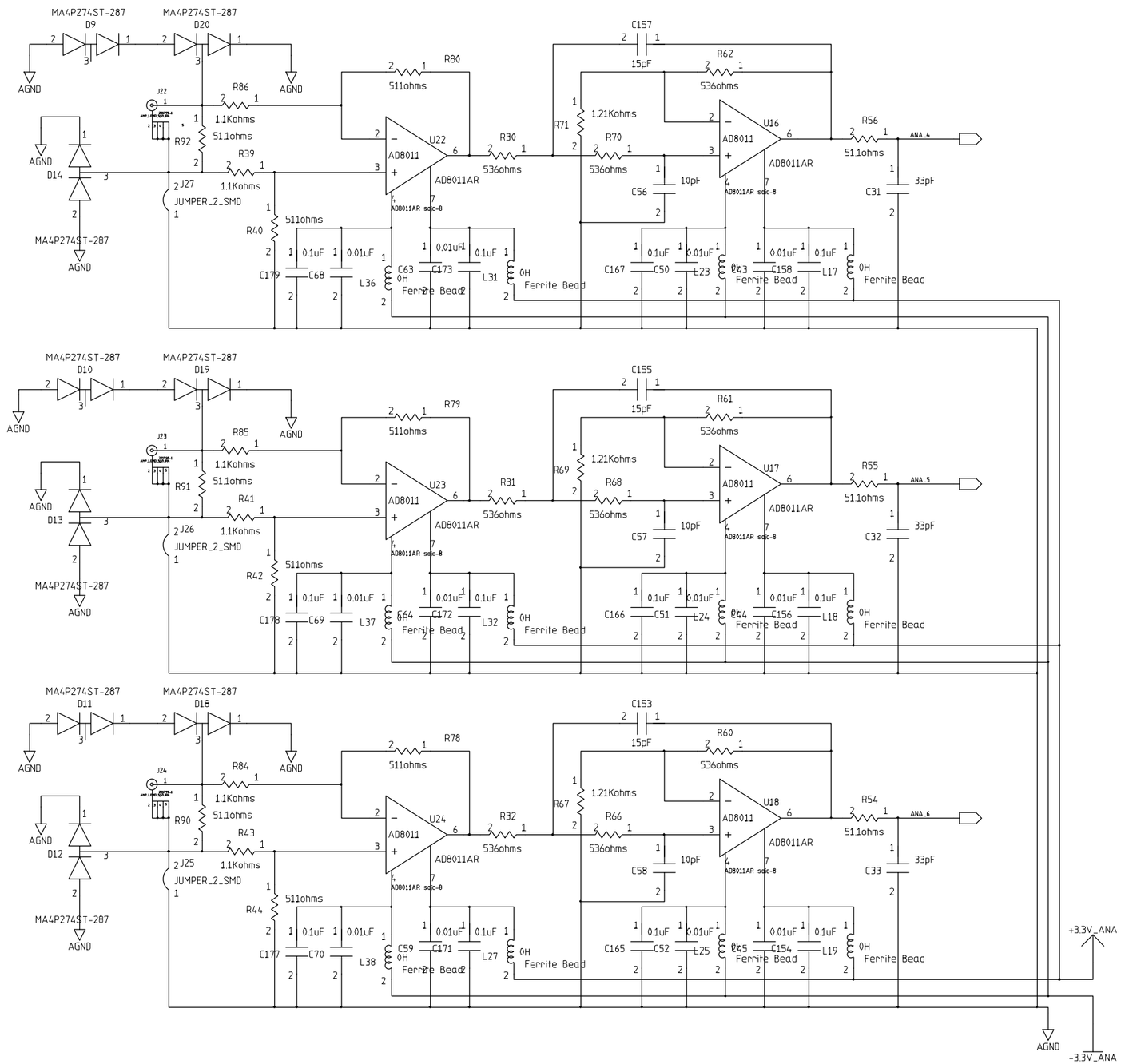
REV	DESCRIPTION	DATE	APPROVED

CONTRACT NO.	
APPROVALS	DATE
DRAWN Mark Koziovsky	
CHECKED	
ISSUED	

ANALOG HIGH GAIN AMPLIFIER

SIZE	FSCM NO.	DWG. NO.	REV
D			
SCALE		SHEET	

H=8ND V=4LA



DWG. NO.	SH.	REV

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

CONTRACT NO.

APPROVALS	DATE
DRAWN Mark Kozlovsky	
CHECKED	
ISSUED	

ANALOG LOW GAIN AMPLIFIER

SIZE	FSCM NO.	DWG. NO.	REV
D			

SCALE | SHEET

H:8ND; V:4LA