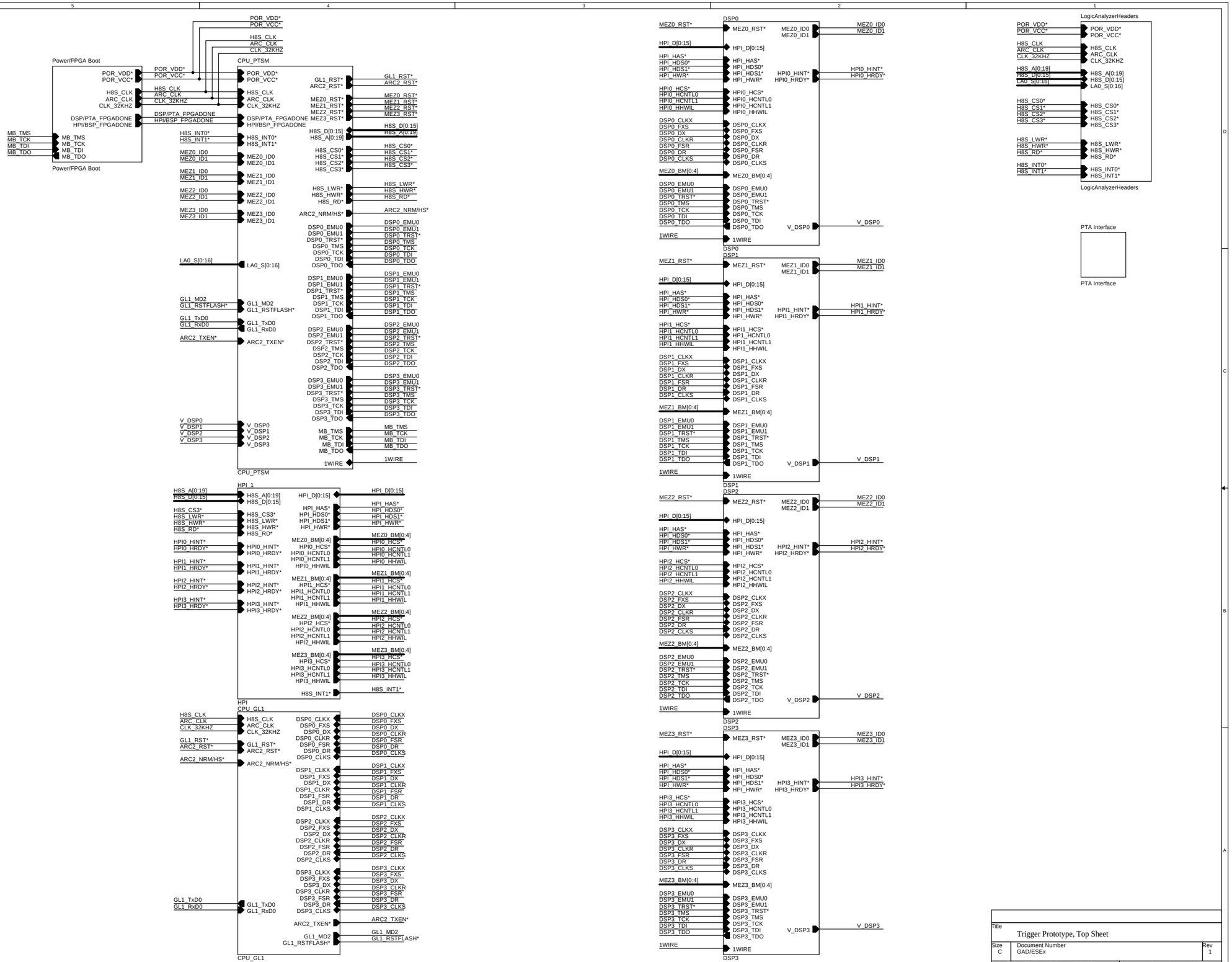
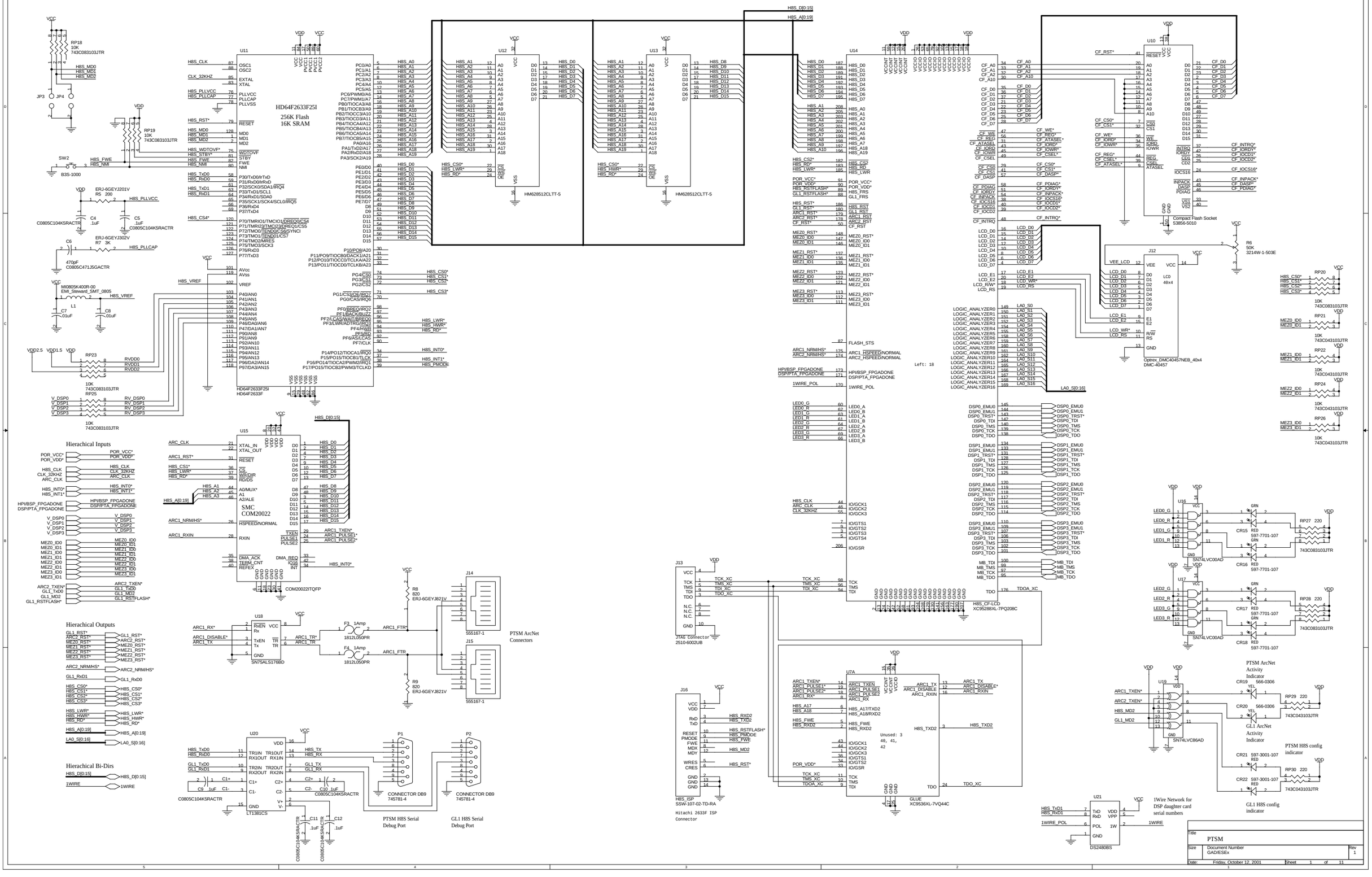
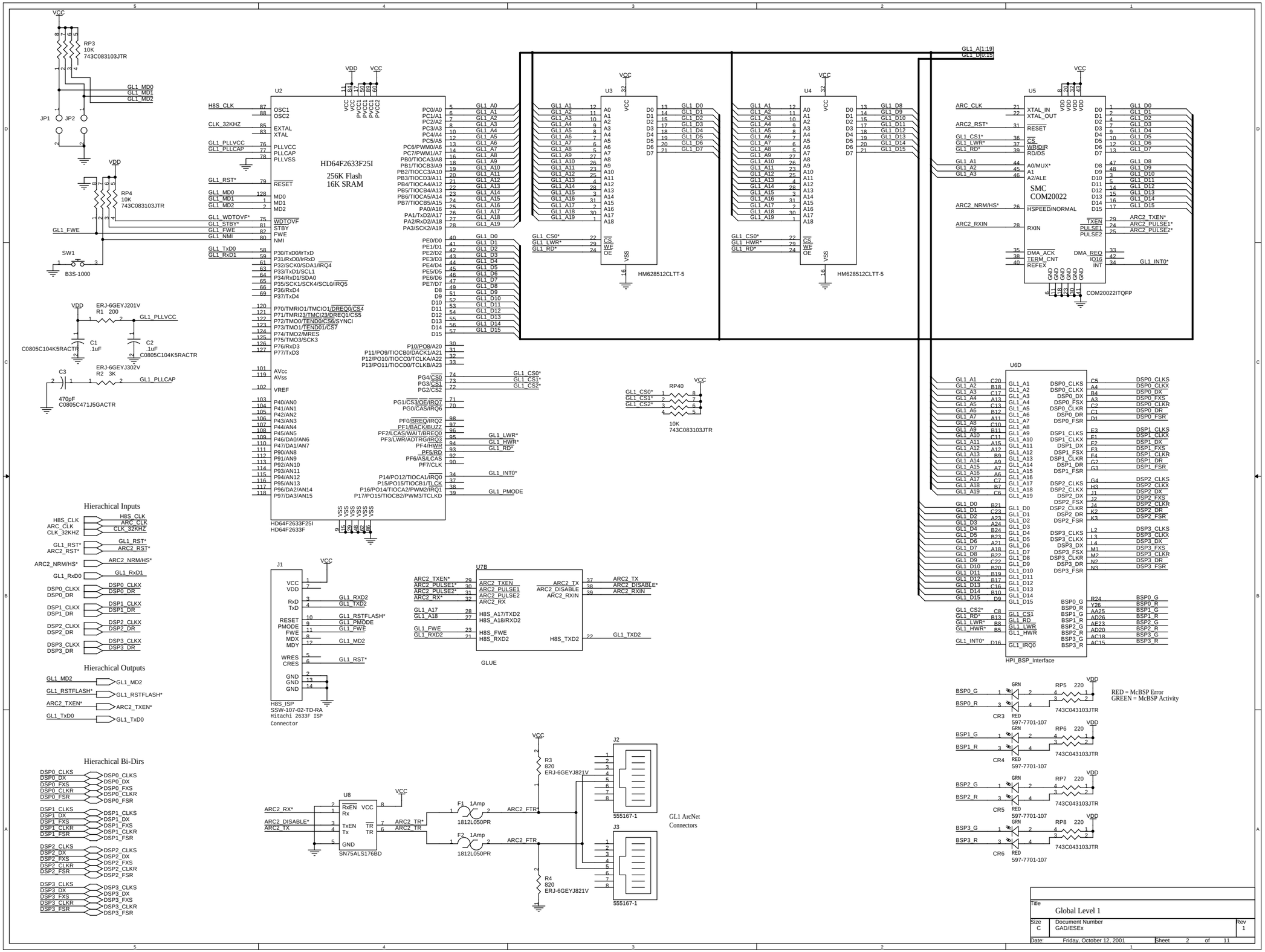


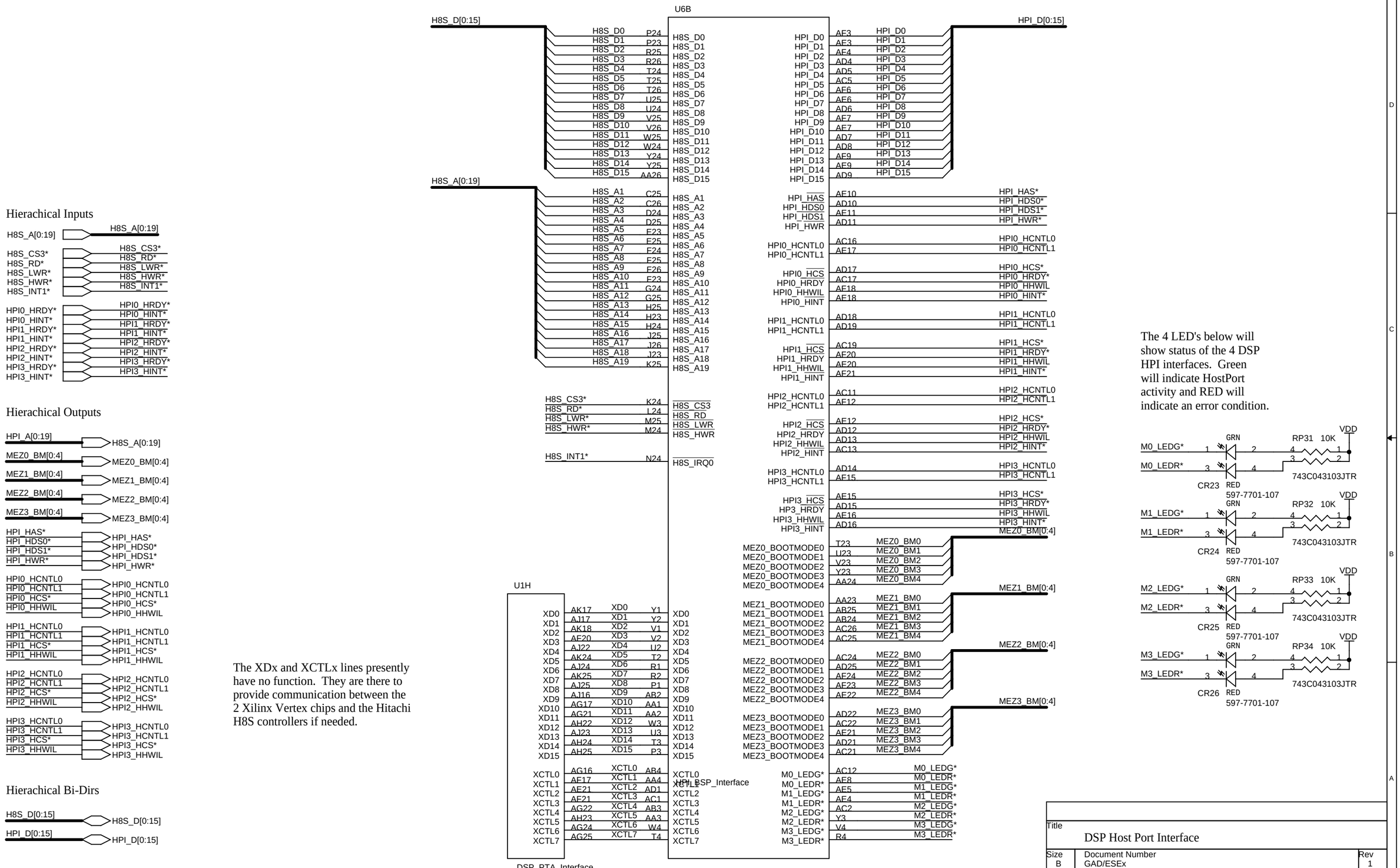
Title: Trigger Prototype, Top Sheet

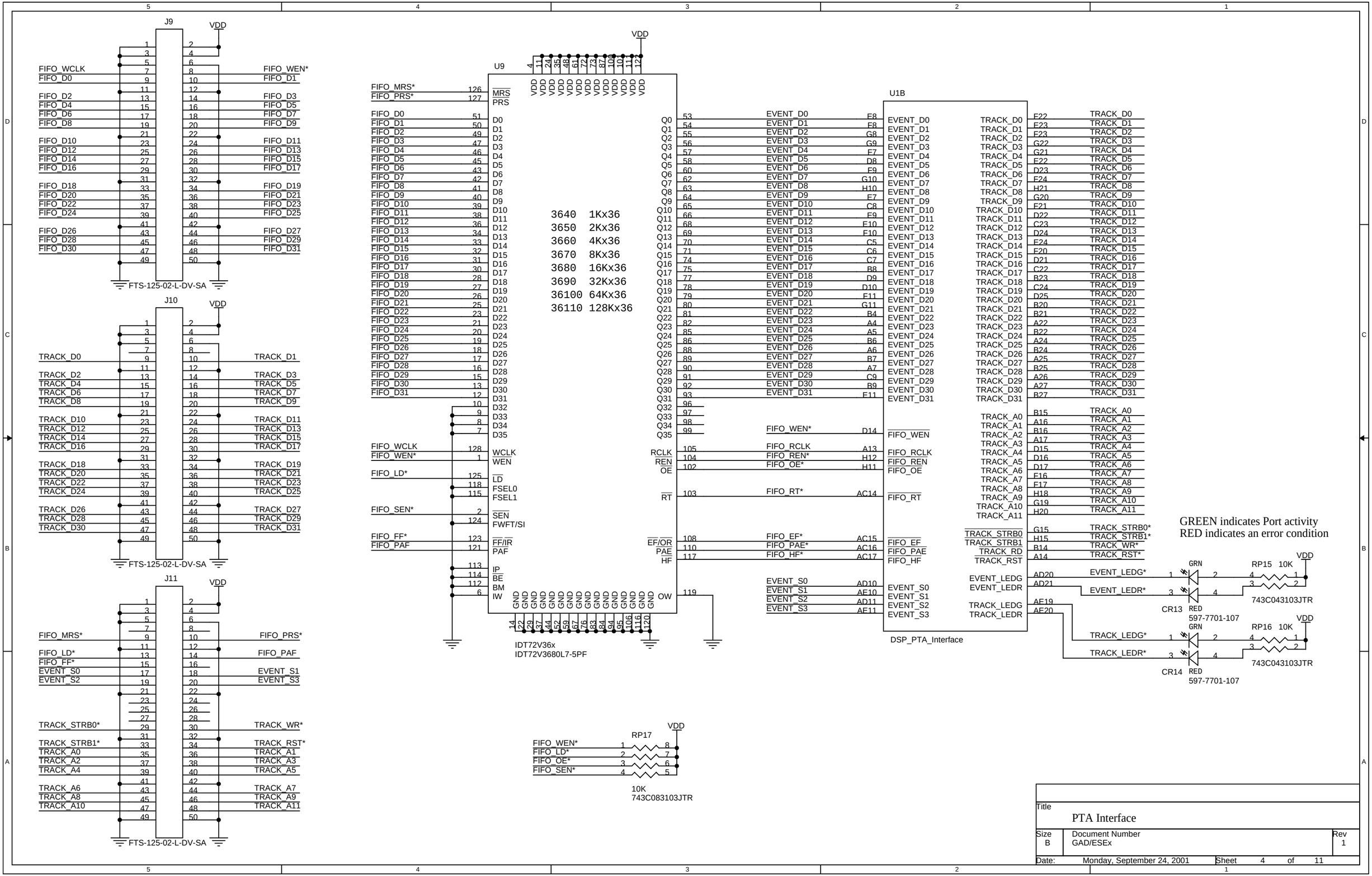
Size	Document Number	Rev
C	GAD/ESEx	1

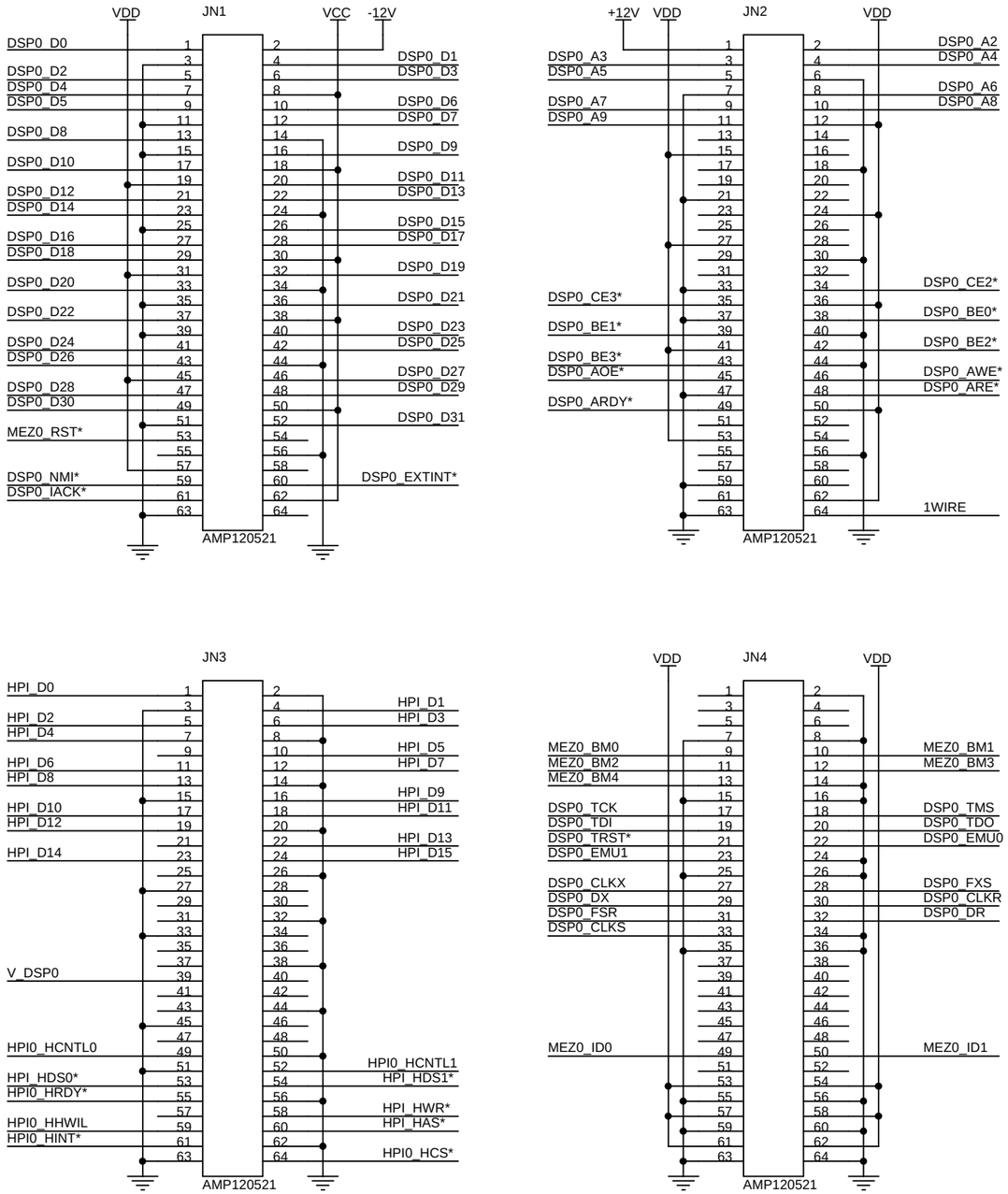
Date: Monday, October 08, 2001 Sheet 0 of 11

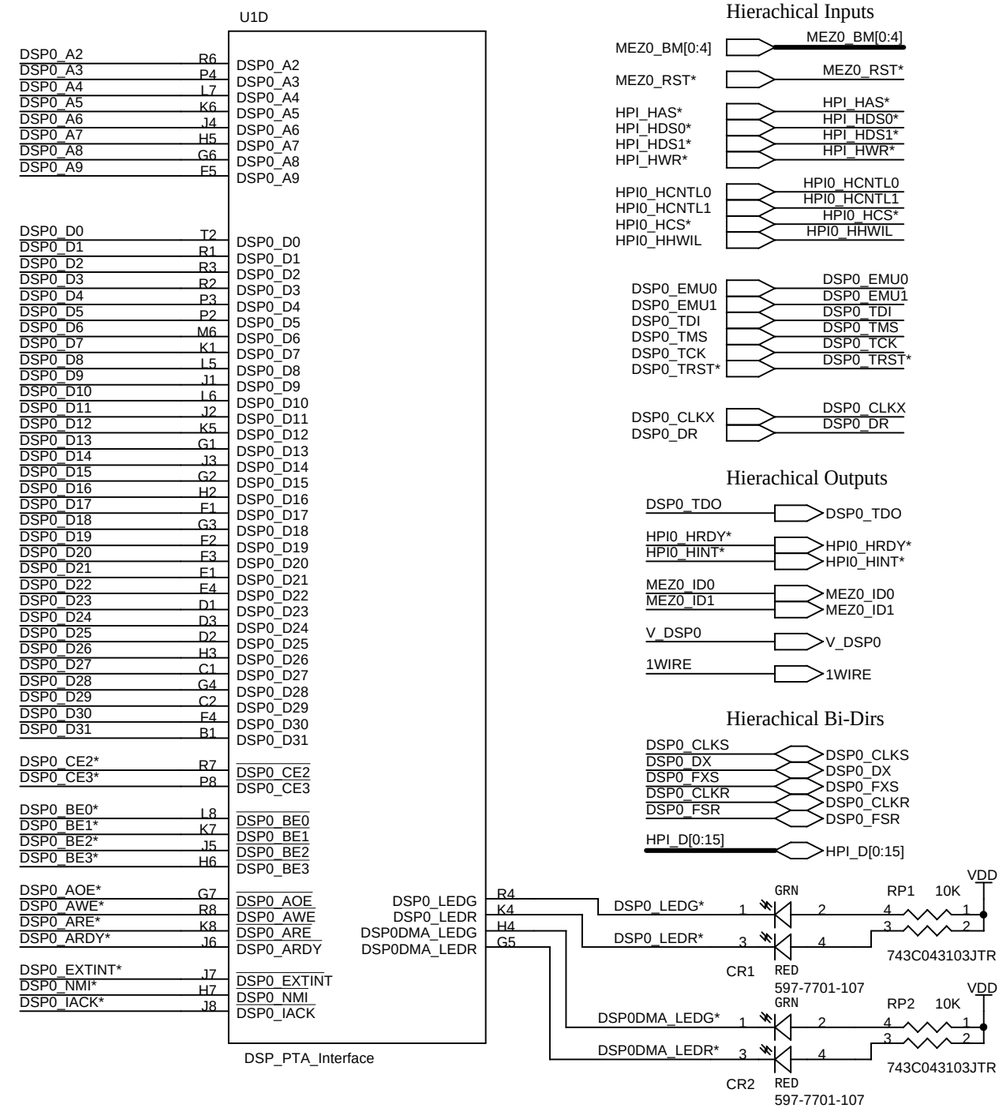

HD64F2633F25I
256K Flash
16K SRAM
HM628512CLTT-5
SMC
COM20022
COM20022ITQFP
Compact Flash Socket
53856-5010
Optrex_DMC40457NEB_40x4
DMC-40457
LCD
40x4
Hierachical Inputs
Hierachical Outputs
Hierachical Bi-Dirs
PTSM ArcNet
Activity
Indicator
GL1 ArcNet
Activity
Indicator
PTSM H8S config
indicator
GL1 H8S config
indicator
PTSM H8S Serial
Debug Port
GL1 H8S Serial
Debug Port
PTSM ArcNet
Connectors
1Wire Network for
DSP daughter card
serial numbers
Title
PTSM
Size
Document Number
GAD/ESEx
Rev
1
Date:
Friday, October 12, 2001
Sheet
1
of
11


HD64F2633F25I
256K Flash
16K SRAM
HD64F2633F25I
HD64F2633F
U2
U3
U4
U5
U6D
U7B
U8
HM628512CLTT-5
COM20022
COM20022ITQFP
HPI_BSP_Interface
GLUE
SN75ALS176BD
H8S_ISP
SSW-107-02-TD-RA
Hitachi 2633F ISP
Connector
J1
J2
J3
555167-1
GL1 ArcNet
Connectors
Hierachical Inputs
Hierachical Outputs
Hierachical Bi-Dirs
RED = McBSP Error
GREEN = McBSP Activity
Title
Global Level 1
Size
C
Document Number
GAD/ESEx
Rev
1
Date:
Friday, October 12, 2001
Sheet
2
of
11

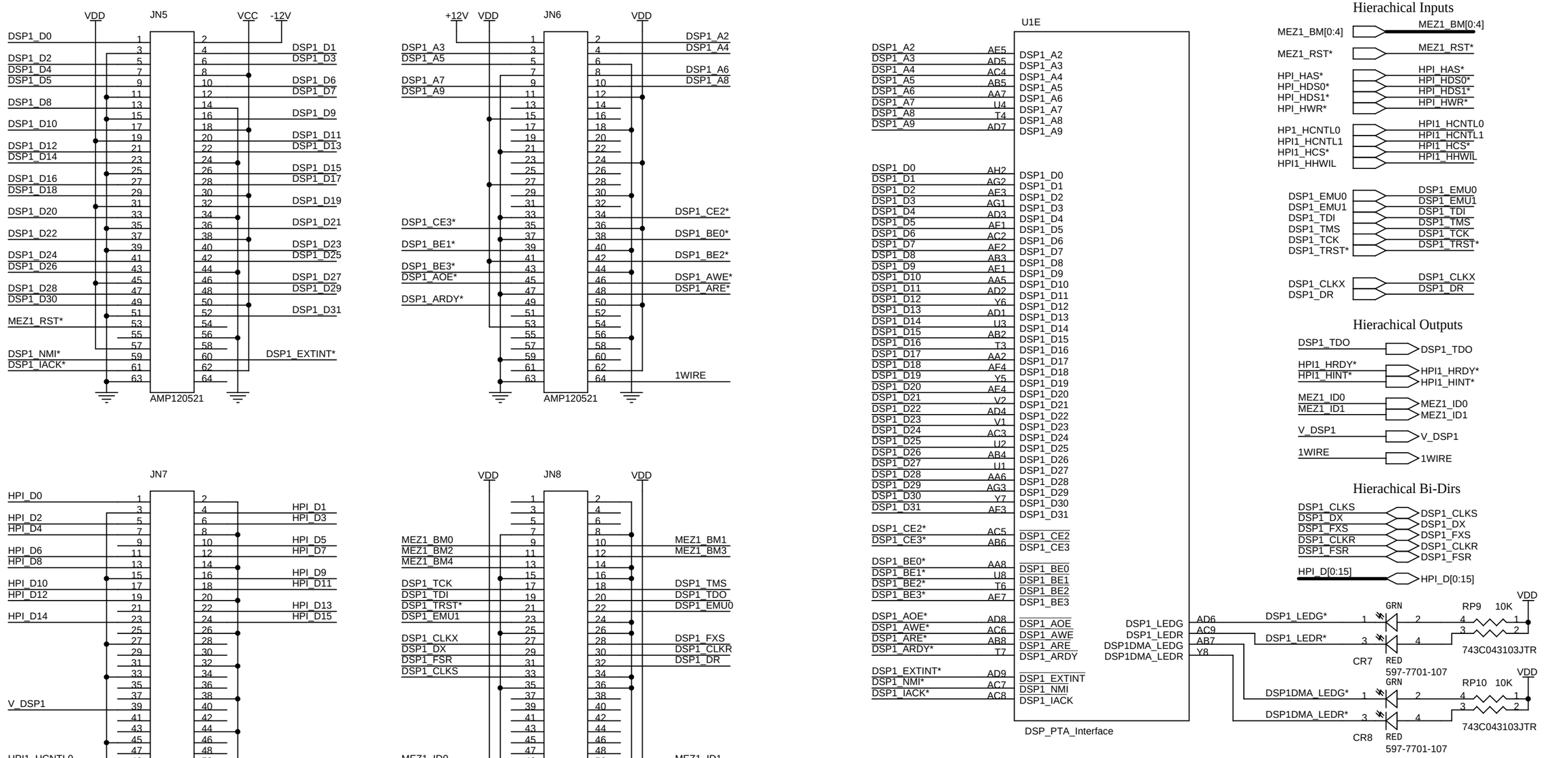

U6B
H8S_D[0:15]
H8S_A[0:19]
HPI_D[0:15]
H8S_D0 P24
H8S_D1 P23
H8S_D2 R25
H8S_D3 R26
H8S_D4 T24
H8S_D5 T25
H8S_D6 T26
H8S_D7 U25
H8S_D8 U24
H8S_D9 V25
H8S_D10 V26
H8S_D11 W25
H8S_D12 W24
H8S_D13 Y24
H8S_D14 Y25
H8S_D15 AA26
H8S_A1 C25
H8S_A2 C26
H8S_A3 D24
H8S_A4 D25
H8S_A5 E23
H8S_A6 E25
H8S_A7 E24
H8S_A8 E25
H8S_A9 E26
H8S_A10 F23
H8S_A11 G24
H8S_A12 G25
H8S_A13 H25
H8S_A14 H23
H8S_A15 H24
H8S_A16 J25
H8S_A17 J26
H8S_A18 J23
H8S_A19 K25
H8S_CS3* K24
H8S_RD* L24
H8S_LWR* M25
H8S_HWR* M24
H8S_INT1* N24
HPI_D0 AE3
HPI_D1 AE3
HPI_D2 AE4
HPI_D3 AD4
HPI_D4 AD5
HPI_D5 AC5
HPI_D6 AE6
HPI_D7 AE6
HPI_D8 AD6
HPI_D9 AE7
HPI_D10 AE7
HPI_D11 AD7
HPI_D12 AD8
HPI_D13 AE9
HPI_D14 AE9
HPI_D15 AD9
HPI_HAS AE10
HPI_HDS0 AD10
HPI_HDS1 AE11
HPI_HWR AD11
HPI0_HCNTL0 AC16
HPI0_HCNTL1 AE17
HPI0_HCS AD17
HPI0_HRDY AC17
HPI0_HHWIL AE18
HPI0_HINT AE18
HPI1_HCNTL0 AD18
HPI1_HCNTL1 AD19
HPI1_HCS AC19
HPI1_HRDY AE20
HPI1_HHWIL AE20
HPI1_HINT AE21
HPI2_HCNTL0 AC11
HPI2_HCNTL1 AE12
HPI2_HCS AE12
HPI2_HRDY AD12
HPI2_HHWIL AD13
HPI2_HINT AC13
HPI3_HCNTL0 AD14
HPI3_HCNTL1 AE15
HPI3_HCS AE15
HP3_HRDY AD15
HPI3_HHWIL AE16
HPI3_HINT AD16
MEZ0_BOOTMODE0 T23
MEZ0_BOOTMODE1 U23
MEZ0_BOOTMODE2 V23
MEZ0_BOOTMODE3 Y23
MEZ0_BOOTMODE4 AA24
MEZ1_BOOTMODE0 AA23
MEZ1_BOOTMODE1 AB25
MEZ1_BOOTMODE2 AB24
MEZ1_BOOTMODE3 AC26
MEZ1_BOOTMODE4 AC25
MEZ2_BOOTMODE0 AC24
MEZ2_BOOTMODE1 AD25
MEZ2_BOOTMODE2 AE24
MEZ2_BOOTMODE3 AE23
MEZ2_BOOTMODE4 AE22
MEZ3_BOOTMODE0 AD22
MEZ3_BOOTMODE1 AC22
MEZ3_BOOTMODE2 AE21
MEZ3_BOOTMODE3 AD21
MEZ3_BOOTMODE4 AC21
M0_LEDG* AC12
M0_LEDR* AE8
M1_LEDG* AE5
M1_LEDR* AE4
M2_LEDG* AC2
M2_LEDR* Y3
M3_LEDG* V4
M3_LEDR* R4
HPI_HAS*
HPI_HDS0*
HPI_HDS1*
HPI_HWR*
HPI0_HCNTL0
HPI0_HCNTL1
HPI0_HCS*
HPI0_HRDY*
HPI0_HHWIL
HPI0_HINT*
HPI1_HCNTL0
HPI1_HCNTL1
HPI1_HCS*
HPI1_HRDY*
HPI1_HHWIL
HPI1_HINT*
HPI2_HCNTL0
HPI2_HCNTL1
HPI2_HCS*
HPI2_HRDY*
HPI2_HHWIL
HPI2_HINT*
HPI3_HCNTL0
HPI3_HCNTL1
HPI3_HCS*
HPI3_HRDY*
HPI3_HHWIL
HPI3_HINT*
MEZ0_BM[0:4]
MEZ0_BM0
MEZ0_BM1
MEZ0_BM2
MEZ0_BM3
MEZ0_BM4
MEZ1_BM[0:4]
MEZ1_BM0
MEZ1_BM1
MEZ1_BM2
MEZ1_BM3
MEZ1_BM4
MEZ2_BM[0:4]
MEZ2_BM0
MEZ2_BM1
MEZ2_BM2
MEZ2_BM3
MEZ2_BM4
MEZ3_BM[0:4]
MEZ3_BM0
MEZ3_BM1
MEZ3_BM2
MEZ3_BM3
MEZ3_BM4
U1H
DSP_PTA_Interface
XD0 AK17
XD1 AJ17
XD2 AK18
XD3 AE20
XD4 AJ22
XD5 AK24
XD6 AJ24
XD7 AK25
XD8 AJ25
XD9 AJ16
XD10 AG17
XD11 AG21
XD12 AH22
XD13 AJ23
XD14 AH24
XD15 AH25
XCTL0 AG16
XCTL1 AF17
XCTL2 AE21
XCTL3 AF21
XCTL4 AG22
XCTL5 AH23
XCTL6 AG24
XCTL7 AG25
XD0 Y1
XD1 Y2
XD2 V1
XD3 V2
XD4 U2
XD5 T2
XD6 R1
XD7 R2
XD8 P1
XD9 AB2
XD10 AA1
XD11 AA2
XD12 W3
XD13 U3
XD14 T3
XD15 P3
XCTL0 AB4
XCTL1 AA4
XCTL2 AD1
XCTL3 AC1
XCTL4 AB3
XCTL5 AA3
XCTL6 W4
XCTL7 T4
Hierachical Inputs
H8S_A[0:19]
H8S_CS3*
H8S_RD*
H8S_LWR*
H8S_HWR*
H8S_INT1*
HPI0_HRDY*
HPI0_HINT*
HPI1_HRDY*
HPI1_HINT*
HPI2_HRDY*
HPI2_HINT*
HPI3_HRDY*
HPI3_HINT*
Hierachical Outputs
HPI_A[0:19]
MEZ0_BM[0:4]
MEZ1_BM[0:4]
MEZ2_BM[0:4]
MEZ3_BM[0:4]
HPI_HAS*
HPI_HDS0*
HPI_HDS1*
HPI_HWR*
HPI0_HCNTL0
HPI0_HCNTL1
HPI0_HCS*
HPI0_HHWIL
HPI1_HCNTL0
HPI1_HCNTL1
HPI1_HCS*
HPI1_HHWIL
HPI2_HCNTL0
HPI2_HCNTL1
HPI2_HCS*
HPI2_HHWIL
HPI3_HCNTL0
HPI3_HCNTL1
HPI3_HCS*
HPI3_HHWIL
Hierachical Bi-Dirs
H8S_D[0:15]
HPI_D[0:15]
The XDx and XCTLx lines presently have no function. They are there to provide communication between the 2 Xilinx Vertex chips and the Hitachi H8S controllers if needed.
The 4 LED's below will show status of the 4 DSP HPI interfaces. Green will indicate HostPort activity and RED will indicate an error condition.
VDD
M0_LEDG*
M0_LEDR*
GRN
RED
CR23
597-7701-107
RP31 10K
743C043103JTR
M1_LEDG*
M1_LEDR*
CR24
RP32 10K
M2_LEDG*
M2_LEDR*
CR25
RP33 10K
M3_LEDG*
M3_LEDR*
CR26
RP34 10K
Title
DSP Host Port Interface
Size
B
Document Number
GAD/ESEx
Rev
1
Date:
Thursday, October 11, 2001
Sheet 3 of 11


J9
FTS-125-02-L-DV-SA
J10
FTS-125-02-L-DV-SA
J11
FTS-125-02-L-DV-SA
U9
IDT72V36x
IDT72V3680L7-5PF
3640 1Kx36
3650 2Kx36
3660 4Kx36
3670 8Kx36
3680 16Kx36
3690 32Kx36
36100 64Kx36
36110 128Kx36
U1B
DSP_PTA_Interface
GREEN indicates Port activity
RED indicates an error condition
CR13
CR14
597-7701-107
RP15 10K
RP16 10K
743C043103JTR
RP17
10K
743C083103JTR
Title
PTA Interface
Size B
Document Number GAD/ESEx
Rev 1
Date: Monday, September 24, 2001
Sheet 4 of 11





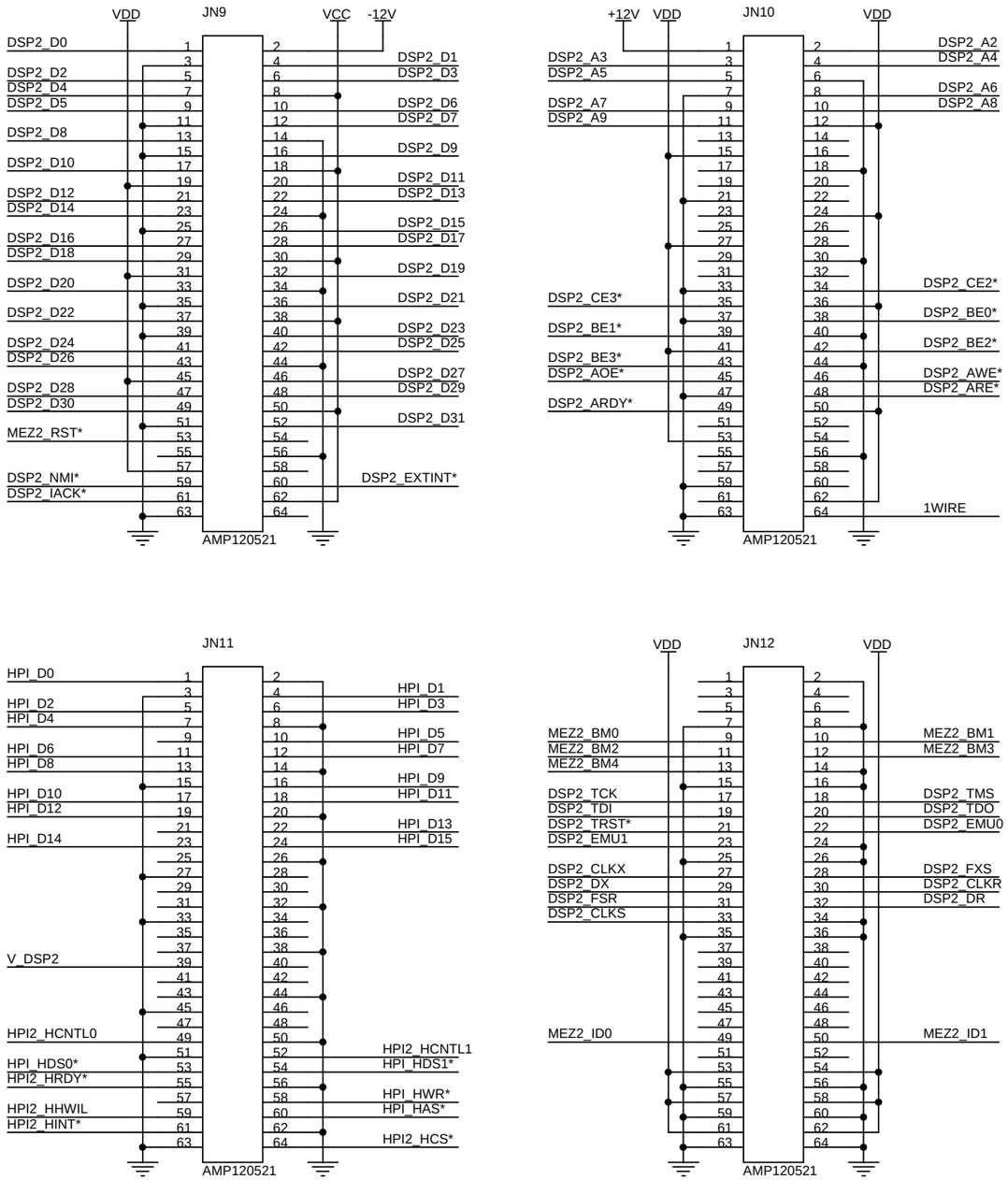
Title	DSP0 Mezzanine Connector	
Size B	Document Number GAD/ESEx	Rev 1
Date: Tuesday, September 25, 2001	Sheet 5 of 11	

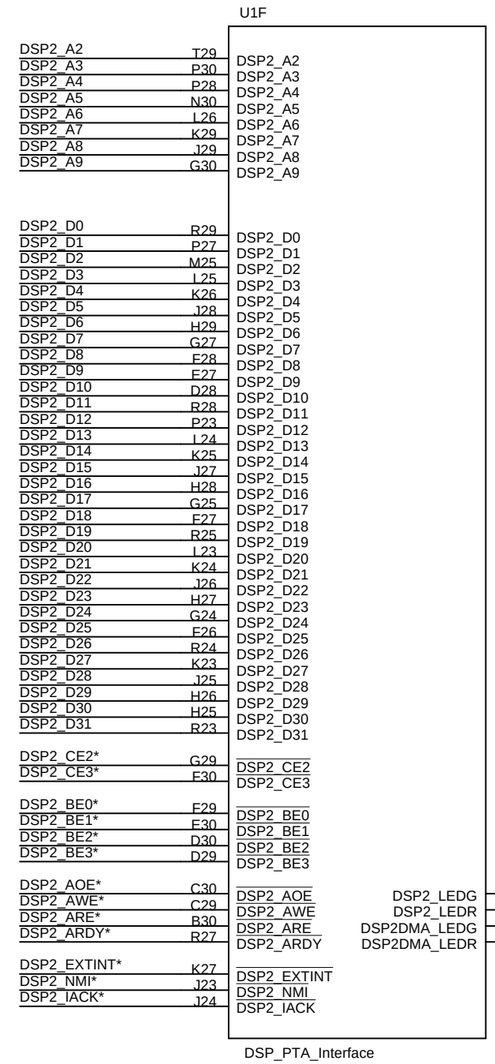


Title
DSP1 Mezzanine Connector

Size	Document Number	Rev
B	GAD/ESEx	1

Date: Tuesday, September 25, 2001 Sheet 6 of 11





Hierachical Inputs

MEZ2_BM[0:4] → MEZ2_BM[0:4]
MEZ2_RST* → MEZ2_RST*
HPI_HAS*, HPI_HDS0*, HPI_HDS1*, HPI_HWR* → HPI_HAS*, HPI_HDS0*, HPI_HDS1*, HPI_HWR*
HPI2_HCNTL0, HPI2_HCNTL1, HPI2_HCS*, HPI2_HHWIL → HPI2_HCNTL0, HPI2_HCNTL1, HPI2_HCS*, HPI2_HHWIL
DSP2_EMU0, DSP2_EMU1, DSP2_TDI, DSP2_TMS, DSP2_TCK, DSP2_TRST* → DSP2_EMU0, DSP2_EMU1, DSP2_TDI, DSP2_TMS, DSP2_TCK, DSP2_TRST*
DSP2_CLKX, DSP2_DR → DSP2_CLKX, DSP2_DR

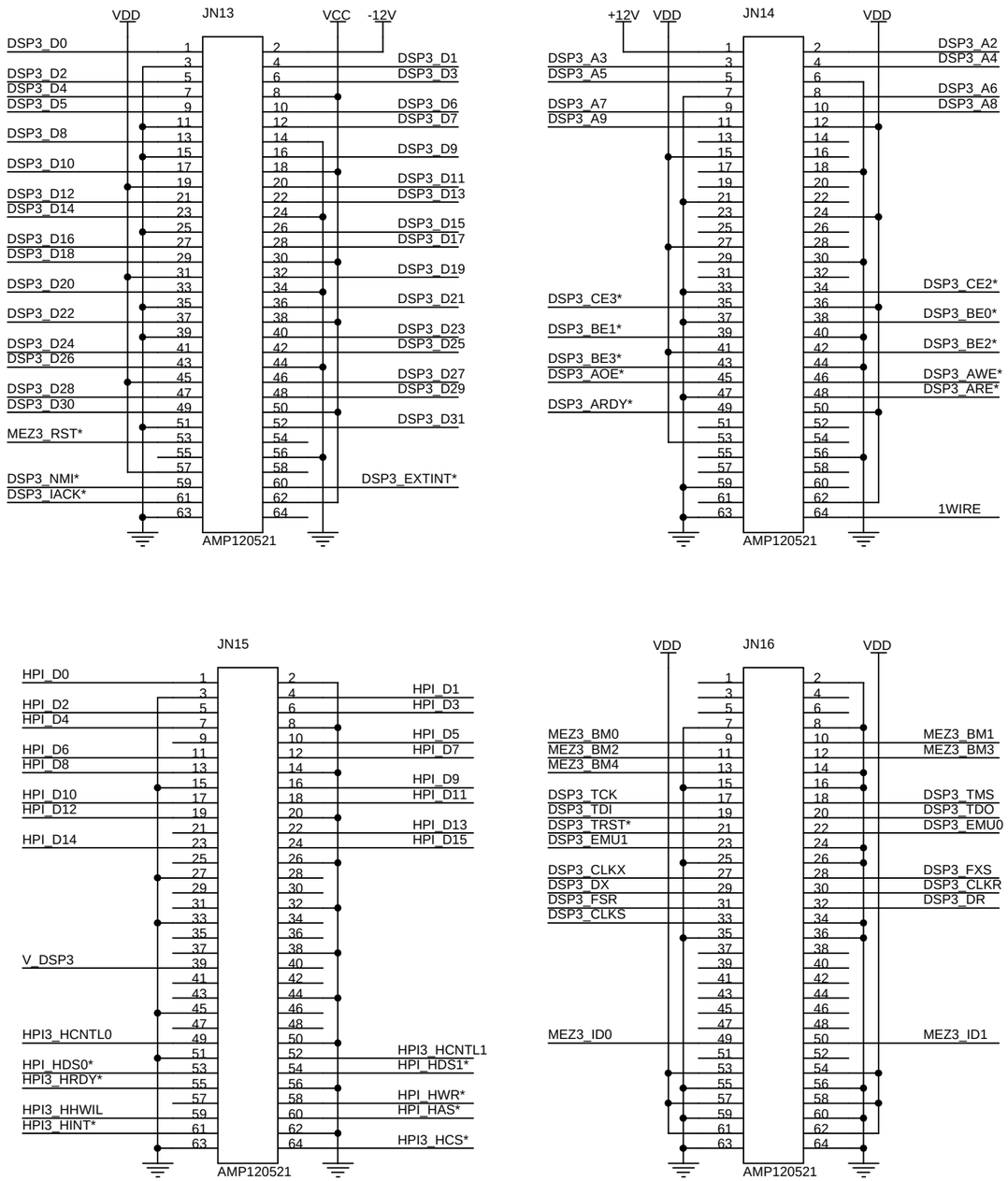
Hierachical Outputs

DSP2_TDO → DSP2_TDO
HPI2_HRDY*, HPI2_HINT* → HPI2_HRDY*, HPI2_HINT*
MEZ2_ID0, MEZ2_ID1 → MEZ2_ID0, MEZ2_ID1
V_DSP2 → V_DSP2
1WIRE → 1WIRE

Hierachical Bi-Dirs

DSP2_CLKS, DSP2_DX, DSP2_FXS, DSP2_CLKR, DSP2_FSR ↔ DSP2_CLKS, DSP2_DX, DSP2_FXS, DSP2_CLKR, DSP2_FSR
HPI_D[0:15] ↔ HPI_D[0:15]

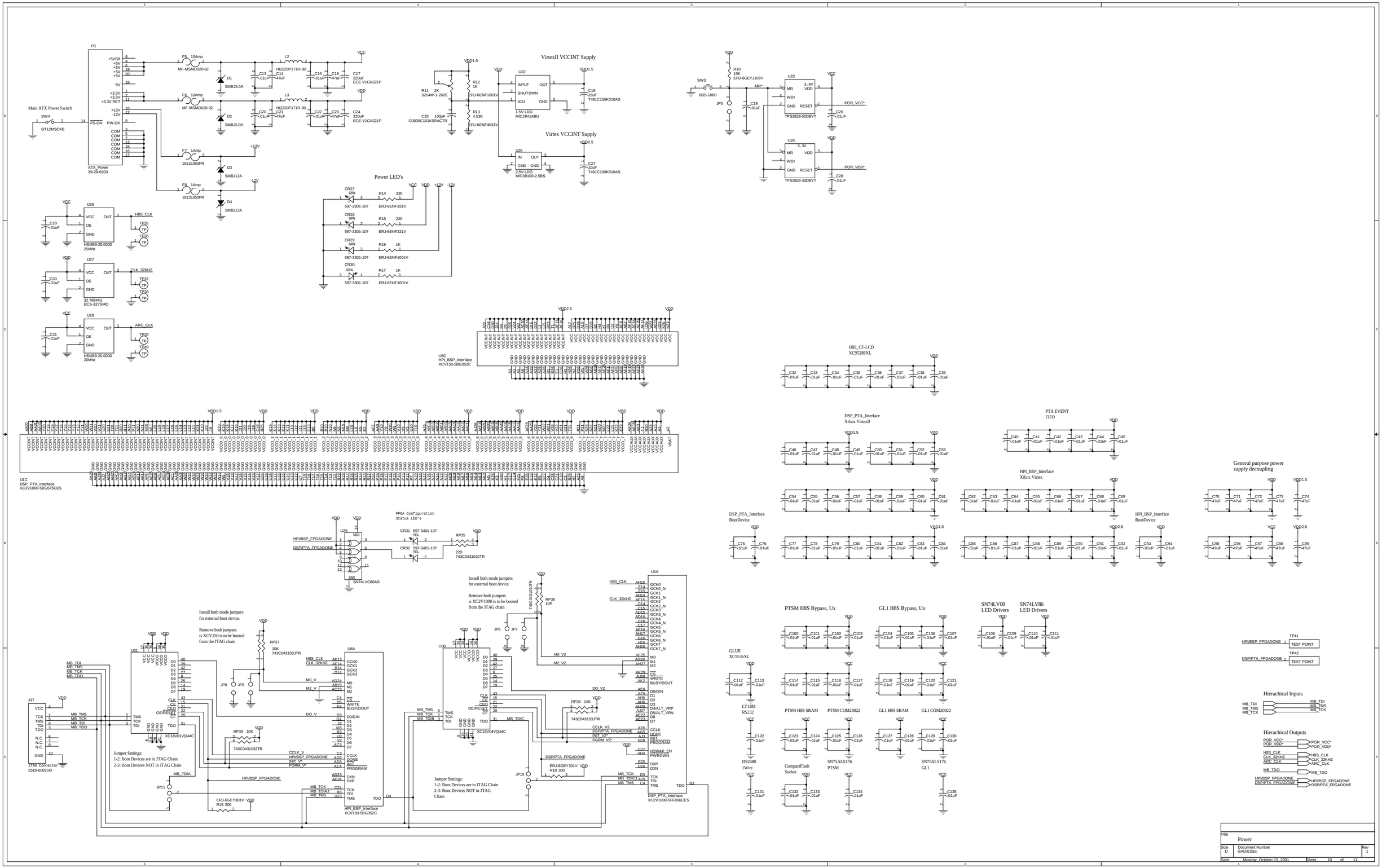
Title	DSP2 Mezzanine Connector	
Size B	Document Number GAD/ESEx	Rev 1
Date: Tuesday, September 25, 2001	Sheet 7 of 11	

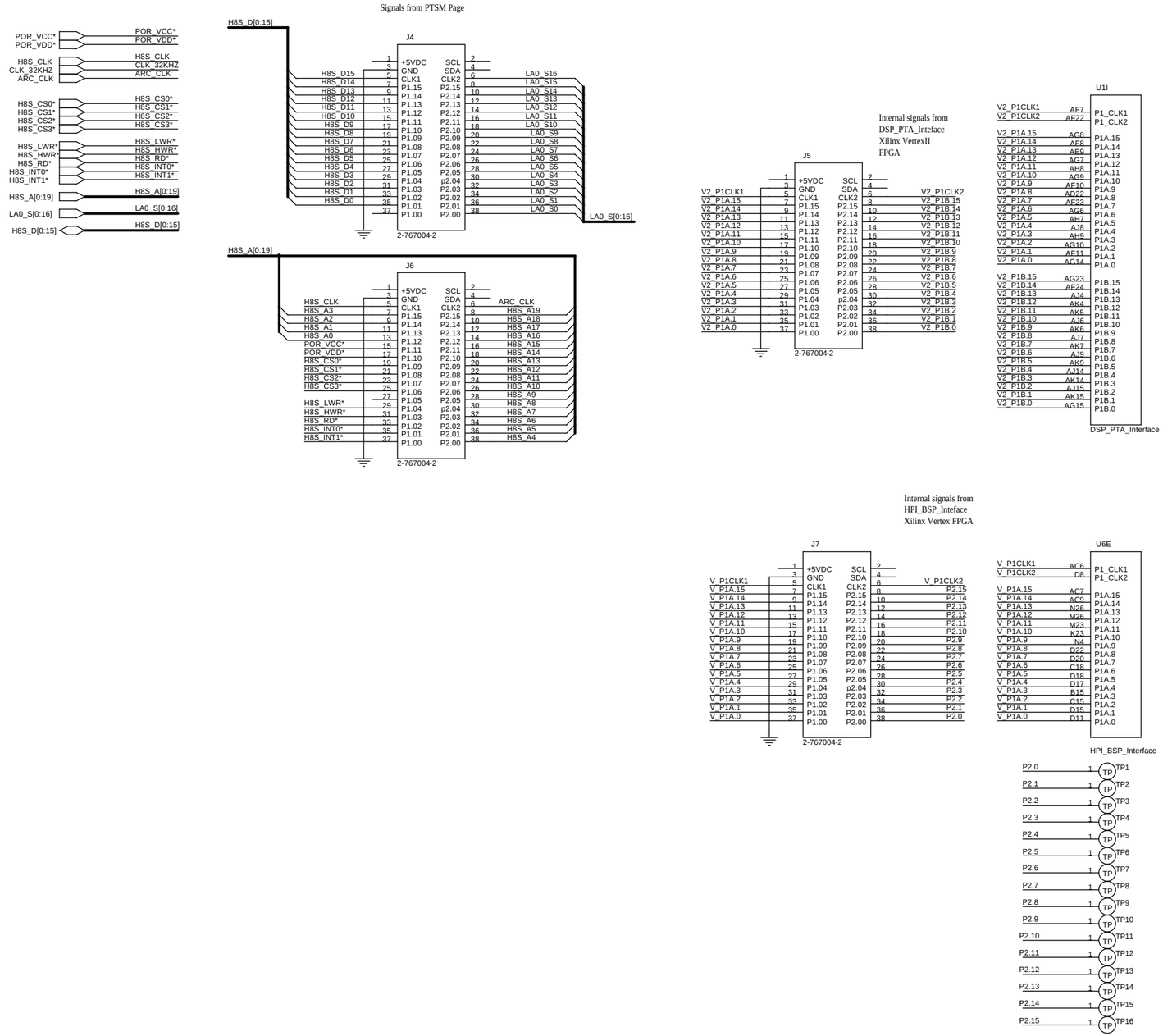


Title
DSP3 Mezzanine Connector

Size	Document Number	Rev
B	GAD/ESEx	1

Date: Tuesday, September 25, 2001 Sheet 8 of 11


Main ATX Power Switch
SW4
GT12MSCKE
P3
ATX_Power
39-29-0203
F5 10Amp
MF-MSMD020-02
F6 10Amp
MF-MSMD020-02
F7 1Amp
1812L050PR
F8 1Amp
1812L050PR
D1 SMBJ5.0A
D2 SMBJ5.0A
D3 SMBJ12A
D4 SMBJ12A
L2 HI2220P171R-00
L3 HI2220P171R-00
C13 .01uF
C14 47uF
C15 .01uF
C16 47uF
C17 220uF ECE-V1CA221P
C20 .01uF
C21 47uF
C22 .01uF
C23 47uF
C24 220uF ECE-V1CA221P
VCC
VDD
+12V
-12V
VirtexII VCCINT Supply
U22
INPUT OUT
SHUTDWN
ADJ GND
1.5V LDO
MIC2941ABU
R11 2K
3214W-1-202E
R12 1K
ERJ-6ENF1001V
R13 4.53K
ERJ-6ENF4531V
C25 .100uF
C0805C101K5RACTR
C18 15uF
T491C156K010AS
VDD1.5
Virtex VCCINT Supply
U25
IN OUT
GND GND
2.5V LDO
MIC39100-2.5BS
C27 10uF
T491C106K010AS
VDD2.5
SW3
B3S-1000
JP5
R10 10K
ERJ-6GEYJ103V
C19 .01uF
MR*
U23
5.0V
MR VDD
WDI
GND RESET
TPS3828-50DBVT
POR_VCC*
C26 .01uF
U24
3.3V
MR VDD
WDI
GND RESET
TPS3828-33DBVT
POR_VDD*
C28 .01uF
U26
VCC OUT
OE
GND
HSM93-25.0000
25Mhz
C29 .01uF
H8S_CLK
TP35
TP36
U27
VCC OUT
OE
GND
32.768Khz
ECS-327SMO
C30 .01uF
CLK_32KHZ
TP37
TP38
U28
VCC OUT
OE
GND
HSM93-20.0000
20Mhz
C31 .01uF
ARC_CLK
TP39
TP40
Power LED's
CR27 GRN 597-3301-107
R14 330 ERJ-6ENF331V
CR28 GRN 597-3301-107
R15 220 ERJ-6ENF221V
CR29 GRN 597-3301-107
R16 1K ERJ-6ENF1001V
CR30 GRN 597-3301-107
R17 1K ERJ-6ENF1001V
U6C
HPI_BSP_Interface
XCV150-5BG352C
H8S_CF-LCD
XC95288XL
C32 .01uF
C33 .01uF
C34 .01uF
C35 .01uF
C36 .01uF
C37 .01uF
C38 .01uF
C39 .01uF
U1C
DSP_PTA_Interface
XC2V1000-5BG575CES
DSP_PTA_Interface
Xilinx VirtexII
C46 .01uF
C47 .01uF
C48 .01uF
C49 .01uF
C50 .01uF
C51 .01uF
C52 .01uF
C53 .01uF
PTA EVENT
FIFO
C40 .01uF
C41 .01uF
C42 .01uF
C43 .01uF
C44 .01uF
C45 .01uF
C54 .01uF
C55 .01uF
C56 .01uF
C57 .01uF
C58 .01uF
C59 .01uF
C60 .01uF
C61 .01uF
HPI_BSP_Interface
Xilinx Virtex
C62 .01uF
C63 .01uF
C64 .01uF
C65 .01uF
C66 .01uF
C67 .01uF
C68 .01uF
C69 .01uF
General purpose power
supply decoupling
C70 47uF
C71 47uF
C72 47uF
C73 47uF
C74 47uF
DSP_PTA_Interface
BootDevice
C75 .01uF
C76 .01uF
C77 .01uF
C78 .01uF
C79 .01uF
C80 .01uF
C81 .01uF
C82 .01uF
C83 .01uF
C84 .01uF
HPI_BSP_Interface
BootDevice
C85 .01uF
C86 .01uF
C87 .01uF
C88 .01uF
C89 .01uF
C90 .01uF
C91 .01uF
C92 .01uF
C93 .01uF
C94 .01uF
C95 47uF
C96 47uF
C97 47uF
C98 47uF
C99 47uF
FPGA Configuration
Status LED's
U29
HPI/BSP_FPGADONE
DSP/PTA_FPGADONE
CR31 597-3401-107 YEL
CR32 597-3401-107 YEL
RP35 220 743C043103JTR
SN74LVC86AD
Install both mode jumpers
for external boot device.
Remove both jumpers
is XC2V1000 is to be booted
from the JTAG chain
RP36 10K 743C043103JTR
U1A
DSP_PTA_Interface
XC2V1000-5FF896CES
Install both mode jumpers
for external boot device.
Remove both jumpers
is XCV150 is to be booted
from the JTAG chain
RP37 10K 743C043103JTR
U31
XC18V01VQ44C
U30
XC18V04VQ44C
U6A
HPI_BSP_Interface
XCV150-5BG352C
JP8
JP9
JP6
JP7
JP10
JP11
RP38 10K 743C043103JTR
RP39 10K 743C043103JTR
ERJ-6GEY301V R19 300
ERJ-6GEY301V R18 300
Jumper Settings:
1-2: Boot Devices are in JTAG Chain
2-3: Boot Devices NOT in JTAG Chain
J17
JTAG Connector
2510-6002UB
PTSM H8S Bypass, Ux
GL1 H8S Bypass, Ux
SN74LV00
LED Drivers
SN74LV86
LED Drivers
GLUE
XC9536XL
LT1381
RS232
DS2480
1Wire
PTSM H8S SRAM
PTSM COM20022
GL1 H8S SRAM
GL1 COM20022
CompactFlash
Socket
SN75ALS176
PTSM
SN75ALS176
GL1
TP41
HPI/BSP_FPGADONE
TEST POINT
TP42
DSP/PTA_FPGADONE
TEST POINT
Hierachical Inputs
MB_TDI
MB_TMS
MB_TCK
Hierachical Outputs
POR_VCC*
POR_VDD*
H8S_CLK
CLK_32KHZ
ARC_CLK
MB_TDO
HPI/BSP_FPGADONE
DSP/PTA_FPGADONE
Title
Power
Size D
Document Number
GAD/ESEx
Rev 1
Date: Monday, October 15, 2001
Sheet 10 of 11



Title	Logic Analyzer Connectors
Size C	Document Number GAD/ESEx
Rev	1
Date:	Thursday, October 11, 2001
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